## SWITCHMODE ${ }^{\text {™ }}$ Series NPN Silicon Power Transistors

The BUS98 and BUS98A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated SWITCHMODE applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times

60 ns Inductive Fall Time $-25^{\circ} \mathrm{C}$ (Typ) 120 ns Inductive Crossover Time $-25^{\circ} \mathrm{C}$ (Typ)

- Operating Temperature Range -65 to $+200^{\circ} \mathrm{C}$

- $100^{\circ} \mathrm{C}$ Performance Specified for:

Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents ( $125^{\circ} \mathrm{C}$ )

## MAXIMUM RATINGS

| Rating | Symbol | BUS98 | BUS98A | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Collector-Emitter Voltage | $\mathrm{V}_{\text {CEO(sus) }}$ | 400 | 450 | Vdc |
| Collector-Emitter Voltage | $\mathrm{V}_{\text {CEV }}$ | 850 | 1000 | Vdc |
| Emitter Base Voltage | $\mathrm{V}_{\mathrm{EB}}$ | 7 |  | Vdc |
| $\begin{aligned} & \text { Collector Current } \text { - Continuous } \\ & \text { - Peak (1) } \\ & \text { Overload } \end{aligned}$ | $\begin{gathered} \mathrm{I}_{\mathrm{C}} \\ \mathrm{I}_{\mathrm{CM}} \\ \mathrm{I}_{\mathrm{ol}} \\ \hline \end{gathered}$ | $\begin{gathered} 30 \\ 60 \\ 120 \end{gathered}$ |  | Adc |
| Base Current - Continuous <br> - Peak (1) | $\begin{gathered} \mathrm{I}_{\mathrm{B}} \\ \mathrm{I}_{\mathrm{BM}} \end{gathered}$ | $\begin{aligned} & 10 \\ & 30 \end{aligned}$ |  | Adc |
| $\begin{gathered} \hline \text { Total Power Dissipation }-\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C} \\ \text { Derate above } 25^{\circ} \mathrm{C} \end{gathered}$ | $P_{\text {D }}$ | $\begin{aligned} & 250 \\ & 142 \\ & 1.42 \end{aligned}$ |  | Watts <br> $\mathrm{W} /{ }^{\circ} \mathrm{C}$ |
| Operating and Storage Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}, \mathrm{T}_{\text {stg }}$ | -65 to +200 |  | ${ }^{\circ} \mathrm{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
| :--- | :---: | :---: | :---: |
| Thermal Resistance, <br> Junction to Case | $\mathrm{R}_{\text {өJC }}$ | 0.7 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Maximum Lead Temperature <br> for Soldering Purposes: <br> $1 / 8 "$ from Case for 5 Seconds | $\mathrm{T}_{\mathrm{L}}$ | 275 | ${ }^{\circ} \mathrm{C}$ |

(1) Pulse Test: Pulse Width $=5 \mathrm{~ms}$, Duty Cycle $\leqq 10 \%$. Designer's and SWITCHMODE are trademarks of ON Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS ( $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ unless otherwise noted)

| Characteristic |  | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OFF CHARACTERISTICS (1) |  |  |  |  |  |  |
| Collector-Emitter Sustaining Voltage (Table 1) $\left(\mathrm{I}_{\mathrm{C}}=200 \mathrm{~mA}, \mathrm{I}_{\mathrm{B}}=0\right) \mathrm{L}=25 \mathrm{mH}$ | $\begin{aligned} & \text { BUS98 } \\ & \text { BUS98A } \end{aligned}$ | $\mathrm{V}_{\text {CEO(sus) }}$ | $\begin{aligned} & 400 \\ & 450 \end{aligned}$ | - | - | Vdc |
| Collector Cutoff Current $\begin{aligned} & \left(\mathrm{V}_{\mathrm{CEV}}=\text { Rated Value, } \mathrm{V}_{\mathrm{BE}(\text { off })}=1.5 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{CEV}}=\text { Rated Value, } \mathrm{V}_{\mathrm{BE} \text { (off })}=1.5 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{C}}=125^{\circ} \mathrm{C}\right) \end{aligned}$ |  | $I_{\text {cev }}$ |  |  | $\begin{aligned} & 0.4 \\ & 4.0 \end{aligned}$ | mAdc |
| $\begin{aligned} & \text { Collector Cutoff Current } \\ & \left(\mathrm{V}_{\mathrm{CE}}=\text { Rated } \mathrm{V}_{\mathrm{CEV}}, \mathrm{R}_{\mathrm{BE}}=10 \Omega\right) \end{aligned}$ | $\begin{aligned} & \mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{C}}=125^{\circ} \mathrm{C} \end{aligned}$ | $I_{\text {CER }}$ |  |  | $\begin{aligned} & 1.0 \\ & 6.0 \end{aligned}$ | mAdc |
| Emitter Cutoff Current $\left(\mathrm{V}_{\mathrm{EB}}=7 \mathrm{Vdc}, \mathrm{I}_{\mathrm{C}}=0\right)$ |  | $\mathrm{I}_{\text {ebo }}$ | - | - | 0.2 | mAdc |
| Emitter-Base Breakdown Voltage $\left(I_{E}=100 \mathrm{~mA}-\mathrm{I}_{\mathrm{C}}=0\right)$ |  | $\mathrm{V}_{\text {EBO }}$ | 7.0 | - | - | Vdc |

SECOND BREAKDOWN

| Second Breakdown Collector Current with Base Forward Biased | $\mathrm{I}_{\mathrm{S} / \mathrm{b}}$ |  | See Figure 12 |  |
| :--- | :---: | :---: | :---: | :---: |
| Clamped Inductive SOA with Base Reverse Biased | RBSOA |  | See Figure 13 |  |

ON CHARACTERISTICS (1)

| $\begin{aligned} & \text { DC Current Gain } \\ & \left(I_{\mathrm{C}}=20 \mathrm{Adc}, \mathrm{~V}_{\mathrm{CE}}=5 \mathrm{Vdc}\right) \\ & \left(\mathrm{I}_{\mathrm{C}}=16 \mathrm{Adc}, \mathrm{~V}_{\mathrm{CE}}=5 \mathrm{~V}\right) \end{aligned}$ | $\begin{aligned} & \text { BUS98 } \\ & \text { BUS98A } \end{aligned}$ | $\mathrm{h}_{\text {FE }}$ | 8 | - | - | - |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Collector-Emitter Saturation Voltage } \\ & \left(I_{C}=20 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=4 \mathrm{Adc}\right) \\ & \left(I_{C}=30 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=8 \mathrm{Adc}\right) \\ & \left(I_{C}=20 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=4 \mathrm{Adc}, \mathrm{~T}_{\mathrm{C}}=100^{\circ} \mathrm{C}\right) \\ & \left(I_{\mathrm{C}}=16 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=3.2 \mathrm{Adc}\right) \\ & \left(I_{C}=24 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=5 \mathrm{Adc}\right) \\ & \left(I_{C}=16 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=3.2 \mathrm{Adc}, \mathrm{~T}_{\mathrm{C}}=100^{\circ} \mathrm{C}\right) \end{aligned}$ | $\begin{aligned} & \text { BUS98 } \\ & \text { BUS98A } \end{aligned}$ | $\mathrm{V}_{\text {CE(sat) }}$ | $\begin{aligned} & - \\ & - \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & - \\ & - \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 3.5 \\ & 2.0 \\ & 1.5 \\ & 5.0 \\ & 2.0 \end{aligned}$ | Vdc |
| $\begin{aligned} & \text { Base-Emitter Saturation Voltage } \\ & \text { ( } \left.I_{C}=20 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=4 \mathrm{Adc}\right) \\ & \left(\mathrm{I}_{\mathrm{C}}=20 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=4 \mathrm{Adc}, \mathrm{~T}_{\mathrm{C}}=100^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{I}_{\mathrm{C}}=16 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=3.2 \mathrm{Adc}\right) \\ & \left(\mathrm{I}_{\mathrm{C}}=16 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=3.2 \mathrm{Adc}, \mathrm{~T}_{\mathrm{C}}=100^{\circ} \mathrm{C}\right) \end{aligned}$ | $\begin{aligned} & \text { BUS98 } \\ & \text { BUS98A } \end{aligned}$ | $\mathrm{V}_{\mathrm{BE} \text { (sat) }}$ | - | - | $\begin{aligned} & 1.6 \\ & 1.6 \\ & 1.6 \\ & 1.6 \end{aligned}$ | Vdc |

DYNAMIC CHARACTERISTICS

| Output Capacitance <br> $\left(\mathrm{V}_{\mathrm{CB}}=10 \mathrm{Vdc}, \mathrm{I}_{\mathrm{E}}=0, \mathrm{f}_{\text {test }}=100 \mathrm{kHz}\right)$ | $\mathrm{C}_{\mathrm{ob}}$ | - | - | 700 |
| :--- | :--- | :--- | :--- | :--- |

## SWITCHING CHARACTERISTICS

## Restive Load (Table 1)

| Delay Time | $\begin{gathered} \left(\mathrm{V}_{\mathrm{CC}}=250 \mathrm{Vdc}, \mathrm{I}_{\mathrm{C}}=20 \mathrm{~A},\right. \\ \mathrm{I}_{\mathrm{B} 1}=4.0 \mathrm{~A}, \mathrm{t}_{\mathrm{p}}=30 \mu \mathrm{~s}, \\ \text { Duty Cycle } \leq 2 \%, \mathrm{~V}_{\mathrm{BE}} \text { (off) }=5 \mathrm{~V} \text { ) } \\ \text { (for BUS98A: } \mathrm{I}_{\mathrm{C}}=16 \mathrm{~A}, \mathrm{Ib}_{1}=3.2 \mathrm{~A} \text { ) } \end{gathered}$ | $t_{d}$ | - | 0.1 | 0.2 | $\mu \mathrm{s}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Rise Time |  | $\mathrm{t}_{\mathrm{r}}$ | - | 0.4 | 0.7 |  |
| Storage Time |  | $\mathrm{t}_{\text {s }}$ | - | 1.55 | 2.3 |  |
| Fall Time |  | $t_{f}$ | - | 0.2 | 0.4 |  |

Inductive Load, Clamped (Table 1)

| Storage Time | $\begin{aligned} & \mathrm{I}_{\mathrm{C}(\mathrm{pk})}=20 \mathrm{~A} \\ & \mathrm{I}_{\mathrm{b} 1}=4 \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{BE}(\mathrm{off})}=5 \mathrm{~V}, \\ & \left.\mathrm{~V}_{\mathrm{CE}(\mathrm{c} 1)}=250 \mathrm{~V}\right) \\ & \mathrm{I}_{\mathrm{C}(\mathrm{pk})}=16 \mathrm{~A} \\ & (\mathrm{I} \\ & \left.\mathrm{IB}_{1}=3.2 \mathrm{~A}\right) \end{aligned}$ | (BUS98) |  | $\mathrm{t}_{\text {sv }}$ | - | 1.55 | - | $\mu \mathrm{s}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Fall Time |  | (BUS98A | $\left(\mathrm{T}^{\mathrm{C}}=25^{\circ} \mathrm{C}\right.$ ) | $t_{\text {fi }}$ | - | 0.06 | - |  |
| Storage Time |  |  | $\left(\mathrm{T}_{\mathrm{C}}=100^{\circ} \mathrm{C}\right)$ | $\mathrm{t}_{\text {sv }}$ | - | 1.8 | 2.8 |  |
| Crossover Time |  |  |  | $\mathrm{t}_{\mathrm{c}}$ | - | 0.3 | 0.6 |  |
| Fall Time |  |  |  | $\mathrm{t}_{\mathrm{fi}}$ | - | 0.17 | 0.35 |  |

(1) Pulse Test: PW $=300 \mu \mathrm{~s}$, Duty Cycle $\leq 2 \%$.

## BUS98 BUS98A

## DC CHARACTERISTICS



Figure 1. DC Current Gain


Figure 2. Collector Saturation Region

$\mathrm{I}_{\mathrm{C}}$, COLLECTOR CURRENT (AMPS)
Figure 3. Collector-Emitter Saturation Voltage


Figure 4. Base-Emitter Voltage


Figure 5. Collector Cutoff Region


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

|  | $\mathrm{V}_{\text {CEO(sus) }}$ | RBSOA AND INDUCTIVE SWITCHING |  | RESISTIVE SWITCHING |
| :---: | :---: | :---: | :---: | :---: |
|  | PW Varied to Attain $\mathrm{I}_{\mathrm{C}}=100 \mathrm{~mA}$ |  |  | TURN-ON TIME <br> $I_{B 1}$ adjusted to obtain the forced $h_{\text {FE }}$ desired <br> TURN-OFF TIME <br> Use inductive switching driver as the input to the resistive test circuit. |
|  | $\begin{aligned} & \mathrm{L}_{\text {coil }}=25 \mathrm{mH}, \mathrm{~V}_{\mathrm{CC}}=10 \mathrm{~V} \\ & \mathrm{R}_{\text {coil }}=0.7 \Omega \end{aligned}$ |  | $\begin{array}{ll} \mathrm{L}_{\text {coil }}=180 \mu \mathrm{H} & \\ \mathrm{R}_{\text {coil }}=0.05 \Omega & \mathrm{~V}_{\text {clamp }}=250 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=20 \mathrm{~V} & \end{array}$ | $V_{C C}=250 \mathrm{~V}$ <br> Pulse Width $=10 \mu \mathrm{~s}$ |
|  | INDUCTIVE | EST CIRCUIT | OUTPUT WAVEFORMS <br> $t_{1}$ Adjusted to Obtain IC $\begin{aligned} & t_{1} \approx \frac{L_{\text {coil }}\left(I_{C(p k)}\right)}{V_{C C}} \\ & t_{2} \approx \frac{L_{\text {coil }}\left(\mathrm{I}_{\mathrm{C}(\mathrm{pk}))}\right.}{\mathrm{V}_{\text {clamp }}} \end{aligned}$ <br> Test Equipment Scope - Tektronix 475 or Equivalent | RESISTIVE TEST CIRCUIT |



Figure 7. Inductive Switching Measurements


Figure 8. Peak-Reverse Current

## BUS98 BUS98A

## SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.
$\mathrm{t}_{\mathrm{sv}}=$ Voltage Storage Time, $90 \% \mathrm{I}_{\mathrm{B} 1}$ to $10 \% \mathrm{~V}_{\text {clamp }}$
$\mathrm{t}_{\mathrm{rv}}=$ Voltage Rise Time, $10-90 \% \mathrm{~V}_{\text {clamp }}$
$\mathrm{t}_{\mathrm{fi}}=$ Current Fall Time, $90-10 \% \mathrm{I}_{\mathrm{C}}$
$\mathrm{t}_{\mathrm{ti}}=$ Current Tail, $10-2 \% \mathrm{I}_{\mathrm{C}}$
$\mathrm{t}_{\mathrm{c}}=$ Crossover Time, $10 \% \mathrm{~V}_{\text {clamp }}$ to $10 \% \mathrm{I}_{\mathrm{C}}$
An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity


Figure 9. Storage Time, $\mathrm{t}_{\mathrm{sv}}$
of these terms.
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from $\mathrm{AN}-222$ :

$$
\mathrm{P}_{\mathrm{SWT}}=1 / 2 \mathrm{~V}_{\mathrm{CC}} \mathrm{l}_{\mathrm{C}}\left(\mathrm{t}_{\mathrm{C}}\right) \mathrm{f}
$$

In general, $t_{r v}+t_{f i} \simeq t_{c}$. However, at lower test currents this relationship may not be valid.
As is common with most switching transistors, resistive switching is specified at $25^{\circ} \mathrm{C}$ and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds ( $\mathrm{t}_{\mathrm{c}}$ and $\mathrm{t}_{\mathrm{sv}}$ ) which are guaranteed at $100^{\circ} \mathrm{C}$.INDUCTIVE SWITCHING


Figure 10. Crossover and Fall Times


Figure 11. Turn-Off Times versus Forced Gain


Figure 12. Turn-Off TM Times versus $\mathrm{Ib}_{2} / \mathrm{lb}_{1}$

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.


Figure 13. Forward Bias Safe Operating Area


Figure 14. Reverse Bias Safe Operating Area

## SAFE OPERATING AREA INFORMATION

## FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_{C}-V_{C E}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C} ; \mathrm{T}_{\mathrm{J}(\mathrm{pk})}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to $10 \%$ but must be derated when $\mathrm{T}_{\mathrm{C}} \geq 25^{\circ} \mathrm{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.
$\mathrm{T}_{\mathrm{J}(\mathrm{pk})}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

## REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives RBSOA characteristics.


Figure 15. Power Derating


Figure 16. Thermal Response

## OVERLOAD CHARACTERISTICS



Figure 17. Rated Overload Safe Operating Area (OLSOA)


Figure 18. Figure 17. $\mathrm{I}_{\mathrm{C}}=\mathrm{f}(\mathrm{dV} / \mathrm{dt})$

## OLSOA

OLSOA applies when maximum collector current is limited and known. A good example Is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 17 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 19) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

## Notes:

- $V_{C E}=V_{C C}+V_{B E}$
- Adjust pulsed current source for desired $\mathrm{I}_{\mathrm{C}}, \mathrm{t}_{\mathrm{p}}$


BUS98 BUS98A

## PACKAGE DIMENSIONS

TO-204AA (TO-3)
CASE 1-07
ISSUE Z


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 1.550 REF |  | 39.37 REF |  |
| B | --- | 1.050 | --- | 26.67 |
| C | 0.250 | 0.335 | 6.35 | 8.51 |
| D | 0.038 | 0.043 | 0.97 | 1.09 |
| E | 0.055 | 0.070 | 1.40 | 1.77 |
| G | 0.430 BSC |  | 10.92 BSC |  |
| H | 0.215 BSC |  | 5.46 BSC |  |
| K | 0.440 | 0.480 | 11.18 | 12.19 |
| L | 0.665 BSC |  | 16.89 BSC |  |
| N | --- | 0.830 | --- | 21.08 |
| Q | 0.151 | 0.165 | 3.84 | 4.19 |
| U | 1.187 BSC |  | 30.15 BSC |  |
| V | 0.131 | 0.188 | 3.33 | 4.77 |

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#### Abstract

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