Surfacing the facts of DMOS Power RF transistors from Published Data Sheets

by
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POLYFET RF DEVICES
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Power RF Mosfets have made considerable progress since the days of introduction some 15 years ago. Original manufacturers, Siliconix and Acrian have left the field, but others have come to take their places. The technology has improved over the course of the years mainly by changing device methodology from VMOS to DMOS structure. Compared to the capabilities achieved in the very early days, we now see power output of up to 600W at 30 Mhz being achieved by Motorola and up to 20W at 1000 Mhz delivered by Polyfet on gold metallized devices.

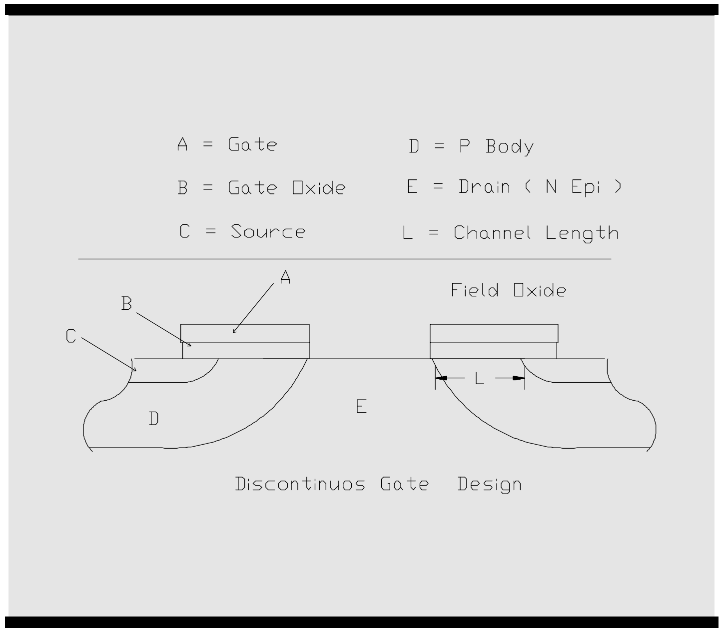


Fig **1**. Cross Section of Vertical DMOS transistor

The industry is now served by a few select companies, namely :- Polyfet RF Devices (Producer of the first gold metallized Fets), MA-COM PHI, Motorola, Phillips and Thomson CSF. The N-channel enhancement mode vertical D-MOS transistor is the choice structure employed by these companies. Although DMOS is the common denominator, there are enough differences in design and processing details to distinguish transistors from one make to another despite similar RF attributes. Therefore, more than likely, some re-tuning of the matching networks will be required when substituting devices. This is also true of Semetex counterfeit devices. (Semetex is neither a licensee nor a approved second source of Polyfet's patented devices.)

Some of the key parameters affecting RF performance are junction and parasitic capacitances, Gm (Forward Transconductance) and maximum drain current, Idsat. Most of this information is readily available from published data sheets. It is the intent of this article to provide the RF engineer some basic knowledge of how to extract "behind the scene" information of the various manufacturers to identify the different die geometries used to create their line of transistors.

Vertical DMOS Basics

First, we shall review the fundamentals of the DMOS transistor in order to relate physical properties to data sheet electrical parameters.

Fig. 2 shows the cross section of a Vertical DMOS structure for a continuous gate design, employed by most manufacturers, and Fig 1 shows the discontinuous gate design employed by Polyfet. The term DMOS stands for Double Diffused MOS. Although this technology was invented over 30 years ago, its progress was overshadowed by the success of the now familiar lateral device structure universally employed for digital MOS circuits. Originally one of the primary advantage of DMOS over standard MOS was the ability to form and control very narrow channels. Whereas standard MOS relied on photo-lithography to control channel lengths of about 5 - 7 microns; DMOS was able to achieve controls of 2 micron or less by depending on precise and controllable diffusion junction depths. In DMOS processing the channel length is formed by the difference in side diffusion between the N^{++} Source diffusion and the P^- Body diffusion. Current flow of a enhancement mode DMOS transistor begins when a positive gate voltage greater than the threshold voltage of the device is applied. Referring to Fig. 2., the current flows laterally from the source, through the channel and then "vertically" down to the drain. The term Vertical DMOS is derived from this pattern of current flow. This pictorial representation of current flow is the "T" in Motorola's TMOS devices.

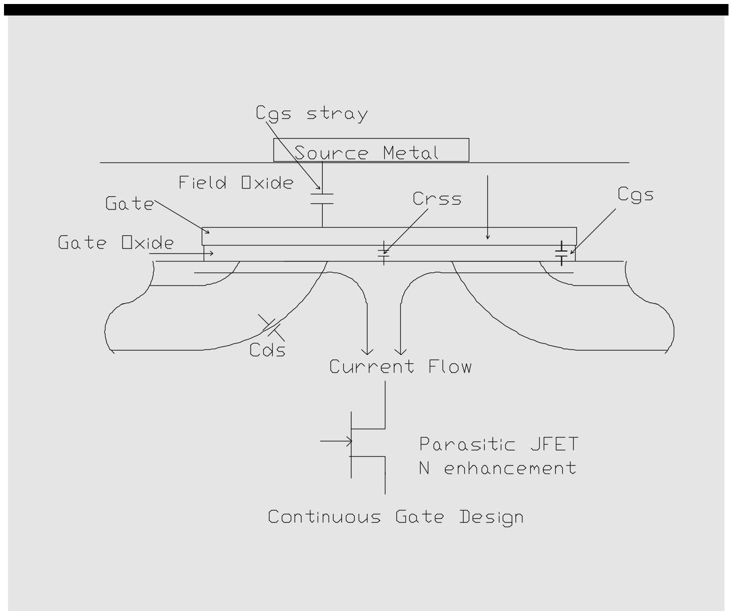


Fig **2**. VDMOS Continuous Gate Design

Drain Current to Gate Voltage Relationship

The classical square law equation describing current flow for MOS devices when the drain voltage that is much greater than the Gate voltage, is describe below in Eq. 1. However this equation does not hold for short channel DMOS devices, especially at higher current levels, due to carrier velocity saturation in a high longitudinal electric field. At high drain currents, Id is better described by Eq. 2.

$$Id \_ 0.5\frac{W}{L}u_n C_o(V_G - V_T)^2 \qquad \mathbf{1}$$

where:-

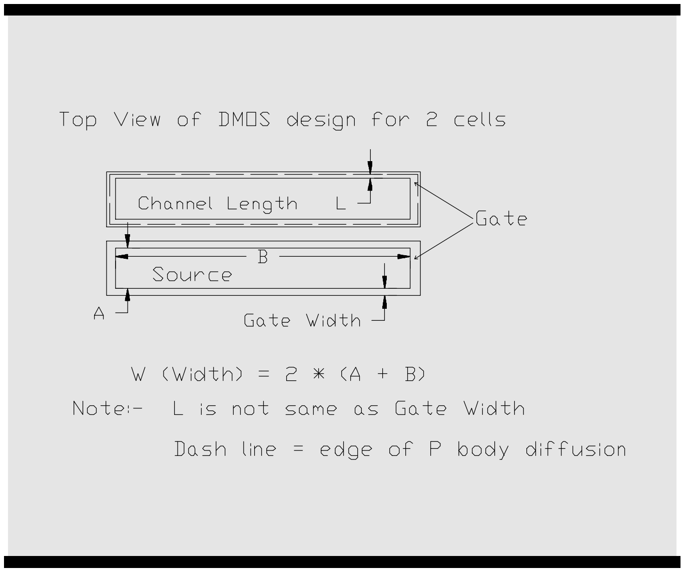
Id = Drain current
W = Width of the gate of the transistor. (Perimeter)
L = Channel length.
u_n = Electron mobility
C_o = Gate capacitance per unit area; inversely proportional to gate oxide thickness
Vg = Applied Gate voltage.
Vt = Gate threshold voltage. (Usually measured as the gate voltage required to cause 1 ua of drain current to flow. Not to be confused by data sheet $VGS_{(th)}$ which is measured at very high drain currents.)

$$Id \_ WC_o(V_G - V_T)v_s \qquad \mathbf{2}$$

where:-

v_s = electron drift velocity

The width, W, of the gate deserves further clarification. Fig 3. shows a top view of a DMOS transistor cell. In high power DMOS transistor designs, many cells are paralleled together to achieve a large W value; thus achieving a large perimeter value. In the case of the Polyfet design, W for the F1 and F2 dice are 6 cm and 1.25 cm long respectively. The channel length, L, which is often called the gate length, is defined by the lateral spacing difference formed by the side diffusions of the source and the P body. Unlike, lateral MOS devices, it is independent of the gate material geometry. For Polyfet designs, L is 1.5 micron wide. Large W/L ratios is necessary to achieve high Idsat and low Rdon values. In contrast to Bipolar transistors which has the benefit of base conductivity modulation to obtain low saturation voltages, MOS transistors have to resort to large active areas to achieve same. This is the prime reason DMOS transistors are more expensive then their bipolar counter parts. However, DMOS transistors have many superior attributes, such as higher power gain and wider bandwidth, to more than justify the premium.



From Equation 1. we note the other parameters that one can adjust to achieve high Idsat are higher electron mobility and C_o. Mobility is affected by doping density and silicon crystal orientation. The main advantage of DMOS over VMOS is that mobility is higher; due to the difference in crystal plane, <111> vs <100>, along which the electrons flow. (650 vs 450 cm^2 per volt-sec.) C_o can be enhanced by thinning down the gate oxide thickness. This value ranges from 800 ^{o}A to 1200^o from manufacturer to manufacturer. The trade off with thin gate oxides is lower Gate to Source voltages at which point it would rupture. Most manufacturers guarantee a minimum of 40V for gate oxide breakdown while typical values are in excess of 60v. The other trade offs with thin gate oxides are increases in parasitic capacitances Crss and Ciss.

Another process parameter change that can improve Idsat and Rdsat (Rdon) is increase in doping of the epi material. A higher doped epi lowers the drain resistance. However, the final limitation is governed by the desired minimum Bvdss value. To achieve a Bvdss of greater than 65 volts and to achieve some degree of ruggedness, doping levels are usually kept at about 2 ohm-cm for the epi. Parasitic capacitance, Coss, is directly affected by epi doping density. Using high doping densities to achieve low Rdsat has the penalty of higher Coss values.

Gm - Forward Transconductance

Gm is measured as a ratio of a change in drain current to a change in gate voltage at a fixed drain to source voltage. Gm is not a constant and varies with applied gate voltages. Fig 4. shows a typical plot of Gm and Id vs Vg for a Polyfet F1B die and the equivalent part from PHI; UF series. At low gate voltages, Gm increases with increasing gate voltage as governed by the square law relationship described in Equation 1 and 3. At higher gate voltage of about 4 - 6 volts Gm begins to saturate in accordance to Eq 2 and 4. Both devices have very similar characteristics and are rated similarly in RF power as well.

At the maximum value of Gm, the scattering-limited drift velocity has a value of about 6.5 X 10^6 cm/sec. For devices with 1000^{o}A of gate oxide, maximum Gm/unit length of perimeter is 24umho/micron. At even higher gate voltages, Gm begins to fall off due to the pinching effects of the parasitic JFET and finite source and drain resistances. The rate of Gm fall off can be reduced by keeping the P body separation large. The adverse effect is an increase in gate to drain capacitance for the continuous gate designs.

Unlike Bipolar transistors where Beta increases with temperature, Gm decreases with increasing temperature. This self regulating feature prevents thermal runaway, adding to the ruggedness of the MOSFET transistor.

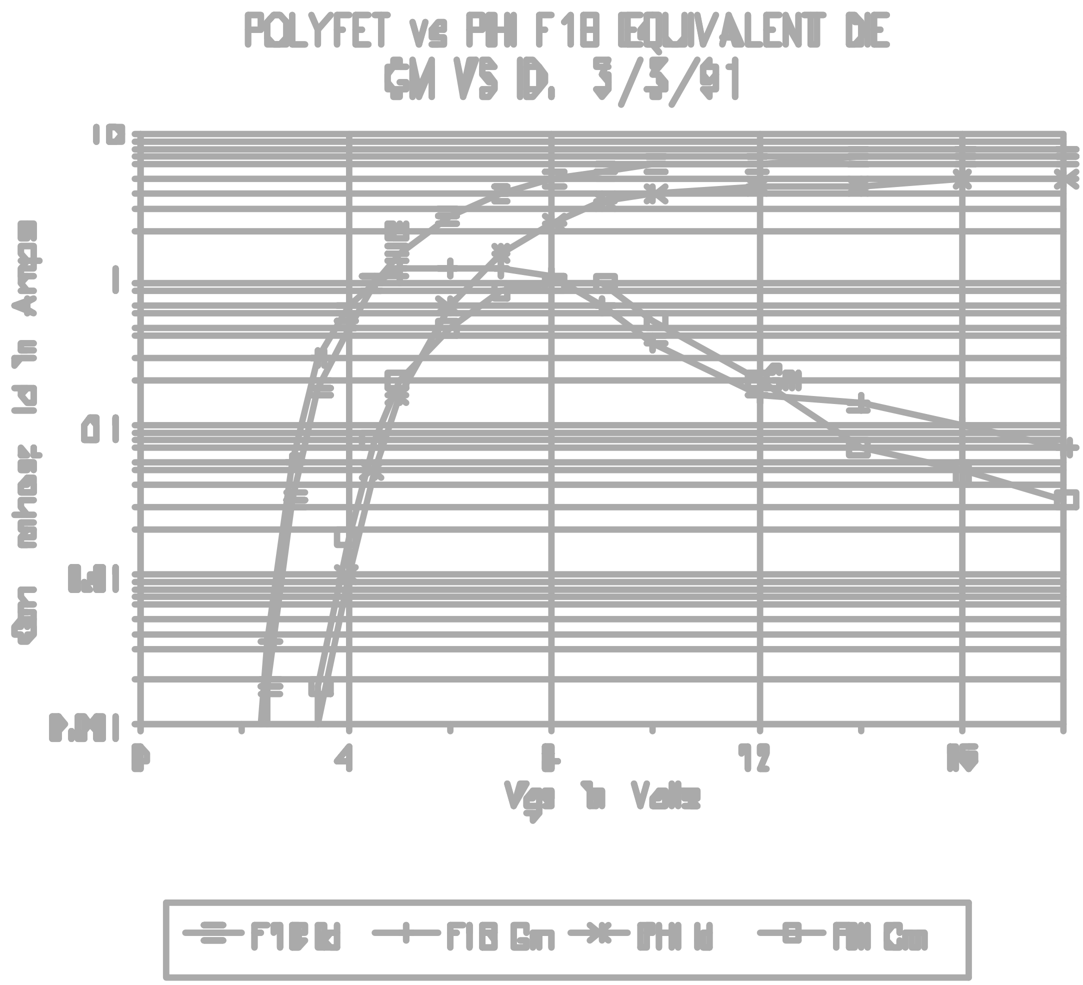


Fig 4. Gm vs Id Polyfet and PHI F1B equivalent die

$$G_m = \frac{W}{L} u_n C_O (V_G - V_T)$$ Derivative of Eq 1. **3**

$$G_m = W C_o v_s$$ Derivative of Eq. 2 **4**

Note Gm is a constant

A very important feature of a RF transistor is its maximum frequency of operation, ft. ft is directly proportional to Gm and inversely proportional to input capacitance. Further more, since Gm is proportional to W/L; it can be shown that ft is inversely proportional to the square of the channel length, L.

$$f_t \propto \frac{u_n}{L^2} \qquad 6$$

RF power gain in an amplifier has been demonstrated to be a function of Gm as well. This relationship is shown in Equation 7.

Obviously, to have good RF performance, power gain and linearity, it is desirous to have Gm

$$f_t \propto \frac{gm}{C_{iss}} \qquad 5$$

$$G_p \propto 10 \log Gm^2 \qquad 7$$

characteristics that are high, obtained at low gate voltages and be as flat a possible over a wide range of gate voltage. Achieving all these require good device design and manufacturing techniques.

Since the other key parameter to obtaining good RF performance is low Crss, an important relationship exists between Gm and Crss. The higher the Gm/Crss ratio, the higher the RF performance capability of the transistor.

Capacitances

Three capacitances associated with the MOS device are shown in Fig. 5. The gate structure has capacitances to both the drain, Cgd, and the source, Cgs. The inherent P body to N drain junction forms Cds. However, instead of these capacitances, all RF manufacturers report values for Ciss, Crss and Coss in their data sheets. Ciss is the parallel combination of Cgs and Cgd and Coss is the parallel combination of Cds and Cgd. Crss is the same as Cgd. Since Cgd is quite small compared to Cds, Coss is nearly equal to Cds. The relationship of these capacitances to voltage bias for a F1B Polyfet die is shown in Fig 6.

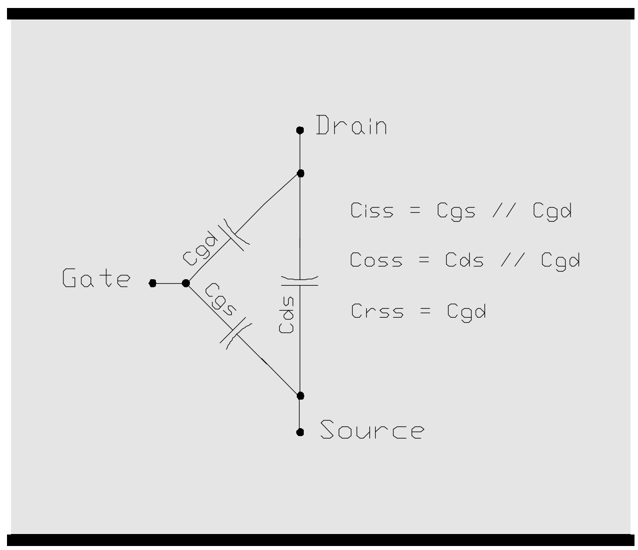


Fig 5 DMOS Capacitances

Coss - Output Capacitance

This is primarily a diode junction capacitance formed between the P body and the Nepi. As with any PN junction capacitance, its has its highest value when there is no bias across Drain to Source/Body. Upon application of a drain voltage, a depletion layer which increases in width with increasing drain voltage is formed. See Fig. 6. As the depletion width increases, capacitance, which is inversely proportional to its plate spacing, falls rapidly. All manufacturers specify Coss at 28V VDS, when it is at its minimum. Since Coss is P body area dependent and epi doping is very similar in value among all manufacturers, for equal Bvdss devices, the value of Coss can be used as a direct comparison of the active device area from one design to another.

Ciss - Input Capacitance

Ciss does not vary as much with Drain to Source voltage bias. Most of this capacitance is formed between Source metal interconnects to Gate material. The dielectric between these two materials is silicon dioxide. Other than keeping this oxide at a maximum, the other option is to keep the Source metal area at a minimum. This is more easily achieved by using Gold metallization because this has a higher current density capability compared to Aluminum. Other contributions to Ciss is Gate to Source overlap capacitance and gate to channel capacitance. Gate to Source overlap is the area formed by the side diffusion of the Source under the gate material. In typical DMOS processing, this is in the order of perhaps half a micron. With the Patented Polyfet process, this overlap is essentially zero. Therefore, with any given transistor size, a low value of Ciss is desirable. The importance of a low value of Ciss in relationship to ft is shown in Eq. 5.

Crss - Feedback capacitance

Despite being the lowest in absolute value among the three capacitances, it has the most effect on RF performance. As in a bipolar transistor, this is also a Miller capacitance and suffers from voltage gain multiplication; See Eq. 8. At zero bias voltage, this capacitance is formed between

$$C_{Miller} \approx Crss(1 + Gm * R_L)$$

Miller Crss Eq. **8**

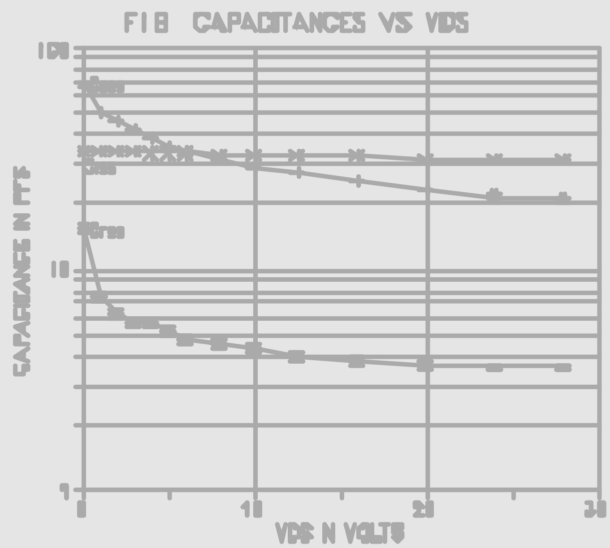


Fig 6. Capacitance vs Vds for Polyfet F1B devices

the gate material and the drain. As drain voltage is applied, the depletion width formed at the P body and drain junction creates another capacitor which connects in series to the former. Being of a lower value, it ultimately dominates as drain voltage is increased. This explains the rapidly falling value of Crss to increasing Vds. For continuous gate designs, the separation distance between P body to P body is kept a minimum to achieve low Crss values. This has the disadvantage of reducing Idsat because it reduces the parasitic JFET current saturation capability. Visualize this as the throat of a pipe being squeezed down in size by the infringing P body diffusions. Given any active transistor area, keeping Crss small while not impairing Idsat, is the key challenge to all RF device designers. A good figure of merit for a RF transistor is a low ratio of Crss/Coss.

Ratio Analysis

By examining ratios of the above mentioned parameters one can determine the make up of a transistor. It is common practice in Power RF transistor

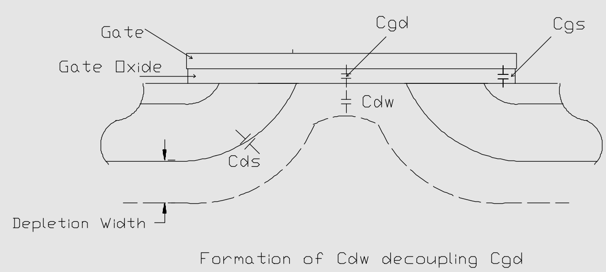


Fig 7. Crss with Reverse Bias Voltage, Vds.

manufacturing to wire bond dice in parallel to achieve higher Power output levels. As an example, the Polyfet F2001 is made with one die in a package and is rated at 2.5W out at 1000 Mhz. When 4 dice are wired in parallel in the same package, the part is rated at 10W out at 1000 Ghz; F2012. Upon reviewing the values of Gm and capacitances in the data sheets, a ratio of 4 between the two transistors can be seen. As another example, this same ratio is found between the BL242 and the BL244 devices. (See Table 1. for details)

The above examples describe single ended devices. Push pull transistors are assembled with two single ended devices on a common flange. Data sheets report DC characteristic for one side only. A comparison study between PHI UF2820R and UF2840P identifies the former as having one die in a single ended configuration and the later a 1+1 in a push pull configuration. The push pull is rated at 40W vs the single ended at 20W. On the other hand, the 28100M is a 3+3 in a push pull configuration as evidenced by a ratio of 3 in capacitance and Gm values.

Die identity can be obtain by evaluating ratios such as Gm/Crss and Crss/Coss and absolute values of Coss. By this method one can determine the different basic die types used to create a product line. Additionally, the generic die that is used to make up a product line can be identified this way. Manufacturers will use the same die to create two or more lines by testing at different frequencies. This is evident between the PHI UF28XX devices and their LF28xx devices. Note the ratios of Gm/Crss, Gm/Coss and Crss/Coss are the same for these two series, indicating the same generic die is being used. Additionally, the LF2805A and the UF2805B are the same part tested at different frequencies.

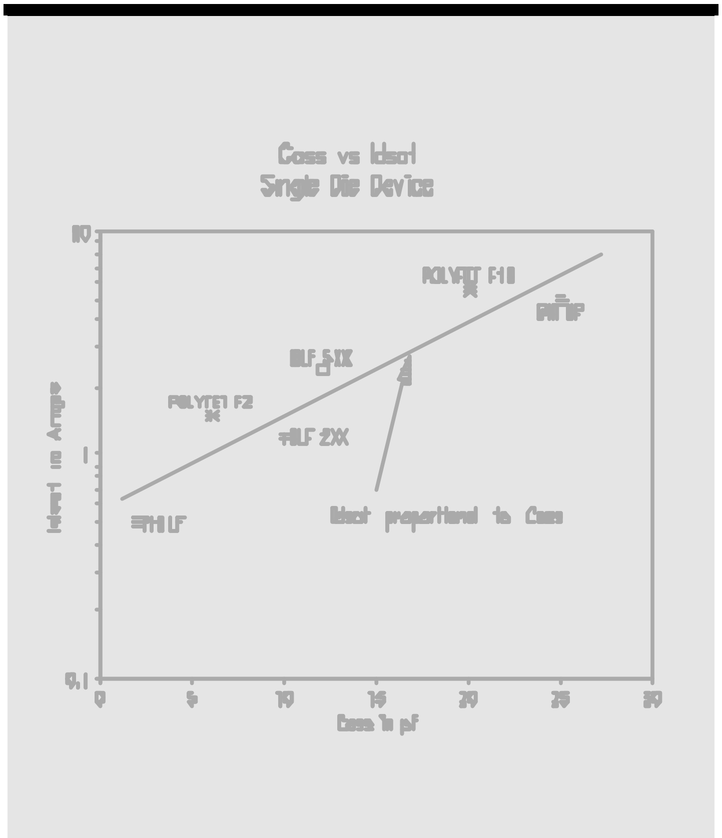


Fig 8. Id vs Coss for a single die device

Fig 8. is a plot of Coss vs Idsat for parts from various manufacturers. The correlation between the two is strong. As mentioned earlier. Coss is a directly proportional to W/L which is one of the key parameters in the Idsat equation. (See Eq. 1 & 2) In Table 1. the single die devices' Coss is highlighted.

Conclusion

There is a lot that can be learned by careful study of Data Sheets. By having a better knowledge of the die make up of a transistor and or product line make up, the RF engineer has more to profit when choosing transistors for his applications.

Table 1.

Comparison of various device characteristics

S.E.=Single Ended; PP= Push Pull

DEVICE	POUT	TEST FREQ MHZ	GAIN Db	Min. GM MHO	No. Dice	Confi-gura-tion	Typical values pf COSS	CRSS	CISS	(Prefer high) RATIO GM/ CRSS	GM/ COSS	(Prefer low) RATIO CRSS/ COSS	IDSAT AMPS
PHI LF DIE SERIES										$x10^{-2}$	$x10^{-2}$	$x10^{-2}$	
LF2802A	2.0	1000	10	0.04	1	SE	**2.0**	0.6	3.0	6.67	2.00	30.00	
LF2805A	5.0	1000	10	0.08	2	SE	4.0	1.2	6.0	"	"	"	
LF2810A	10.0	1000	10	0.16	4	SE	8.0	2.4	12.0	"	"	"	
POLYFET F2 DIE SERIES													
F2001	2.5	1000	10	0.20	1	SE	**6.0**	1.0	9.0	20.00	3.33	16.67	1.4
F2002	5.0	1000	10	0.40	2	SE	12.0	2.0	18.0	"	"	"	2.8
F2021	7.5	1000	10	0.60	3	SE	18.0	3.0	27.0	"	"	"	4.2
F2012	10.0	1000	10	0.80	4	SE	24.0	4.0	36.0	"	"	"	5.6
PHI LOW PWR UF DIE SERIES -- APPEARS TO BE LF SERIES DIE BUT LOWER RF PERFORMANCE													
UF2805B	5.0	500	10	0.08	2	SE	4.0	1.2	6.0	6.67	2.00	30.00	
UF2810P	10.0	500	10	0.08	2+2	PP	4.0	1.2	6.0	"	"	"	1.0
UF2815B	15.0	500	10	0.24	6	SE	12.0	3.6	18.0	"	"	"	
PHI OLDER UF DIE SERIES													
DU2820S	20.0	175	13	0.50	1	SE	**30.0**	8.0	30.0	6.25	1.67	26.67	
DU2840S	40.0	175	13	1.00	2	SE	60.0	16.0	60.0	"	"	"	
DU2860T	60.0	175	13	1.50	3	SE	90.0	24.0	90.0	"	"	"	
PHI NEW UF DIE SERIES													
UF2820R	20.0	500	10	0.60	1	SE	**25.0**	8.0	35.0	7.50	2.40	32.00	
UF2840P	40.0	500	10	0.60	1+1	PP	25.0	8.0	35.0	"	"	"	5.0
UF28100M	100.0	500	10	1.80	3+3	PP	75.0	24.0	105.0	"	"	"	
UF28150J	150.0	500	8	2.40	4+4	PP	100.0	32.0	140.0	"	"	"	
POLYFET F1B DIE SERIES													
F1069	20.0	400	10	0.80	1	SE	**20.0**	4.0	30.0	20.00	4.00	20.00	5.0
F1058	30.0	400	13	0.80	1+1	SE	20.0	4.0	30.0	"	"	"	5.0
F1008	40.0	400	13	1.60	2+2	PP	40.0	8.0	60.0	"	"	"	10.0
F1072	100.0	400	10	2.40	3+3	PP	60.0	12.0	90.0	"	"	"	15.0
F1015	100.0	400	12	3.20	4+4	PP	80.0	16.0	120.0	"	"	"	20.0
PHILLIPS 500Mhz DIE SERIES													
BLF543	10.0	500	12	0.30	1	SE	**12.0**	3.2	16.0	9.38	2.50	26.67	2.4
BLF544	20.0	500	11	0.60	2	SE	24.0	6.4	32.0	"	"	"	4.8
BLF545	40.0	500	11	0.60	2+2	PP	24.0	6.4	32.0	"	"	"	4.8
BLF546	80.0	500	11	1.20	4+4	PP	48.0	12.8	64.0	"	"	"	10.0
BLF548	150.0	500	10	2.40	8+8	PP	96.0	25.6	128.0	"	"	"	20.0
ACRIAN ISOFET DIE SERIES													
VMIL20FT	20.0	175	13	0.35	1	SE	**40.0**	2.0	30.0	17.50	0.88	5.00	
VMIL40FT	40.0	175	13	0.70	2	SE	80.0	4.0	60.0	"	"	"	
VMIL120FT	120.0	175	13	2.10	6	SE	240.0	12.0	180.0	"	"	"	
MOTOROLA DIE SERIES													
MRF175LU	100.0	400	10	3.00	?	SE	200.0	20.0	180.0	15.00	1.50	10.00	
MRF175GU	150.0	400	12	3.00	?	PP	200.0	20.0	180.0	"	"	"	
PHILLIPS LOW FREQ DIE SERIES													
BLF242	5.0	175	13	0.15	1	SE	**10.0**	1.0	15.0	15.00	1.50	10.00	1.2
BLF244	15.0	175	13	0.60	4	SE	40.0	4.0	60.0	"	"	"	5.0
BLF245	30.0	175	13	1.20	8	SE	80.0	8.0	120.0	"	"	"	10.07

<u>Additional Reading</u>

1. U.S. Patent 4,561,168. "Method of Making Shadow Isolated Metal DMOS FET Devices. Inventors D. Pitzer & J. Rice. Assignee: Siliconix. Dec 31 1985

2. U.S. Patent 4,866,492. "Low Loss Fet". Inventor: Fred. Quigg. Assignee: Polyfet RF Devices. Sep 30 1988.

3. U.S. Patent 4,877,749. "Method of Forming Low Loss Fet". Inventor: Fred. Quigg. Assignee: Polyfet RF Devices. Sep 30 1988.

4. "Double Diffused MOS transistor achieves microwave Gain." T Gauge et el. Electronics Feb. 15 1971.

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7. "HF Power Amplifier Design Using VMOS Power FETs". L. Leighton, RF Design, Vol 3, No 1, Jan. 1980; pg. 32-37.

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