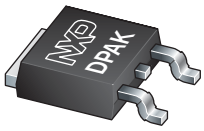



# BUJ105AD

## Silicon diffused power transistor

Rev. 2 — 3 November 2011 Product data sheet

## 1. Product profile

### 1.1 General description

High-voltage, high-speed planar-passivated NPN power switching transistor in a SOT428 (D-PAK) surface mounted package.

### 1.2 Features and benefits

- Low thermal resistance
- Fast switching

### 1.3 Applications

- Electronic lighting ballast
- Inverters
- DC-to-DC converters
- Motor control systems

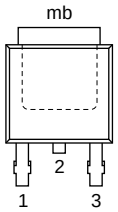
### 1.4 Quick reference data

- $V_{CESM} \leq 700$ V
- $P_{tot} \leq 80$ W
- $I_C \leq 8$ A
- $h_{FEsat} = 11$ (typ)

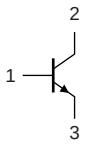
## 2. Pinning information

**Table 1. Pinning**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1 | base | | |
| 2 | collector [1] | | |
| 3 | emitter | | |
| mb | mounting base; connected to collector | | |




SOT428 (D-PAK)




sym056

[1] It is not possible to make a connection to pin 2 of the SOT428 (D-PAK) package.

## 3. Ordering information

**Table 2. Ordering information**

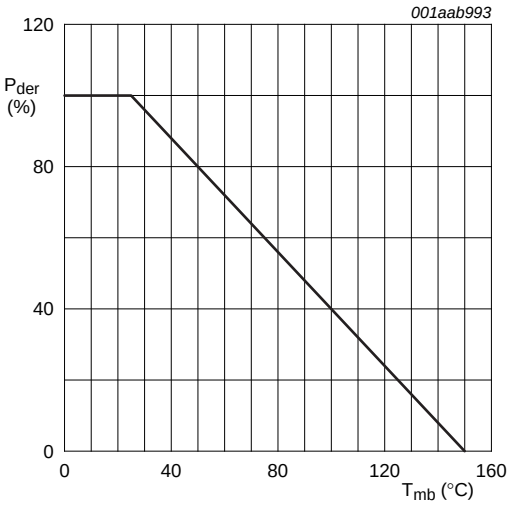
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BUJ105AD | D-PAK | plastic single-ended surface mounted package; 3 leads (one lead cropped) | SOT428 |

## 4. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CESM}$ | peak collector-emitter voltage | $V_{BE}$ = 0 V | - | 700 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | - | 400 | V |
| $V_{CBO}$ | collector-base voltage | open emitter | - | 700 | V |
| $I_C$ | collector current (DC) | | - | 8 | A |
| $I_{CM}$ | peak collector current | | - | 16 | A |
| $I_B$ | base current (DC) | | - | 4 | A |
| $I_{BM}$ | peak base current | | - | 8 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = ≤ 25 °C; see Figure 1 | - | 80 | W |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_j$ | junction temperature | | - | 150 | °C |




$$P_{der}(\%) = \frac{P_{tot}}{P_{tot(25\ °C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature**

## 5. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | see Figure 2 | | - | - | 1.56 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | | [1] | - | 75 | - | K/W |

[1] Device mounted on a printed-circuit board; minimum footprint

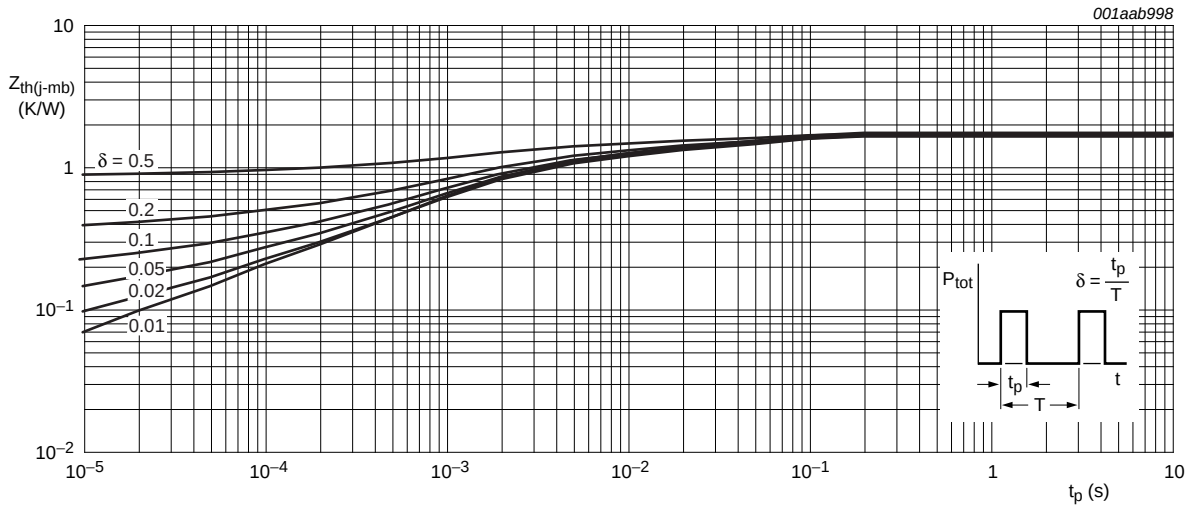



**Fig 2. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

**Table 5. Characteristics**

*$T_{mb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{CES}$ | collector-emitter cut-off current | $V_{BE}$ = 0 V; $V_{CE}$ = $V_{CESMmax}$ | [1] | - | - | 0.2 | mA |
| | | $V_{BE}$ = 0 V; $V_{CE}$ = $V_{CESMmax}$; $T_j$ = 125 °C | [1] | - | - | 0.5 | mA |
| $I_{CBO}$ | collector-base cut-off current | $V_{BE}$ = 0 V; $V_{CE}$ = $V_{CESMmax}$ | [1] | - | - | 0.2 | mA |
| $I_{CEO}$ | collector-emitter cut-off current | $V_{CEO}$ = $V_{CEOMmax}$ = 400 V | [1] | - | - | 0.1 | mA |
| $I_{EBO}$ | emitter-base cut-off current | $V_{EB}$ = 9 V; $I_C$ = 0 A | | - | - | 1 | mA |
| $V_{CEOsus}$ | collector-emitter sustaining voltage | $I_B$ = 0 A; $I_C$ = 10 mA; L = 25 mH; see Figure 3 and 4 | | 400 | - | - | V |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = 4.0 A; $I_B$ = 0.8 A; see Figure 11 | | - | 0.3 | 1.0 | V |
| $V_{BEsat}$ | base-emitter saturation voltage | $I_C$ = 4.0 A; $I_B$ = 0.8 A; see Figure 12 | | - | 1.0 | 1.5 | V |
| $h_{FE}$ | DC current gain | $I_C$ = 1 mA; $V_{CE}$ = 5 V | | 10 | 14 | 34 | |
| | | $I_C$ = 500 mA; $V_{CE}$ = 5 V; see Figure 10 | | 13 | 23 | 36 | |
| $h_{FEsat}$ | DC saturation current gain | $I_C$ = 4.0 A; $V_{CE}$ = 5 V | | 8 | 11 | 15 | |

**Table 5. Characteristics** *...continued*

*$T_{mb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Dynamic characteristics** | | | | | | |
| Switching times (resistive load); see Figure 5 and 6 | | | | | | |
| $t_{on}$ | turn-on time | $I_{Con}$ = 5 A; $I_{Bon}$ = −$I_{Boff}$ = 1 A; $R_L$ = 75 Ω | - | 0.65 | 1 | µs |
| $t_{stg}$ | storage time | | - | 1.8 | 2.5 | µs |
| $t_f$ | fall time | | - | 0.3 | 0.5 | µs |
| Switching times (inductive load); see Figure 7 and 8 | | | | | | |
| $t_{stg}$ | storage time | $I_{Con}$ = 5 A; $I_{Bon}$ = 1 A; $L_B$ = 1 µH; $V_{BB}$ = −5 V | - | 1.2 | 1.7 | µs |
| $t_f$ | fall time | | - | 20 | 50 | ns |
| Switching times (inductive load); see Figure 7 and 8 | | | | | | |
| $t_{stg}$ | storage time | $I_{Con}$ = 5 A; $I_{Bon}$ = 1 A; $L_B$ = 1 µH; $V_{BB}$ = −5 V; $T_j$ = 100 °C | - | 1.4 | 1.9 | µs |
| $t_f$ | fall time | | - | 25 | 100 | ns |

[1] Measured with half sine-wave voltage (curve tracer).

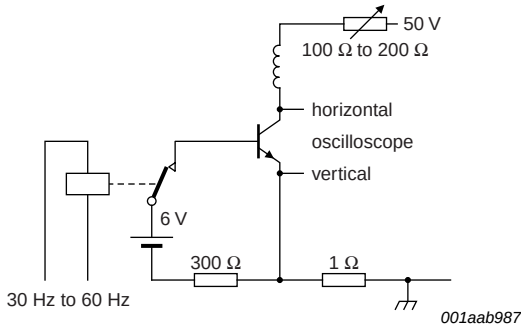



**Fig 3. Test circuit for collector-emitter sustaining voltage**

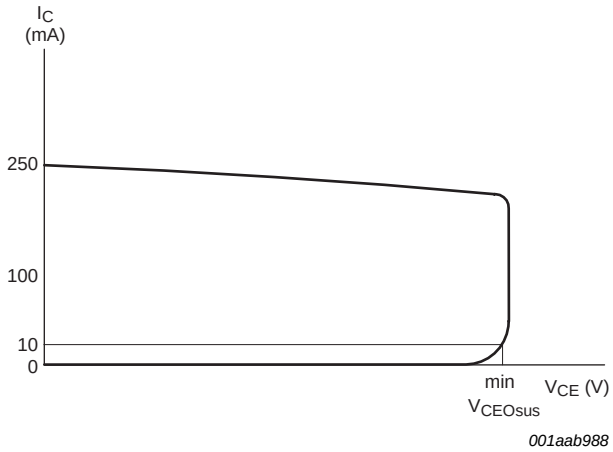
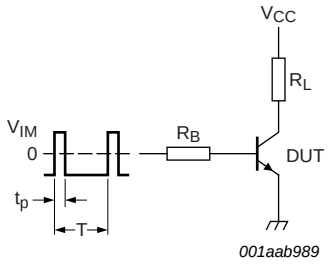



**Fig 4. Oscilloscope display for collector-emitter sustaining voltage test waveform**




$V_{IM}$ = −6 V to +8 V; $V_{CC}$ = 250 V; $t_p$ = 20 μs;
$\delta = t_p/T = 0.01$.

$R_B$ and $R_L$ calculated from $I_{Con}$ and $I_{Bon}$ requirements.

**Fig 5. Test circuit for resistive load switching**

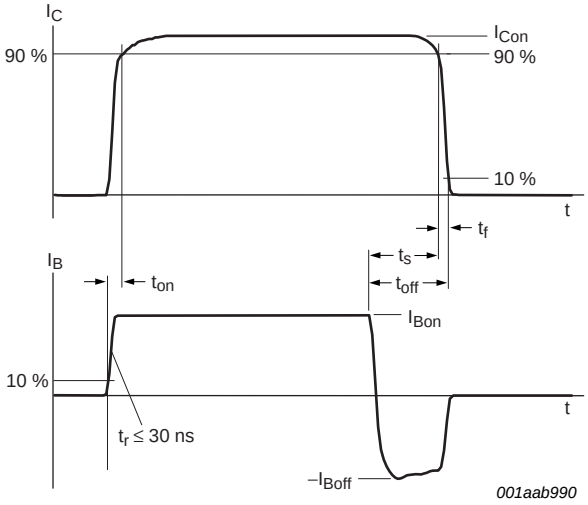
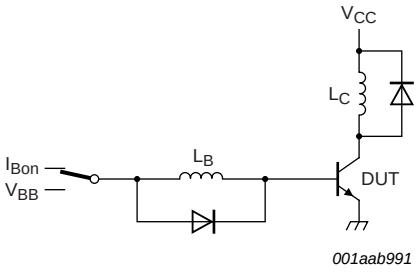



**Fig 6. Switching times waveforms for resistive load**




$V_{CC}$ = 300 V; $V_{BB}$ = −5 V; $L_C$ = 200 μH; $L_B$ = 1 μH.

**Fig 7. Test circuit for inductive load switching**

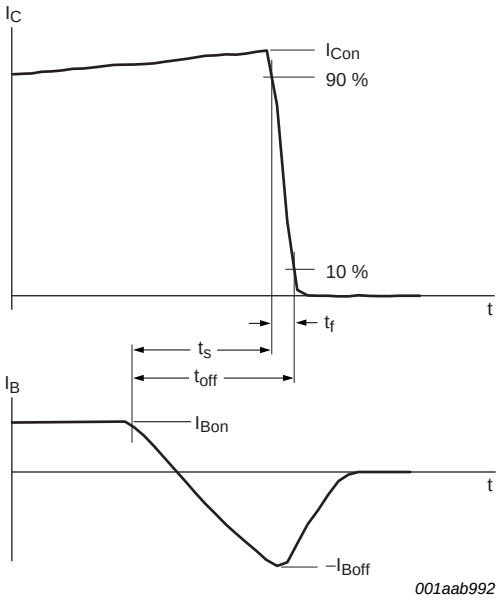



**Fig 8. Switching times waveforms for inductive load**

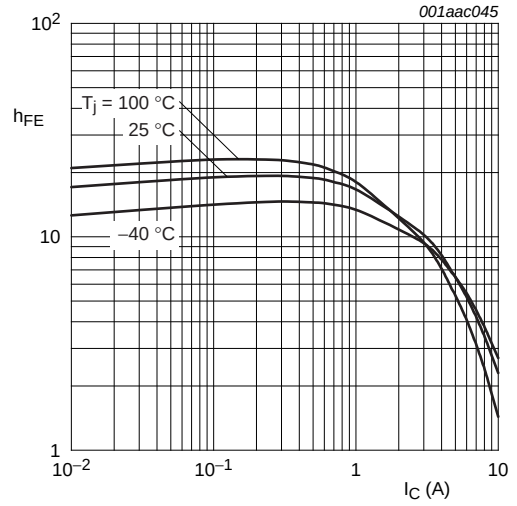



**Fig 9. DC current gain as a function of collector current; typical values at $V_{CE}$ = 1 V**

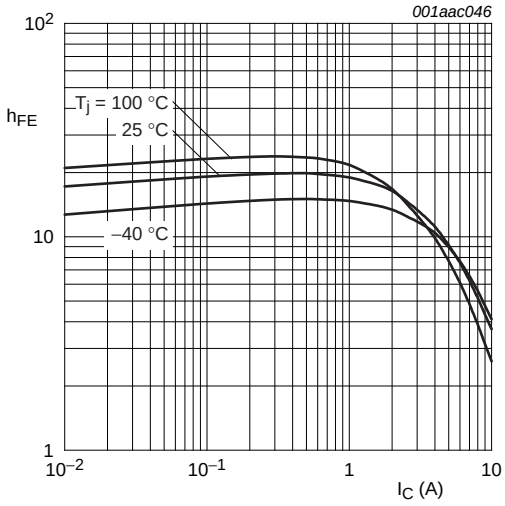
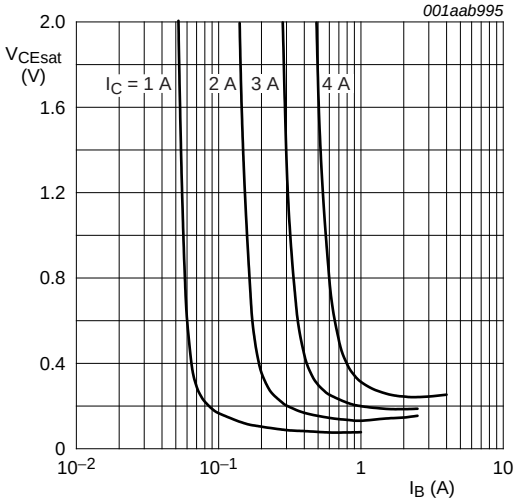
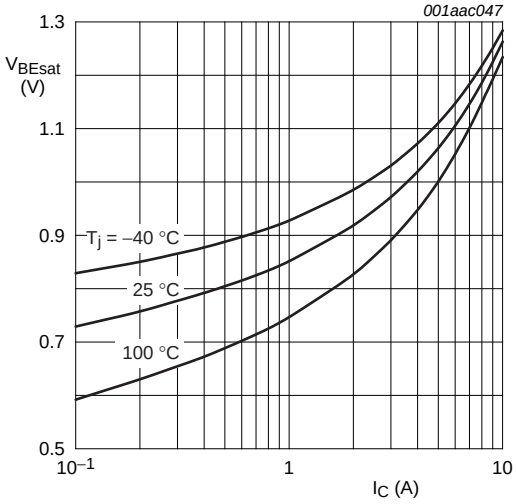



**Fig 10. DC current gain as a function of collector current; typical values at $V_{CE}$ = 5 V**



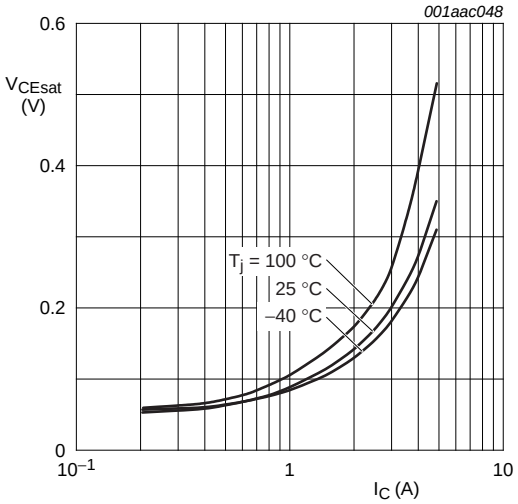

$T_j$ = 25 °C.

**Fig 11. Collector-emitter saturation voltage as a function of base current; typical values**



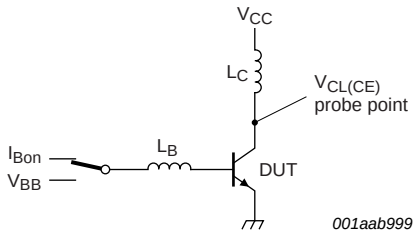

$I_C/I_B$ = 4.

**Fig 12. Base-emitter saturation voltage as a function of collector current; typical values**



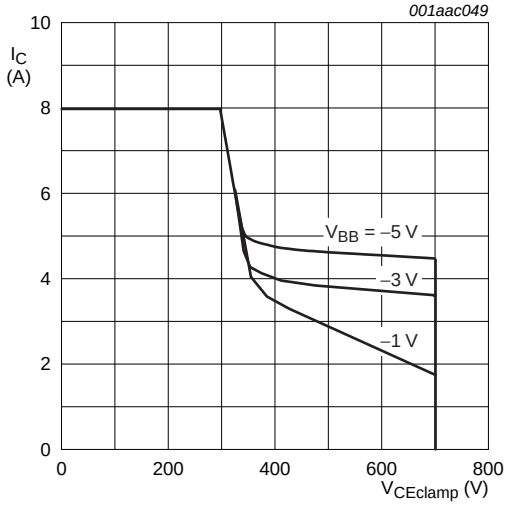

$I_C/I_B = 4$.

**Fig 13. Collector-emitter saturation voltage as a function of collector current; typical values**




$V_{CEclamp}$ < 700 V; $V_{CC}$ = 150 V; $V_{BB}$ = –5 V, –3 V and –1 V; $L_B$ = 1 μH; $L_C$ = 200 μH.

**Fig 14. Test circuit for reverse bias safe operating area**




$T_j < T_{j(max)}$.

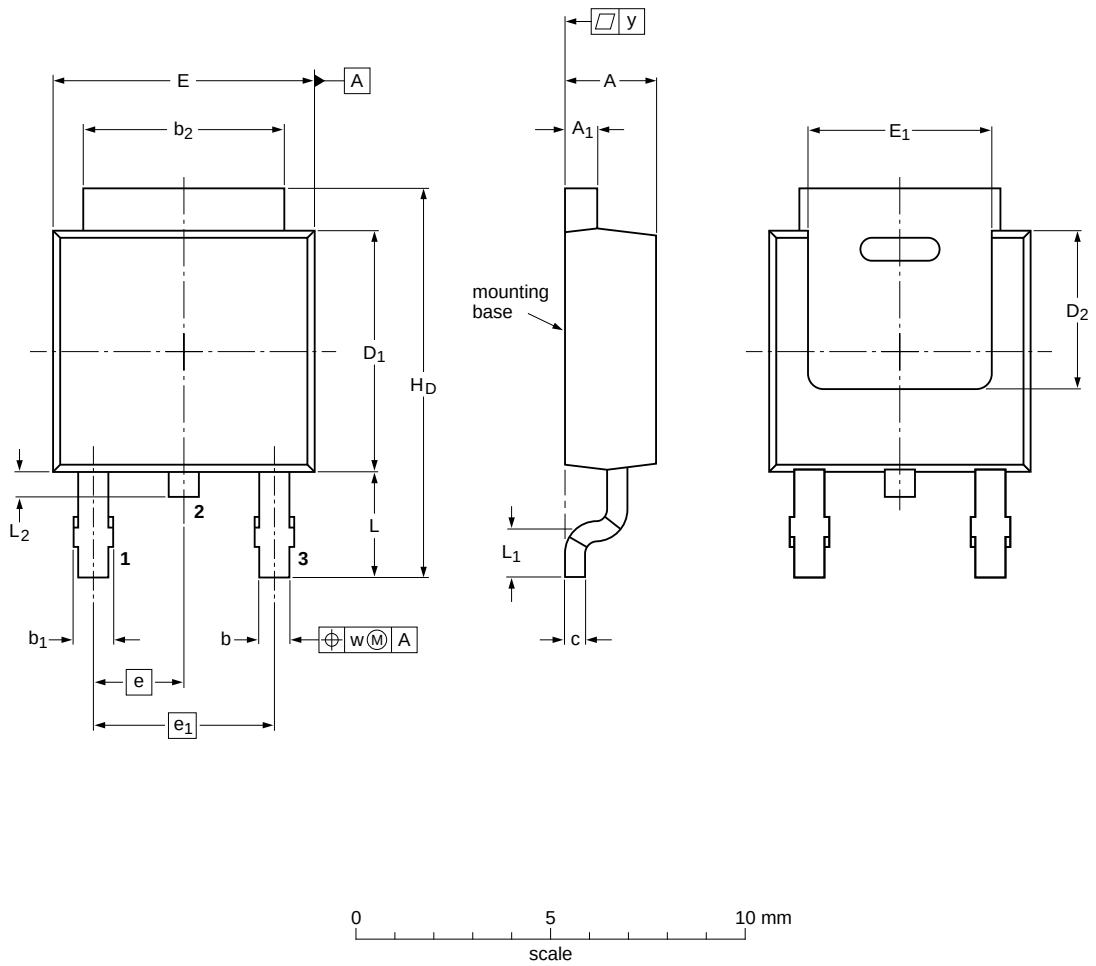
**Fig 15. Reverse bias safe operating area**

## 7. Package information

Epoxy meets requirements of UL94 V-0 at 1/8 inch.

## 8. Package outline

**Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)** **SOT428**



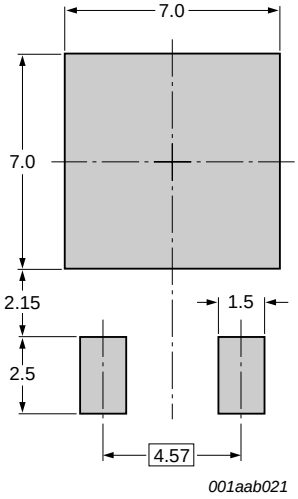

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | $b_2$ | c | $D_1$ | $D_2$ min | E | $E_1$ min | e | $e_1$ | $H_D$ | L | $L_1$ min | $L_2$ | w | y max |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.38<br>2.22 | 0.93<br>0.46 | 0.89<br>0.71 | 1.1<br>0.9 | 5.46<br>5.00 | 0.56<br>0.20 | 6.22<br>5.98 | 4.0 | 6.73<br>6.47 | 4.45 | 2.285 | 4.57 | 10.4<br>9.6 | 2.95<br>2.55 | 0.5 | 0.9<br>0.5 | 0.2 | 0.2 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT428 | | TO-252 | SC-63 | | | ~~06-02-14~~<br>06-03-16 |

**Fig 16. Package outline SOT428 (SC-63)**

## 9. Mounting




Dimensions in mm.

**Fig 17. SOT428 soldering pattern for surface mounting**

## 10. Revision history

**Table 6. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BUJ105AD v.2 | 20111103 | Product data sheet | - | BUJ105AD v.1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| BUJ105AD v.1 | 20041214 | Product data sheet | - | - |

# 11. Legal information

## 11.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 13. Contents





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**Date of release: 3 November 2011**
**Document identifier: BUJ105AD**