## N-Channel Enhancement-Mode Vertical DMOS FETs

## Ordering Information

| $\mathrm{BV}_{\mathrm{DSS}} /$ |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{BV}_{\mathrm{DGS}}$ |

## Features

- Low threshold - 2.0V max.
- High input impedance
- Low input capacitance - 50pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N - and P-channel devices


## Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.
Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Package Option



## Thermal Characteristics

| Package | $\mathbf{I}_{\mathrm{D}}$ (continuous) $^{*}$ | $\mathrm{I}_{\mathrm{D}}$ (pulsed) | Power Dissipation <br> $@ \mathbf{T}_{\mathbf{C}}=\mathbf{2 5} \mathbf{C}$ | $\theta_{\mathrm{jc}}$ <br> ${ }^{\circ} \mathbf{C} / \mathbf{W}$ | $\theta_{\mathrm{ja}}$ <br> ${ }^{\circ} \mathbf{C} / \mathbf{W}$ | $\mathrm{I}_{\mathrm{DR}}{ }^{*}$ | $\mathbf{I}_{\mathrm{DRM}}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{TO}-92$ | 350 mA | 2.0 A | 1.0 W | 125 | 170 | 350 mA | 2.0 A |

${ }^{*} I_{D}$ (continuous) is limited by max rated $T_{j}$.

## Electrical Characteristics (@ $25^{\circ} \mathrm{C}$ unless otherwise specified)

| Symbol | Parameter |  | Min | Typ | Max | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $B V_{\text {DSS }}$ | Drain-to-Source Breakdown Voltage | TN0110 | 100 |  |  | V | $\mathrm{I}_{\mathrm{D}}=1 \mathrm{~mA}, \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V}$ |
|  |  | TN0106 | 60 |  |  |  |  |
| $\mathrm{V}_{\mathrm{GS} \text { (th) }}$ | Gate Threshold Voltage |  | 0.6 |  | 2.0 | V | $\mathrm{V}_{\mathrm{GS}}=\mathrm{V}_{\mathrm{DS}}, \mathrm{I}_{\mathrm{D}}=0.5 \mathrm{~mA}$ |
| $\Delta \mathrm{V}_{\text {GS(th) }}$ | Change in $\mathrm{V}_{\mathrm{GS} \text { (th) }}$ with Temperature |  |  | -3.2 | -5.0 | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ | $\mathrm{V}_{\mathrm{GS}}=\mathrm{V}_{\mathrm{DS}}, \mathrm{I}_{\mathrm{D}}=1.0 \mathrm{~mA}$ |
| $\mathrm{I}_{\text {GSS }}$ | Gate Body Leakage |  |  |  | 100 | nA | $\mathrm{V}_{\mathrm{GS}}= \pm 20 \mathrm{~V}, \mathrm{~V}_{\mathrm{DS}}=0 \mathrm{~V}$ |
| $\mathrm{I}_{\text {DSS }}$ | Zero Gate Voltage Drain Current |  |  |  | 10 | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{DS}}=$ Max Rating |
|  |  |  |  |  | 500 |  | $\begin{aligned} & \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{DS}}=0.8 \text { Max Rating } \\ & \mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C} \end{aligned}$ |
| $\mathrm{I}_{\mathrm{D} \text { (ON) }}$ | ON-State Drain Current |  | 0.75 | 1.4 |  | A | $\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{DS}}=25 \mathrm{~V}$ |
|  |  |  | 2.0 | 3.4 |  |  | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}, \mathrm{~V}_{\mathrm{DS}}=25 \mathrm{~V}$ |
| $\mathrm{R}_{\mathrm{DS} \text { (ON) }}$ | Static Drain-to-Source ON-State Resistance |  |  | 2.0 | 4.5 | $\Omega$ | $\mathrm{V}_{\mathrm{GS}}=4.5 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=250 \mathrm{~mA}$ |
|  |  |  |  | 1.6 | 3.0 |  | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=500 \mathrm{~mA}$ |
| $\Delta \mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ | Change in $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ with Temperature |  |  | 0.6 | 1.1 | \%/ ${ }^{\circ} \mathrm{C}$ | $\mathrm{I}_{\mathrm{D}}=0.5 \mathrm{~A}, \mathrm{~V}_{\mathrm{GS}}=10 \mathrm{~V}$ |
| $\mathrm{G}_{\mathrm{FS}}$ | Forward Transconductance |  | 225 | 400 |  | mซ | $\mathrm{V}_{\mathrm{DS}}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=500 \mathrm{~mA}$ |
| $\mathrm{C}_{\text {ISS }}$ | Input Capacitance |  |  | 50 | 60 | pF | $\begin{aligned} & V_{G S}=0 V, V_{D S}=25 V \\ & f=1 \mathrm{MHz} \end{aligned}$ |
| $\mathrm{C}_{\text {OSS }}$ | Common Source Output Capacitance |  |  | 25 | 35 |  |  |
| $\mathrm{C}_{\mathrm{RSS}}$ | Reverse Transfer Capacitance |  |  | 4.0 | 8.0 |  |  |
| $\mathrm{t}_{\mathrm{d}(\mathrm{ON})}$ | Turn-ON Delay Time |  |  | 2.0 | 5.0 | ns | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=25 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{D}}=1.0 \mathrm{~A} \\ & \mathrm{R}_{\mathrm{GEN}}=25 \Omega \end{aligned}$ |
| $\mathrm{t}_{\mathrm{r}}$ | Rise Time |  |  | 3.0 | 5.0 |  |  |
| $\mathrm{t}_{\mathrm{d} \text { (OFF) }}$ | Turn-OFF Delay Time |  |  | 6.0 | 7.0 |  |  |
| $\mathrm{t}_{\mathrm{f}}$ | Fall Time |  |  | 3.0 | 6.0 |  |  |
| $\mathrm{V}_{\text {SD }}$ | Diode Forward Voltage Drop |  |  | 1.0 | 1.5 | V | $\mathrm{I}_{\mathrm{SD}}=0.5 \mathrm{~A}, \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V}$ |
| $\mathrm{t}_{\mathrm{rr}}$ | Reverse Recovery Time |  |  | 400 |  | ns | $\mathrm{I}_{\mathrm{SD}}=0.5 \mathrm{~A}, \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V}$ |

Notes:

1. All D.C. parameters $100 \%$ tested at $25^{\circ} \mathrm{C}$ unless otherwise stated. (Pulse test: $300 \mu \mathrm{~s}$ pulse, $2 \%$ duty cycle.)
2. All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit



PULSE GENERATOR



## Typical Performance Curves

Output Characteristics


Transconductance vs. Drain Current


Maximum Rated Safe Operating Area


Saturation Characteristics


Power Dissipation vs. Case Temperature


Thermal Response Characteristics


## Typical Performance Curves



