



N-Channel Depletion-Mode Vertical DMOS FETs

Ordering Information

BV _{DSX} / BV _{DGX}	R _{DS(ON)} (max)	I _{DSS} (min)	Order Number / Package		
			TO-92	TO-220	TO-243AA*
350V	25	150mA	DN2535N3	DN2535N5	—
400V	25	150mA	DN2540N3	DN2540N5	DN2540N8

* Same as SOT-89. Product shipped on 2000 piece carrier tape reels.

Features

- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Normally-on switches
- Solid state relays
- Converters
- Linear amplifiers
- Constant current sources
- Power supply circuits
- Telecom

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSX}
Drain-to-Gate Voltage	BV _{DGX}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Product marking for TO-243AA:

DN5D

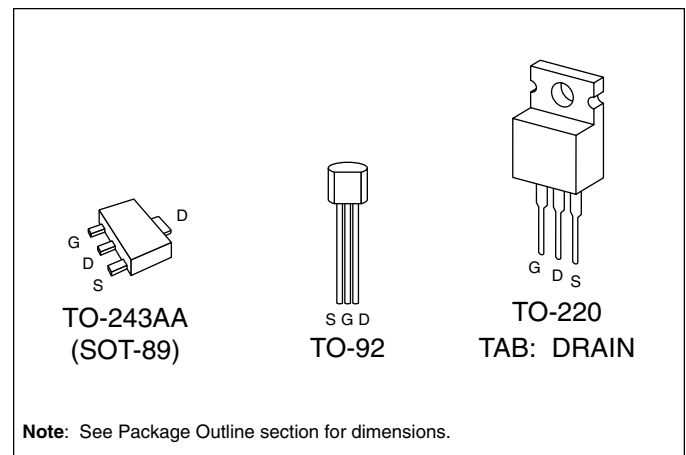
Where = 2-week alpha date code

Advanced DMOS Technology

These low threshold depletion-mode (normally-on) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Thermal Characteristics

Package	I _D (continuous)*	I _D (pulsed)	Power Dissipation @ T _C = 25°C	θ _{JC} °C/W	θ _{JA} °C/W	I _{DR} *	I _{DRM}
TO-92	120mA	500mA	1.0W	125	170	120mA	500mA
TO-220	500mA	500mA	15.0W	8.3	70	500mA	500mA
TO-243AA	170mA	500mA	1.6W (T _A = 25°) [†]	15	78 [†]	170mA	500mA

* I_D (continuous) is limited by max rated T_J.

[†] Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate. T_A = 25°C

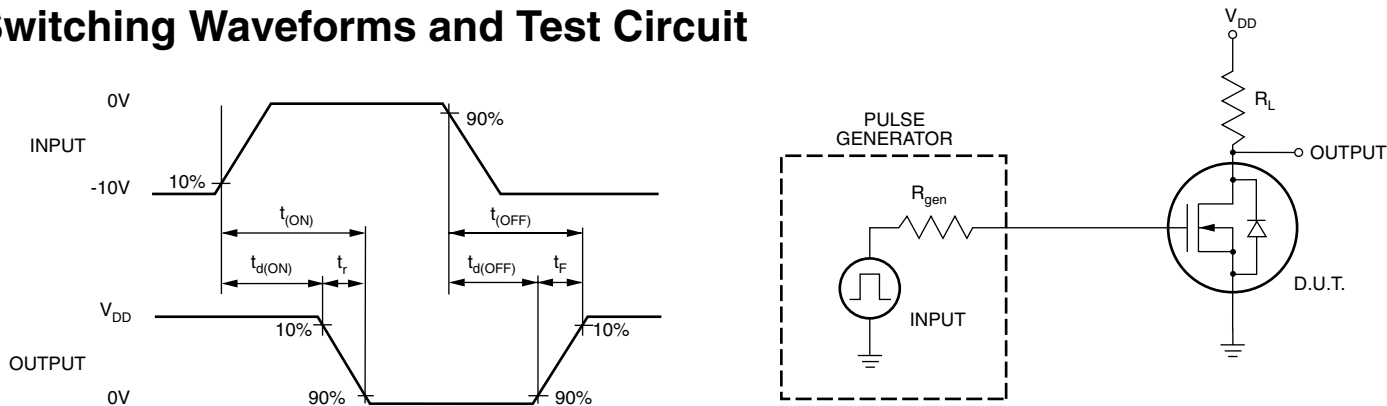
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV _{DSX}	Drain-to-Source Breakdown Voltage	DN2540	400			V _{GS} = -5V, I _D = 100µA
		DN2535	350			
V _{GS(OFF)}	Gate-to-Source OFF Voltage	-1.5		-3.5	V	V _{DS} = 25V, I _D = 10µA
ΔV _{GS(OFF)}	Change in V _{GS(OFF)} with Temperature			4.5	mV/°C	V _{DS} = 25V, I _D = 10µA
I _{GSS}	Gate Body Leakage Current			100	nA	V _{GS} = ± 20V, V _{DS} = 0V
I _{D(OFF)}	Drain-to-Source Leakage Current			10	µA	V _{GS} = -10V, V _{DS} = Max Rating
				1	mA	V _{GS} = -10V, V _{DS} = 0.8 Max Rating T _A = 125°C
I _{DSS}	Saturated Drain-to-Source Current	150			mA	V _{GS} = 0V, V _{DS} = 25V
R _{DS(ON)}	Static Drain-to-Source ON-State Resistance		17	25	Ω	V _{GS} = 0V, I _D = 120mA
R _{DS(ON)}	Change in R _{DS(ON)} with Temperature			1.1	%/°C	V _{GS} = 0V, I _D = 120mA
G _{FS}	Forward Transconductance		325		mS	I _D = 100mA, V _{DS} = 10V
C _{ISS}	Input Capacitance		200	300	pF	V _{GS} = -10V, V _{DS} = 25V f = 1 MHz
C _{OSS}	Common Source Output Capacitance		12	30		
C _{RSS}	Reverse Transfer Capacitance		1	5		
t _{d(ON)}	Turn-ON Delay Time			10	ns	V _{DD} = 25V, I _D = 150mA, R _{GEN} = 25Ω
t _r	Rise Time			15		
t _{d(OFF)}	Turn-OFF Delay Time			15		
t _f	Fall Time			20		
V _{SD}	Diode Forward Voltage Drop			1.8	V	V _{GS} = -10V, I _{SD} = 120mA
t _{rr}	Reverse Recovery Time		800		ns	V _{GS} = -10V, I _{SD} = 1A

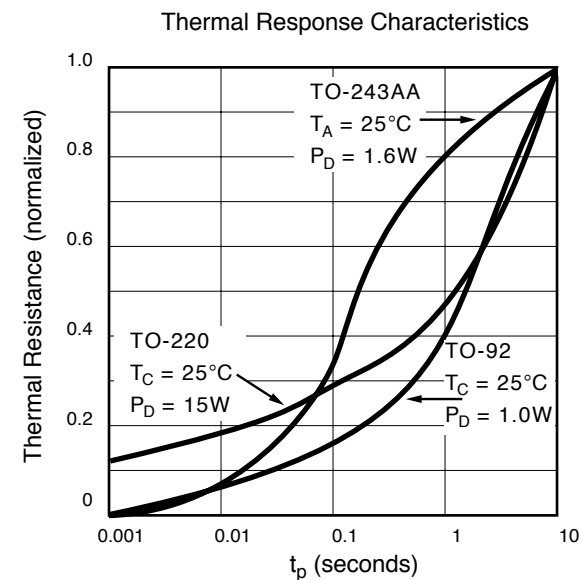
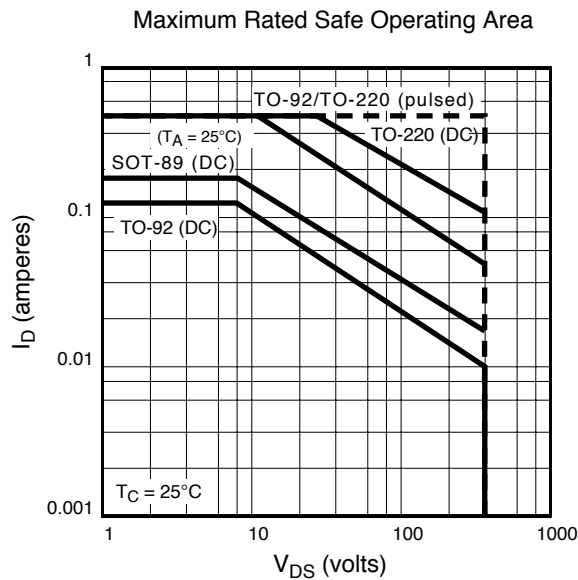
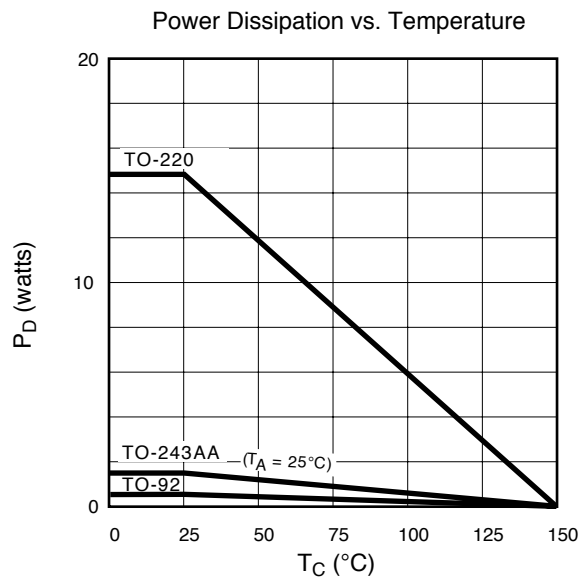
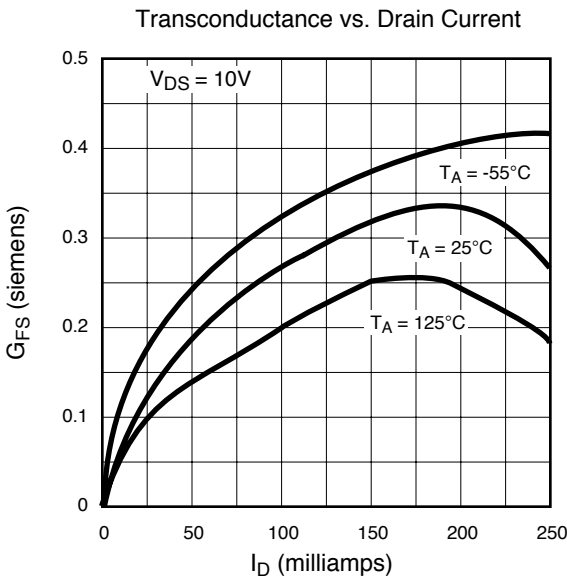
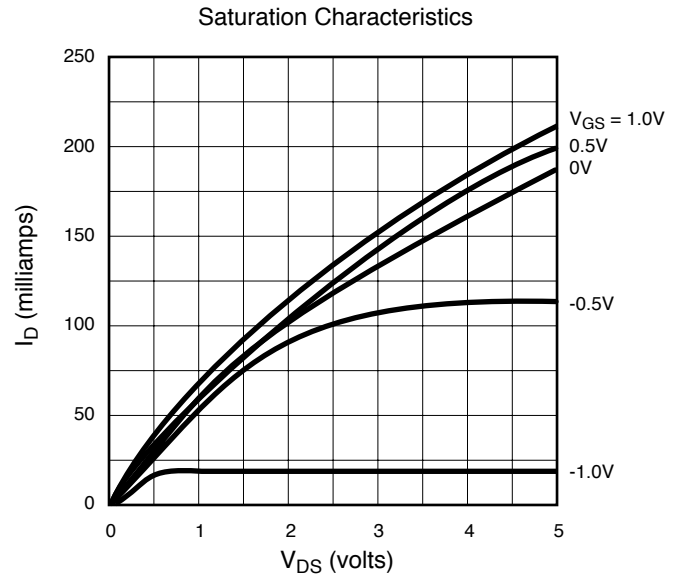
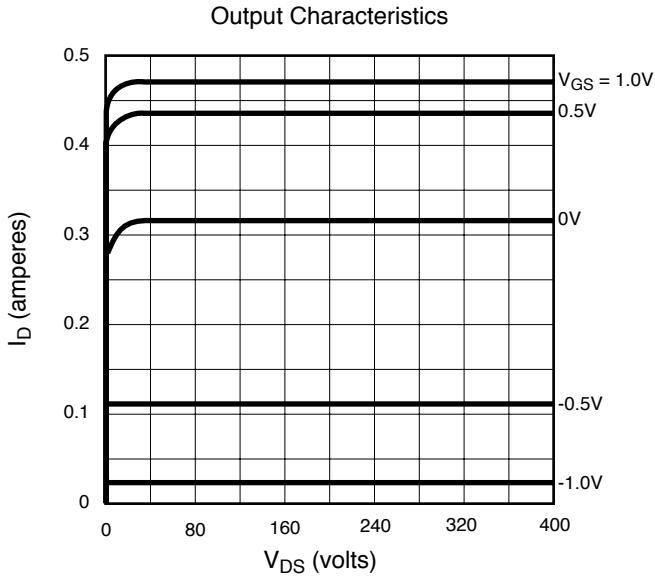
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Typical Performance Curves



Typical Performance Curves

