

Philips Components

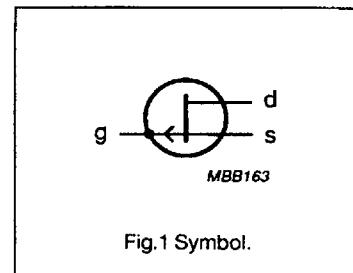
Data sheet	
status	Preliminary specification
date of issue	October 1990

2N5460/5461/5462**P-channel J-FETs****DESCRIPTION**

P-channel silicon junction field-effect transistor in a TO-92 plastic envelope. It is intended for use as an analog switch and an amplifier.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	drain
3	source

PIN CONFIGURATION

P-channel J-FETs

2N5460/5461/5462

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	40	V
V_{GS}	gate-source voltage		-	40	V
$-I_G$	gate current		-	10	mA
P_{tot}	total power dissipation	$T_{amb} \leq 40^\circ C$	-	310	mW
T_{stg}	storage temperature range		-65	150	$^\circ C$
T_j	junction temperature		-	150	$^\circ C$

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient	355	K/W

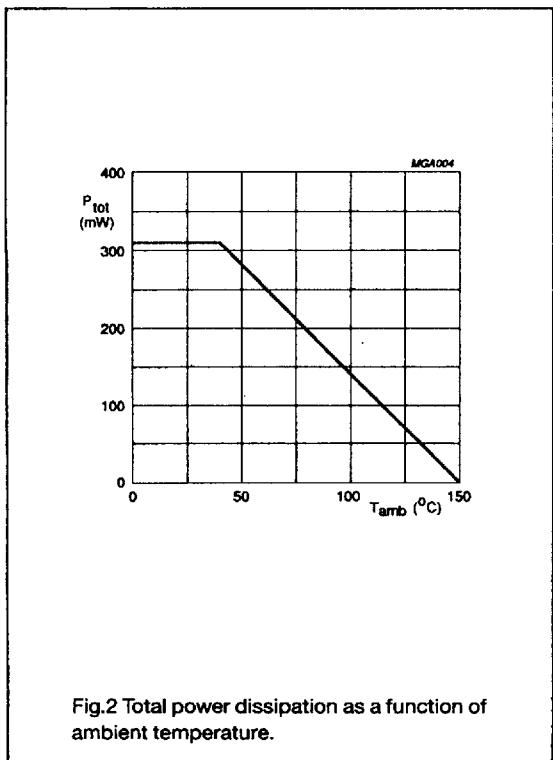


Fig.2 Total power dissipation as a function of ambient temperature.

P-channel J-FETs

2N5460/5461/5462

CHARACTERISTICS

 $T_{amb} = 25^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT	
I_{GSS}	gate-source leakage current	$V_{GS} = 20\text{ V}$ $V_{DS} = 0$	-	5	nA	
		$V_{GS} = 20\text{ V}$ $V_{DS} = 0$ $T_{amb} = 100^\circ\text{C}$	-	1	μA	
$-I_{DSS}$	drain-source leakage current	$-V_{DS} = 15\text{ V}$ $V_{GS} = 0$ 2N5460 2N5461 2N5462	1 2 4	5 9 16	mA mA mA	
V_{GS}	gate-source voltage	$-I_D = 0.1\text{ mA}$ $-V_{DS} = 15\text{ V}$	2N5460	0.5	4	V
V_{GS}	gate-source voltage	$-I_D = 0.2\text{ mA}$ $-V_{DS} = 15\text{ V}$	2N5461	0.8	4.5	V
V_{GS}	gate-source voltage	$-I_D = 0.4\text{ mA}$ $-V_{DS} = 15\text{ V}$	2N5462	1.5	6	V
$V_{P(GS)}$	gate-source cut-off voltage	$-I_D = 1\text{ }\mu\text{A}$ $-V_{DS} = 15\text{ V}$ 2N5460 2N5461 2N5462	0.75 1 1.8	6 7.5 9	V V V	
$ y_{fs} $	transfer admittance	$-V_{DS} = 15\text{ V}$ $V_{GS} = 0$ $f = 1\text{ kHz}$ 2N5460 2N5461 2N5462	1 1.5 2	4 5 6	mS mS mS	
$ y_{os} $	output admittance	$-V_{DS} = 15\text{ V}$ $V_{GS} = 0$ $f = 1\text{ kHz}$	-	75	μS	
C_{iss}	input capacitance	$-V_{DS} = 15\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$	-	7	pF	
C_{rss}	feedback capacitance	$-V_{DS} = 15\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$	-	2	pF	
NF	noise figure	$-V_{DS} = 15\text{ V}$ $V_{GS} = 0$ $f = 100\text{ Hz}$ $B = 1\text{ Hz}$	-	2.5	dB	

P-channel J-FETs

2N5460/5461/5462

PACKAGE OUTLINE

