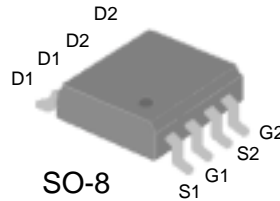


DUAL N-CHANNEL ENHANCEMENT-MODE POWER MOSFETS

Simple drive requirement
Lower gate charge
Fast switching characteristics

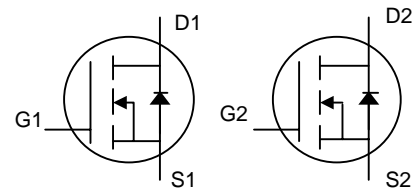


BV_{DSS} 40V
 $R_{DS(ON)}$ 20m Ω
 I_D 7.8A

Description

Advanced Power MOSFETs from Silicon Standard provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SSM9960M is in the SO-8 package, which is widely preferred for commercial and industrial surface mount applications, and is well suited for low voltage applications such as DC/DC converters.



 This device is available with Pb-free lead finish (second-level interconnect) as SSM9960GM.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current ³	7.8	A
$I_D @ T_A=100^\circ\text{C}$	Continuous Drain Current ³	6.2	A
I_{DM}	Pulsed Drain Current ¹	20	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	2	W
	Linear Derating Factor	0.016	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-a}	Thermal Resistance Junction-ambient ³	Max. 62.5	$^\circ\text{C}/\text{W}$

Electrical Characteristics @ $T_J=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	-	0.032	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=7A$	-	-	20	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=5A$	-	-	32	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=7A$	-	25	-	S
I_{DSS}	Drain-Source Leakage Current ($T_J=25^\circ\text{C}$)	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current ($T_J=70^\circ\text{C}$)	$V_{DS}=32V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=7A$	-	14.7	-	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=20V$	-	7.1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	6.8	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=20V$	-	11.5	-	ns
t_r	Rise Time	$I_D=1A$	-	6.3	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	28.2	-	ns
t_f	Fall Time	$R_D=20\Omega$	-	12.6	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1725	-	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	235	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	145	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	$V_D=V_G=0V, V_S=1.3V$	-	-	1.54	A
V_{SD}	Forward On Voltage ²	$T_J=25^\circ\text{C}, I_S=2.3A, V_{GS}=0V$	-	-	1.3	V

Notes:

- 1.Pulse width limited by max. junction temperature.
- 2.Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- 3.Surface mounted on 1 in² copper pad of FR4 board ; 135°C/W when mounted on min. copper pad.

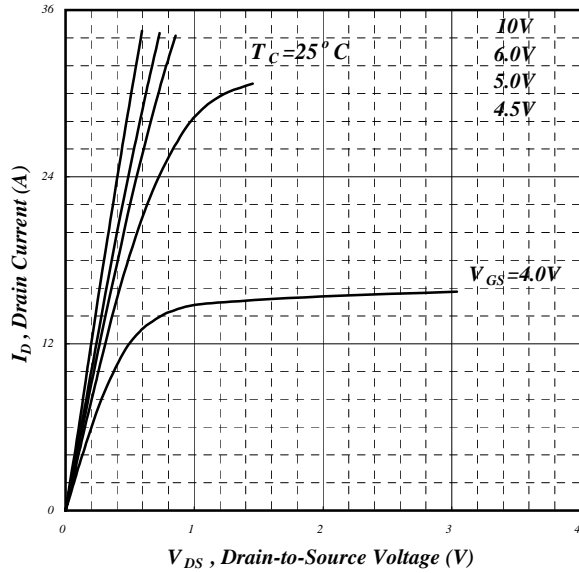


Fig 1. Typical Output Characteristics

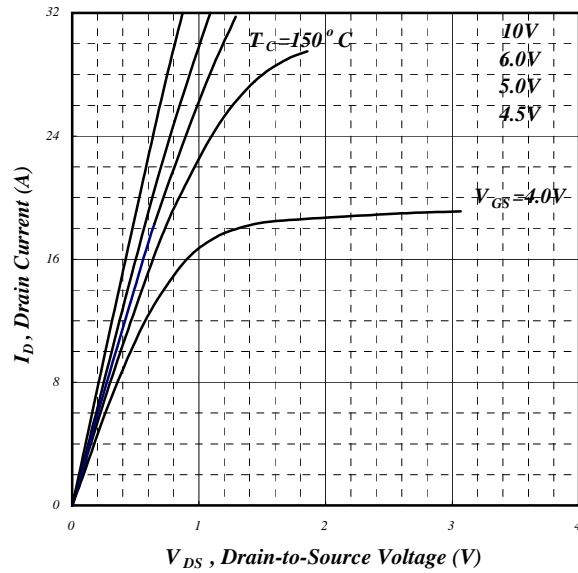


Fig 2. Typical Output Characteristics

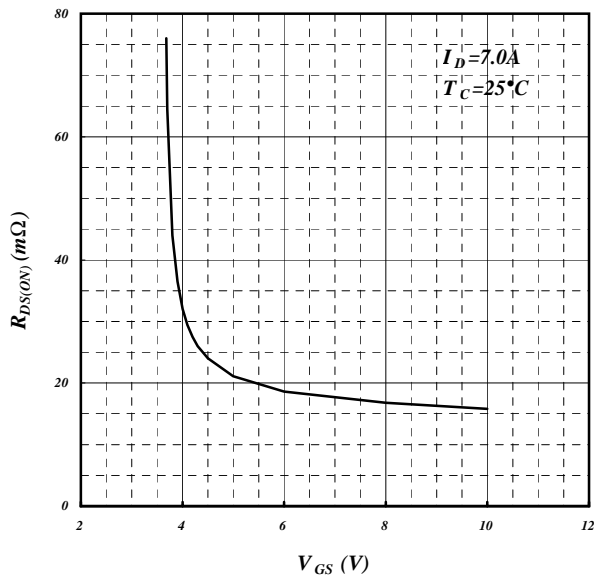


Fig 3. On-Resistance v.s. Gate Voltage

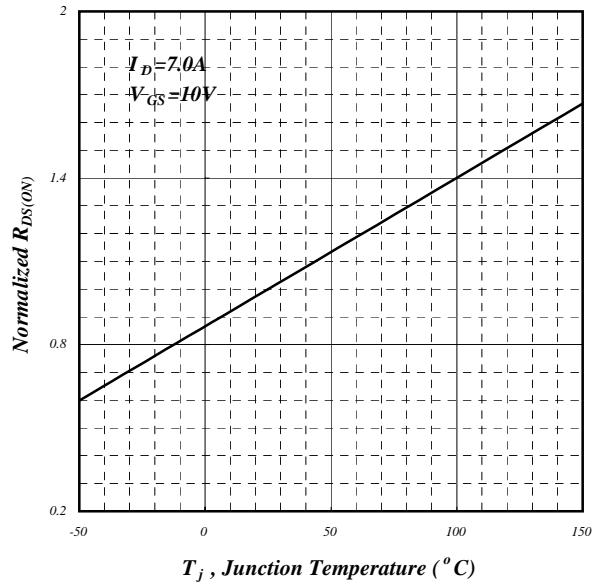


Fig 4. Normalized On-Resistance vs. Junction Temperature

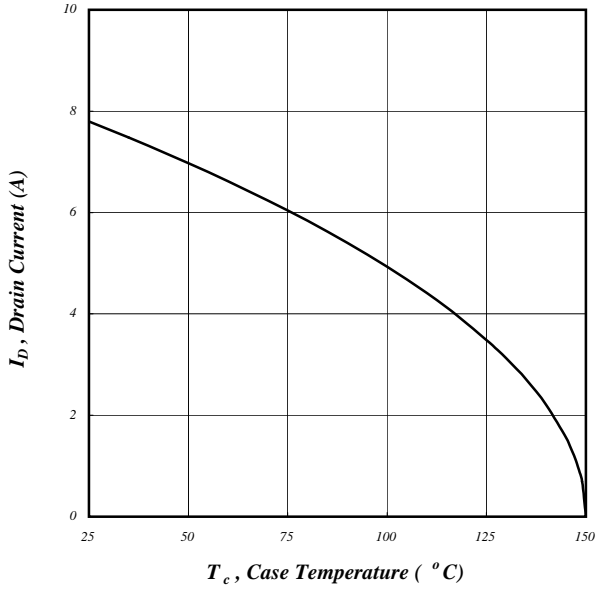


Fig 5. Maximum Drain Current vs. Case Temperature

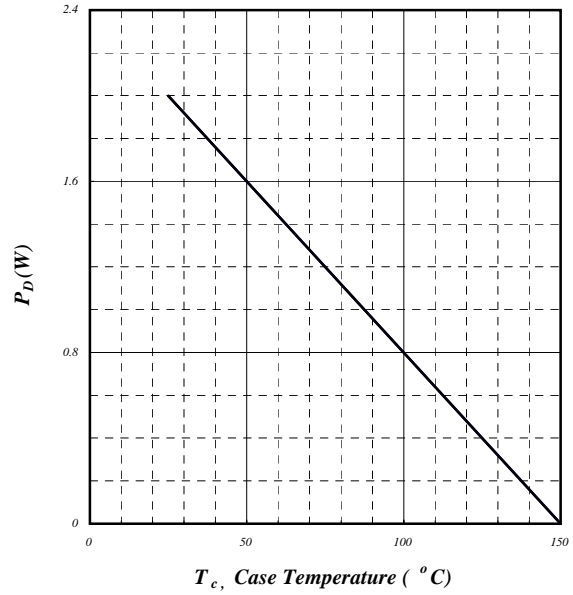


Fig 6. Typical Power Dissipation

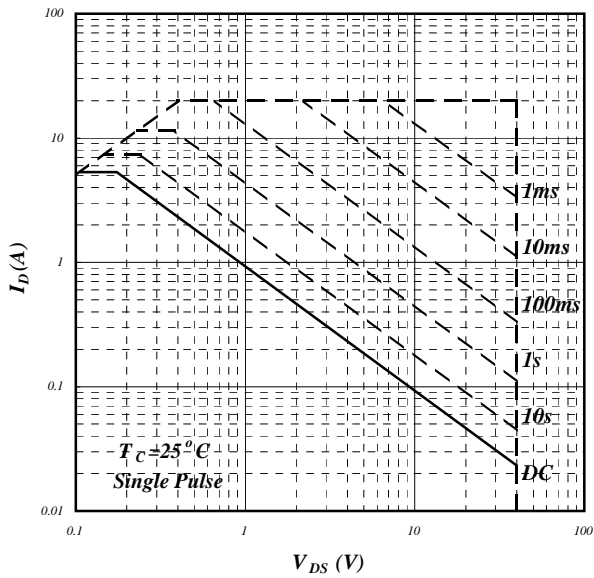


Fig 7. Maximum Safe Operating Area

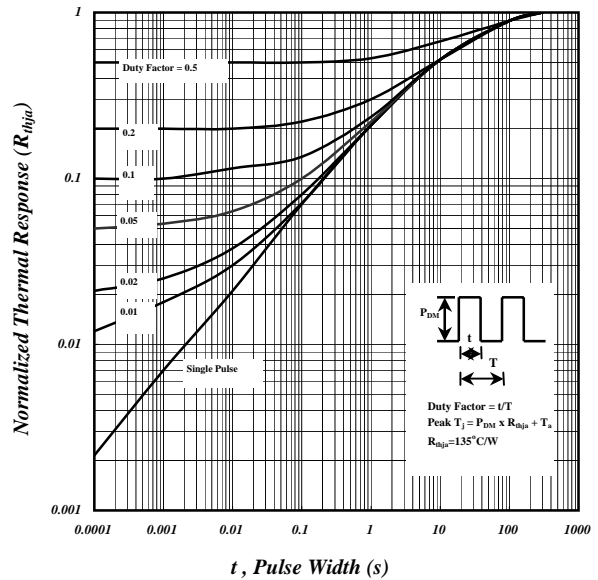


Fig 8. Effective Transient Thermal Impedance

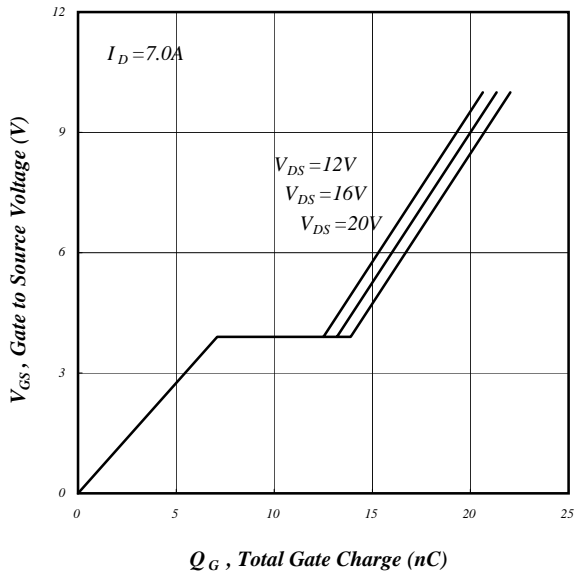


Fig 9. Gate Charge Characteristics

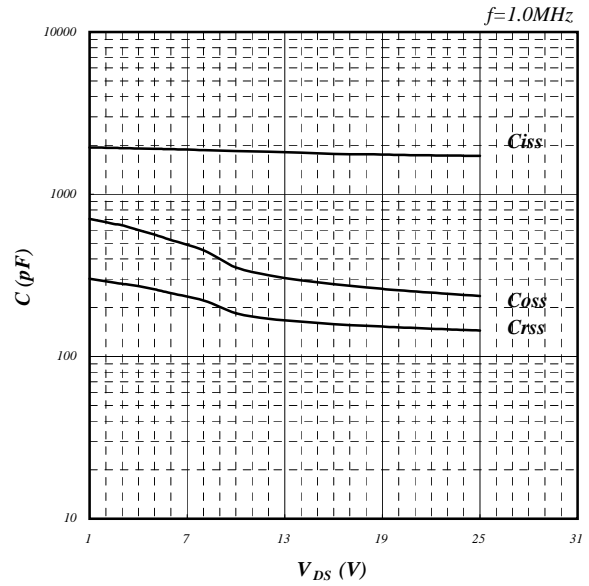


Fig 10. Typical Capacitance Characteristics

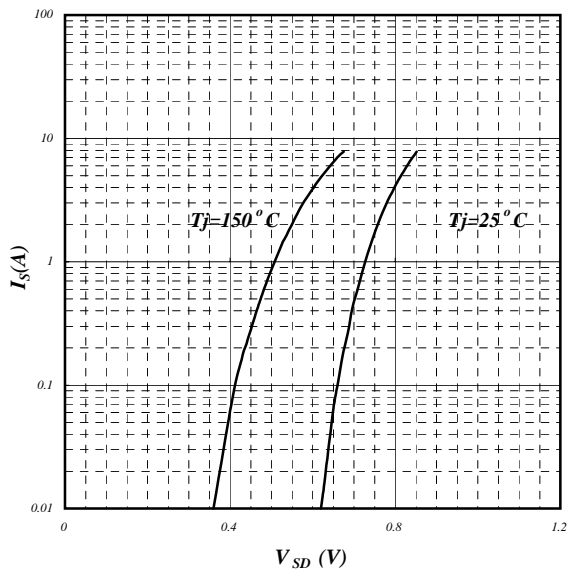


Fig 11. Forward Characteristic of Reverse Diode

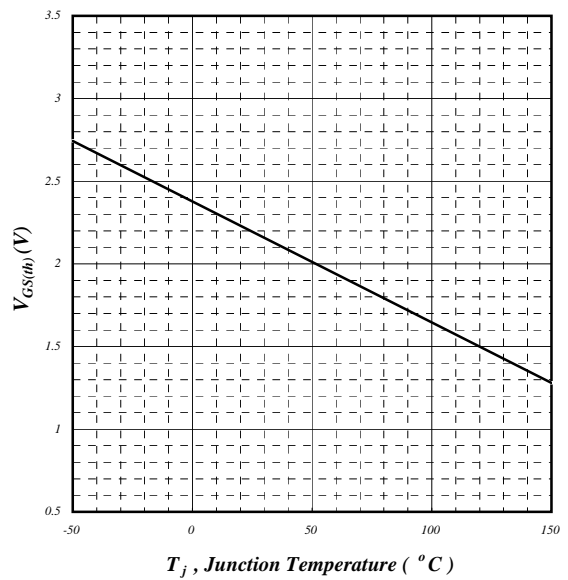


Fig 12. Gate Threshold Voltage vs. Junction Temperature

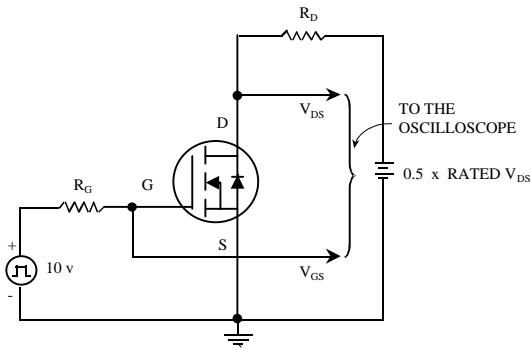


Fig 13. Switching Time Circuit

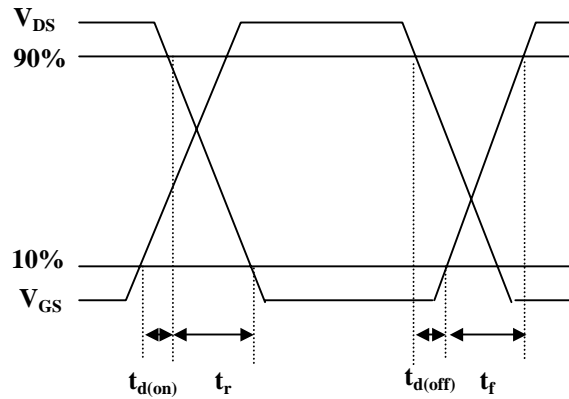


Fig 14. Switching Time Waveform

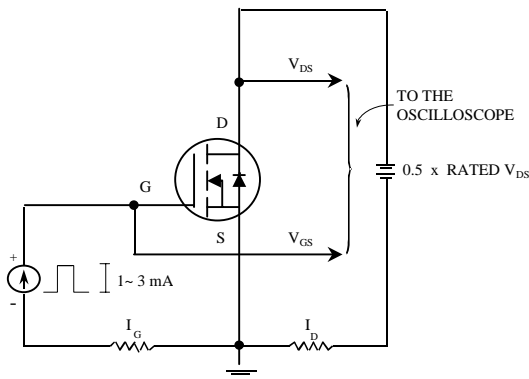


Fig 15. Gate Charge Circuit

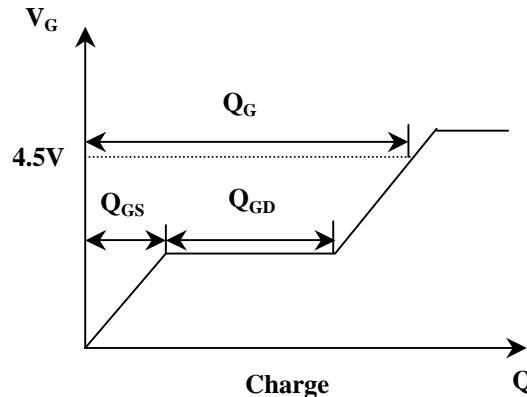


Fig 16. Gate Charge Waveform

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