

N-Channel 150-V (D-S) MOSFET

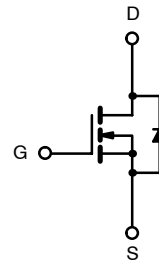
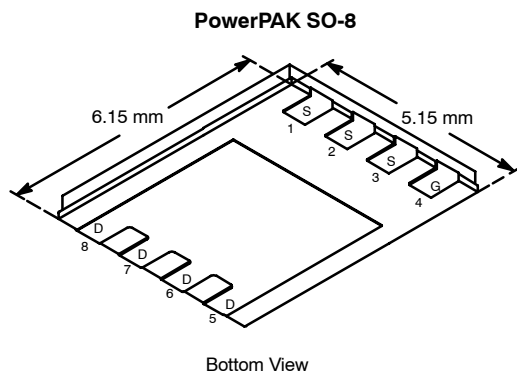
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
150	0.050 @ $V_{GS} = 10$ V	6.7

FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching
- 100% R_g Tested

APPLICATIONS

- Primary Side Switch for High Density DC/DC
- Telecom/Server 48-V DC/DC
- Industrial and 42-V Automotive



N-Channel MOSFET

Ordering Information: Si7846DP-T1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	150		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	6.7	4.0	A
	$T_A = 70^\circ\text{C}$		5.4	3.3	
Pulsed Drain Current		I_{DM}	50		
Avalanch Current		I_{AS}	25		
Continuous Source Current (Diode Conduction) ^a		I_S	4.3	1.6	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	5.2	1.9	W
	$T_A = 70^\circ\text{C}$		3.3	1.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	19	24	$^\circ\text{C/W}$
	Steady State		52	65	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	1.5	1.8	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

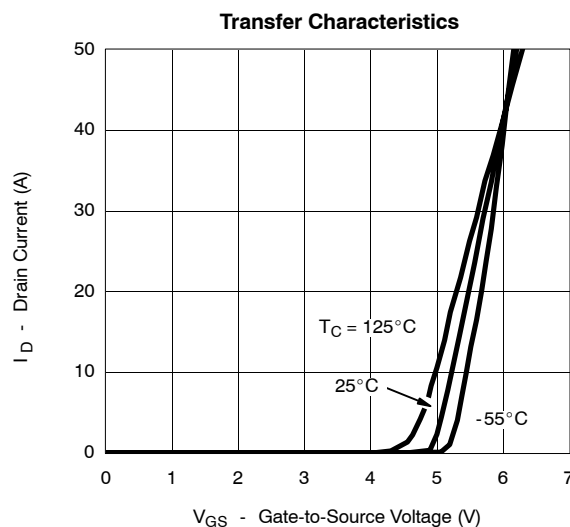
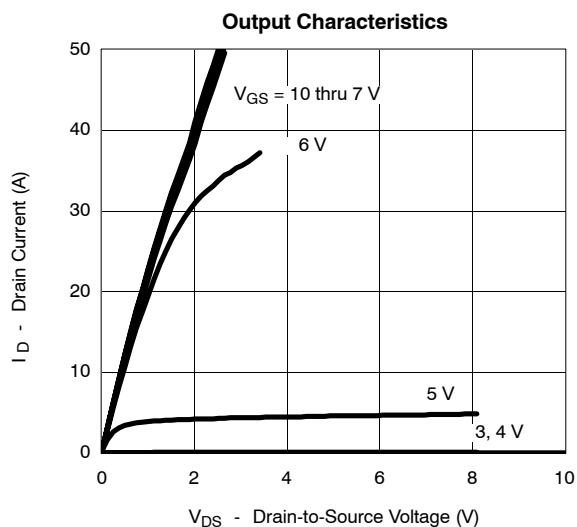
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 120 V, V _{GS} = 0 V			1	μA
		V _{DS} = 120 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 5 A		0.041	0.050	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5 A		18		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.8 A, V _{GS} = 0 V		0.75	1.1	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 75 V, V _{GS} = 10 V, I _D = 5 A		30	36	nC
Gate-Source Charge	Q _{gs}			8.5		
Gate-Drain Charge	Q _{gd}			8.5		
Gate Resistance	R _g		0.2	0.85	1.4	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 75 V, R _L = 15 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _G = 6 Ω		12	18	ns
Rise Time	t _r			7	11	
Turn-Off Delay Time	t _{d(off)}			22	33	
Fall Time	t _f			10	15	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.8 A, di/dt = 100 A/μs		40	70	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

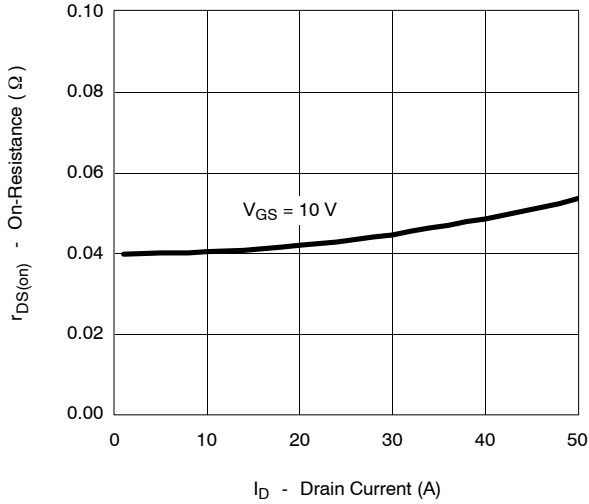
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



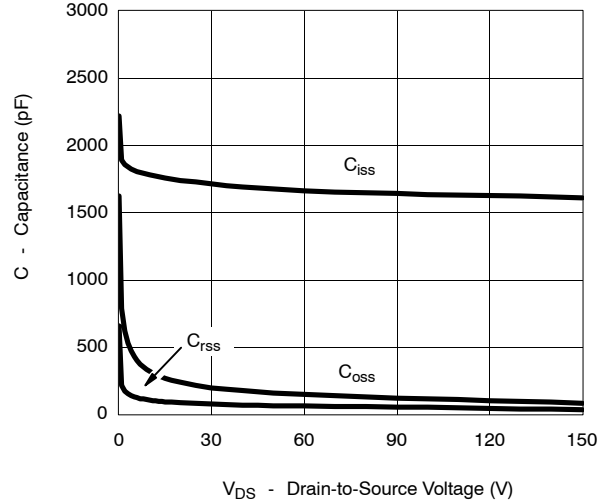


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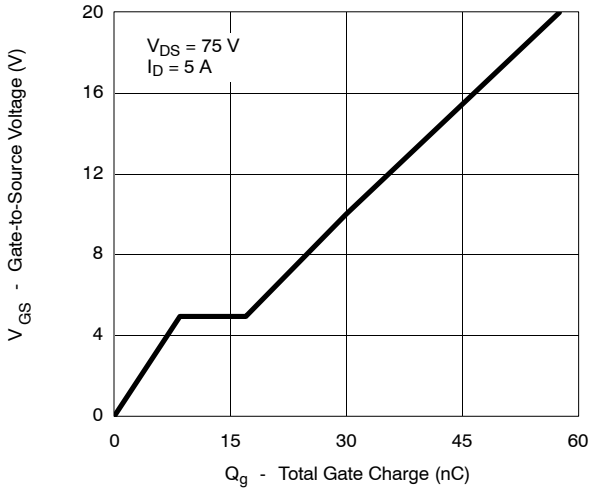
On-Resistance vs. Drain Current



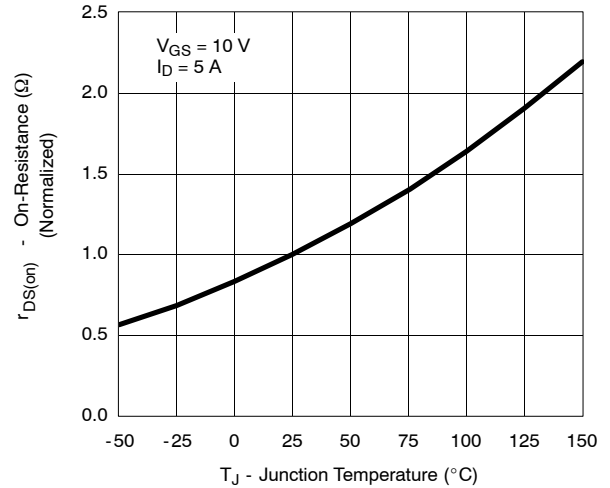
Capacitance



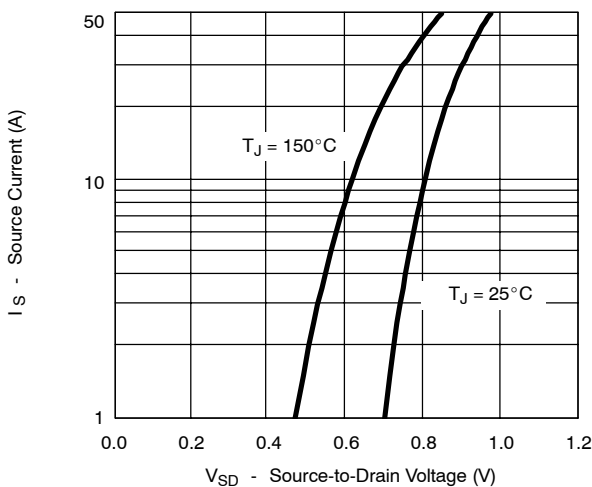
Gate Charge



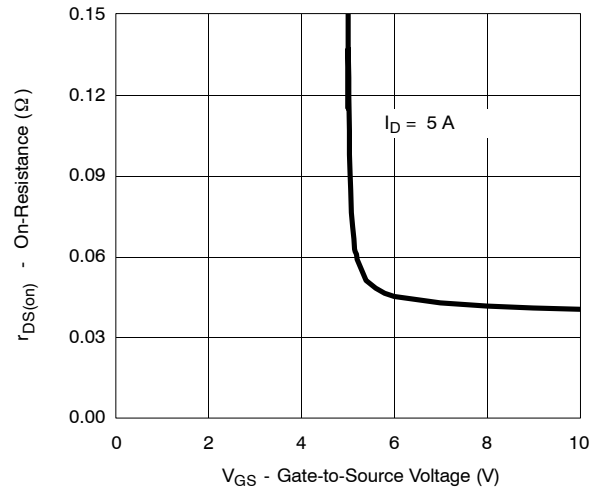
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

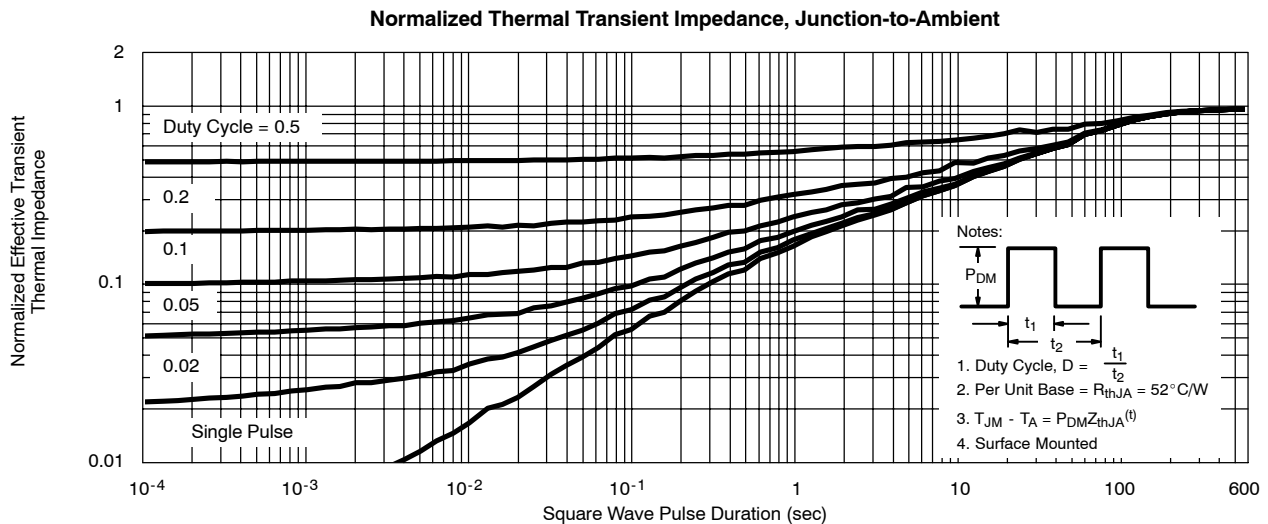
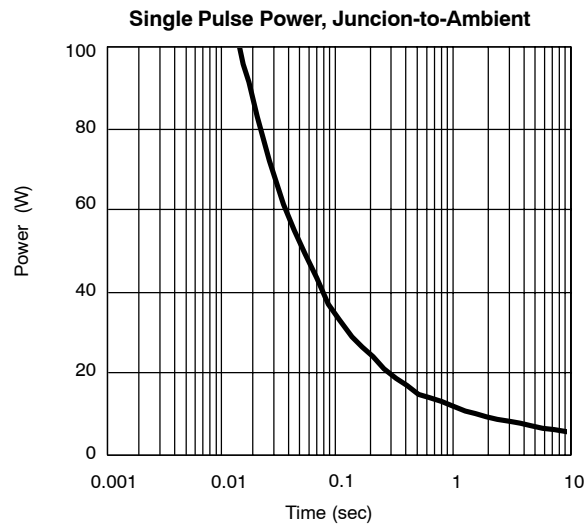
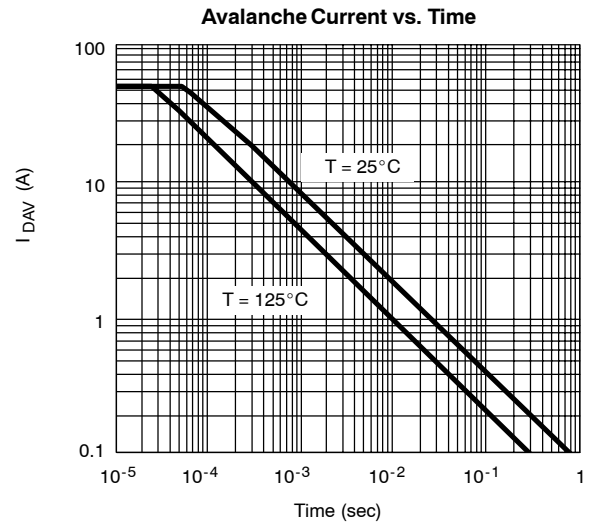
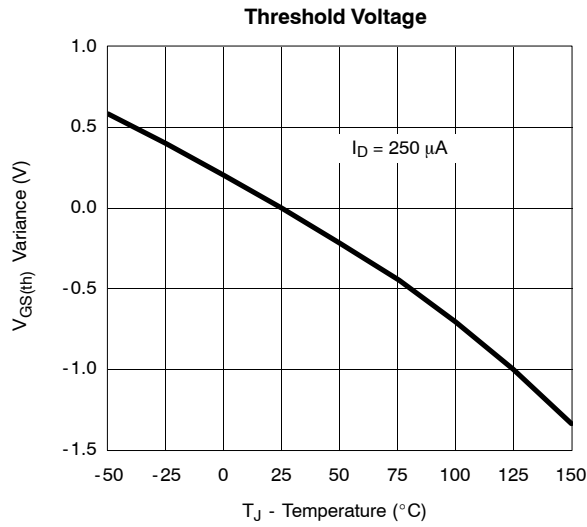


On-Resistance vs. Gate-to-Source Voltage





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