

P-Channel 12-V (D-S) MOSFET

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

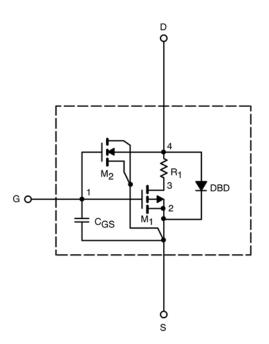
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

SUBCIRCUIT MODEL SCHEMATIC

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



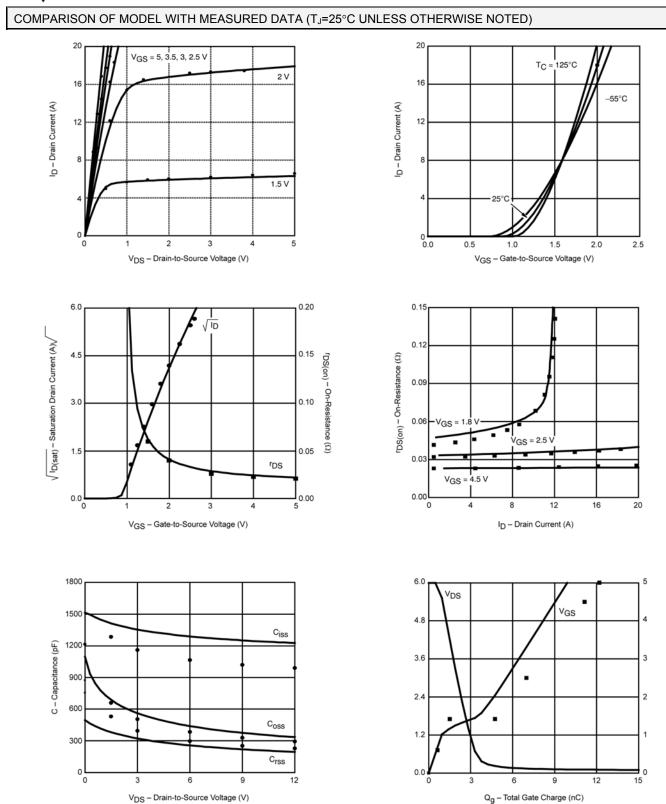
| Parameter | Symbol | Test Condition | Simulated Data | Measured Data | Unit |
|---|------------------------|--|-------------------|------------------|------|
| Static | | | 1 | <u> </u> | |
| Gate Threshold Voltage | V _{GS(th)} | V_{DS} = V_{GS} , I_D = -250 μ A | 0.70 | | V |
| On-State Drain Current ^a | I _{D(on)} | $V_{\text{DS}} \leq -5$ V, V_{GS} = -4.5 V | 116 | | А |
| Drain-Source On-State Resistance ^a | ۲ _{DS(on)} | V_{GS} = -4.5 V, I _D = -5.3 A | 0.023 | 0.025 | Ω |
| | | V_{GS} = -2.5 V, I _D = -4.6 A | 0.034 | 0.033 | |
| | | $V_{GS} = -1.8 \text{ V}, \text{ I}_{D} = -2 \text{ A}$ | 0.049 | 0.046 | |
| Forward Transconductance ^a | g _{fs} | V_{DS} = -5 V, I _D = -5.3 A | 17 | 17 | S |
| Diode Forward Voltage ^a | V _{SD} | $I_{\rm S}$ = -1 A, $V_{\rm GS}$ = 0 V | -0.78 | -0.70 | V |
| Dynamic ^b | | | • | | |
| Total Gate Charge | Qg | V_{DS} = -6 V, V_{GS} = -4.5 V, I_{D} = -5.3 A | 9.3 | 11.5 | nC |
| Gate-Source Charge | Q _{gs} | | 1.5 | 1.5 | |
| Gate-Drain Charge | Q_gd | | 3.2 | 3.2 | |
| Turn-On Delay Time | t _{d(on)} | V_{DD} = -6 V, R _L = 6 Ω I _D \cong -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω | 21 | 25 | ns |
| Rise Time | tr | | 19 | 45 | |
| Turn-Off Delay Time | t _{d(off)} | | 73 | 72 | |
| Fall Time | t _f | | 15 | 60 | |

Notes a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.



SPICE Device Model Si2333DS

Vishay Siliconix



Note: Dots and squares represent measured data.