International
IOR Rectifier

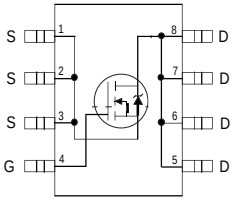
IRF7805/IRF7807

PRELIMINARY

HEXFET® Chip-Set for DC-DC Converters

- N Channel Application Specific MOSFETs
- Ideal solution for mobile processor DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Low Figure of Merit

SO-8



Top View

Description

These new devices employ advanced technology HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge.The reduced conduction and switching losses make them ideal for high efficiency DC-DC Converters that power the latest generation of mobile microprocessors.

The IRF7805/IRF7807 combination offers maximum efficiency for CPU core DC-DC converters while a pair of IRF7807 devices provides a cost effective way to generate the remaining system voltages.

	IRF7805	IRF7807
Vds	30V	30V
Rds(on)	11mΩ	25mΩ
Fom	110	110
Qg	26nC	12nC
Qgd	6.8nC	2.9nC
Qgs	1.4nC	0.75nC

Absolute Maximum Ratings

Parameter			IRF7805	IRF7807	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current	25°C	I_D	13	8.3	A
	70°C		10	66	
Pulsed Drain Current		I_{DM}	100	66	
Power Dissipation	25°C	P_D	2.5		W
	70°C		1.6		
Junction & Storage Temperature Range		T_J, T_{STG}	–55 to 150		°C
Continuous Source Current		I_S	2.5	2.5	A
Pulsed source Current		I_{OL}	106	66	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient④	$R_{\theta JA}$	50	°C/W

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Electrical Characteristics IRF7805 IRF7807

Parameter		Min	Typ	Max	Min	Typ	Max	Units	Conditions
Static Drain-Source on Resistance	R_{DS}(on)		9.2	11		17	25	mΩ	V_{GS} = 5V, I_D = 7A
Gate Threshold Voltage	V_{GS}(th)	0.7			0.7			V	V_{DS} = V_{GS}, I_D = 250µA
Drain-Source Leakage Current	I_{DSS}			1			1	µA	V_{DS} = 24V I_D = 7A
Gate-Source Leakage Current	I_{GSS}			±100			±100	nA	V_{GS} = ±12V
Total Gate Charge	Qg		25	37		12	17	nC	V_{GS} = 5V, I_D = 7A
Pre-Vth Gate-Source Charge	Qgs1		3.6			2.1			V_{GS} = 16V, I_D = 7A
Post-Vth Gate-Source Charge	Qgs2		1.4	2		0.75	1.1	nC	
Output Charge	Qdss								
Gate to Drain (Charge)	Qgd		6.8	9.5		2.9	4.1		
Gate Resistance	Rg		1.7			1.2		Ω	
Turn-on Delay Time	t_d(on)		11			14			V_{DD} = 15V I_D = 1A Rg = 6Ω V_{GS} = 4.5V R_{DS} = 15Ω
Rise Time	t_r		10			72		ns	
Turn-off Delay Time	t_d (off)		83			24			
Fall Time	t_f		48			76			

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Min	Typ	Max	Units	Conditions
Diode Forward Voltage	V_{SD}			1.2			1.2	V	I_S = V_{GS} = I_S = 13A, V_{GS} = 0V
Reverse Recovery Time	t_{rr}		92	140		68	100	ns	I_F = 8A
Reverse Recovery Charge	Q_{rr}		150	230		100	150	nC	di/dt = 100A/µs
Reverse Recovery Change (with Parallel Schottky)	$Q_{rr(s)}$								

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② I_{SD} ≤ 11A, di/dt ≤ 110A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C.
③ Pulse width ≤ 300 µs; duty cycle ≤ 2%.
④ When mounted on 1 inch square copper board, t < 10 sec.

In-depth analysis of the synchronous buck regulator has been performed with both Spice and more detailed Mathcad simulations. Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are approximated by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive}$$

This can be expanded to ;

$$P_{loss} = \left(I_{rms}^{\ 2} \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes a term new to power MOSFET users - Q_{gs2} This element is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2} can be seen from fig 1.

Q_{gs2} indicates the charge that must be supplied by the gate driver once the threshold voltage has been reached (t1) and the drain current rises to I_{dmax} (t2) at which point the drain voltage collapses. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

In the past it has been common for designers to use a much simpler equation to look for suitable control FET devices.

$$R_{ds(on)} \times Q_g$$

This oversimplification misses the impact that Q_{gs2}, Q_{gs1}, Q_{osss} & Q_{gd} have on the MOSFET power losses. So important are these new gate charge elements in understanding MOSFET power losses that engineers at International Rectifier have recommended that the new terms Q_{gs2}, Q_{gs1} and Q_{oss} be added to the data sheet characteristics.

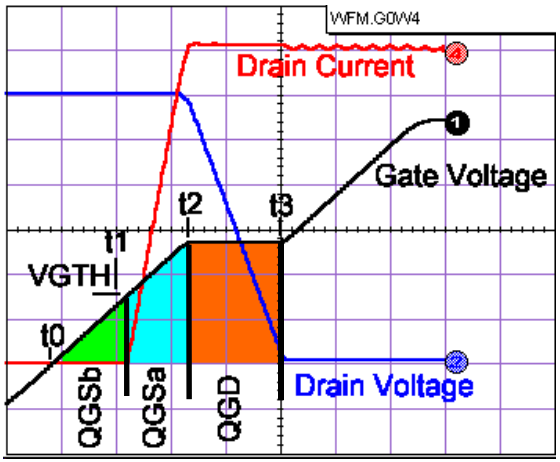

Figure 1: Typical MOSFET switching waveform

The power loss equation for Q2 is approximated by;

$$P_{loss} = \left(I_{rms}^{\ 2} \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become dominant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device (Fig 2). Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on. The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, result-

ing in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be carefully controlled to minimize the potential for Cdv/dt turn on.

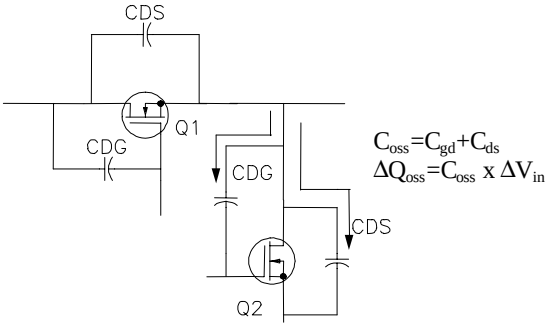

Figure 2: Q_{oss} Characteristic

Typical Mobile PC Application

The performance of these new devices has been tested in circuit and correlates well with performance predictions generated by the system models. IRF7805 and IRF7807 were designed specifically for the mobile Pentium II CPU core supply. Fig 3 shows performance characteristics for this converter under low charge battery conditions, typical battery and worst case adapter input. An advantage of this new technology platform is that the MOSFETs it produces are suitable for both control FET and synchronous FET applications. This has been demonstrated with the 3.3V and 5V converters. (Fig 4 and Fig 5). In these applications the same MOSFET IRF7807 was used for both the control FET (Q1) and the synchronous FET (Q2). This provides a highly effective cost/performance solution

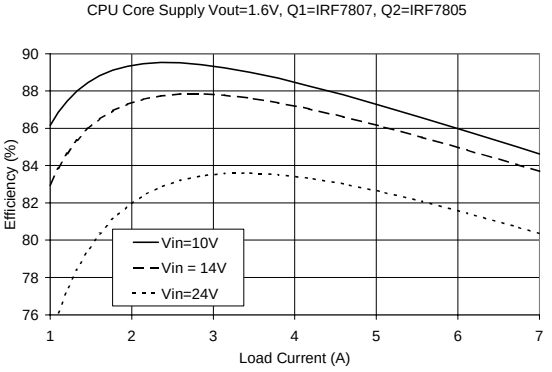

Figure 3

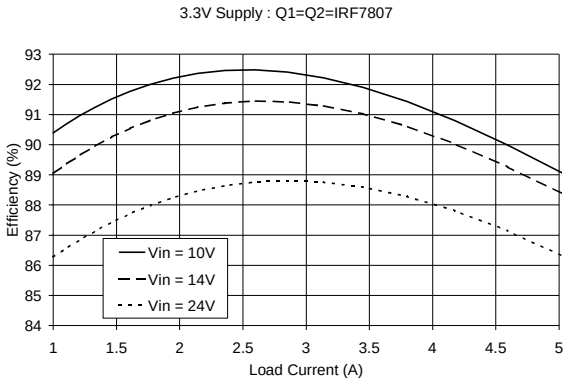

Figure 4

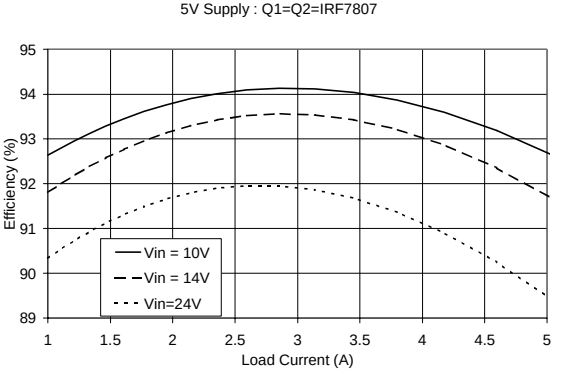

Figure 5

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IRF7805

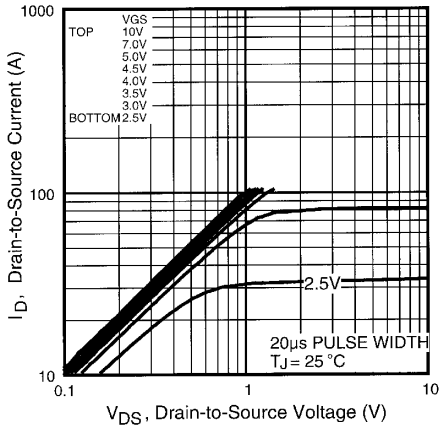
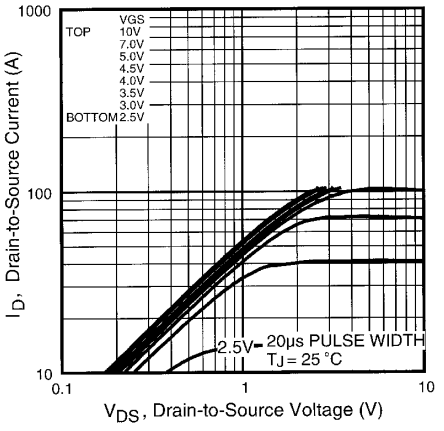


Figure 6

IRF7807



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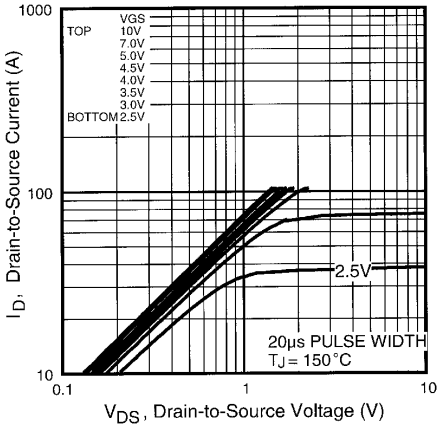

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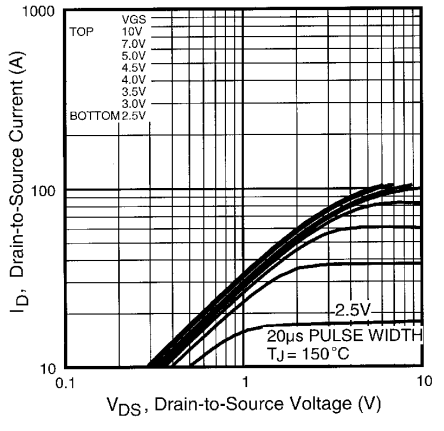

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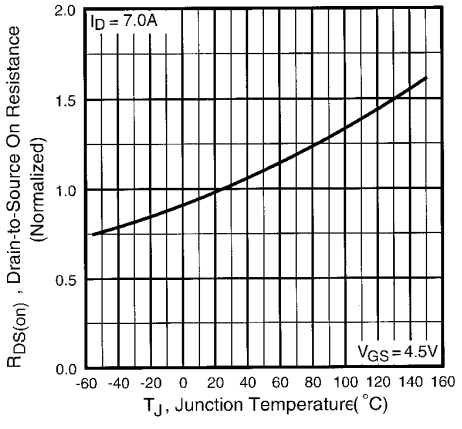

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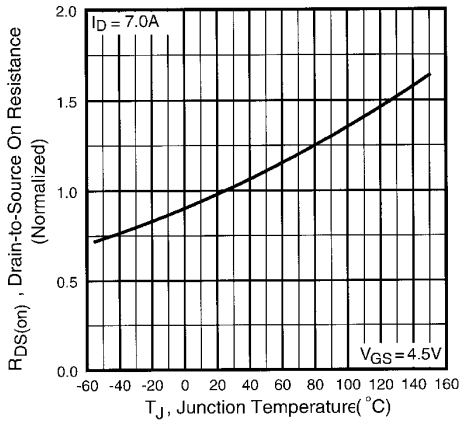

Figure 11

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IRF7805

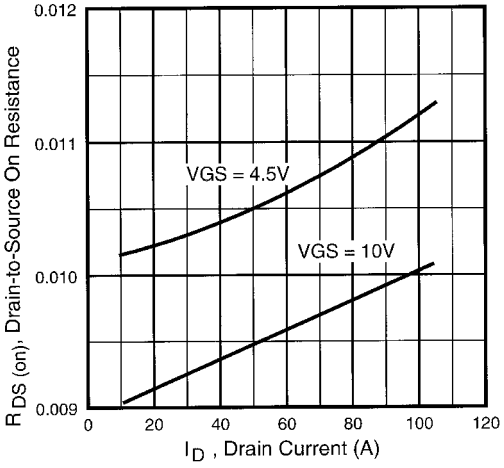


Figure 12

IRF7807

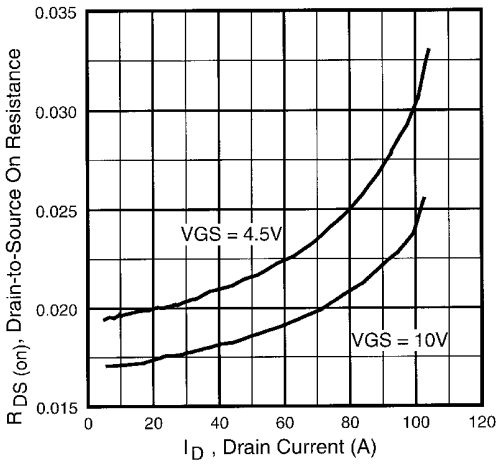


Figure 13

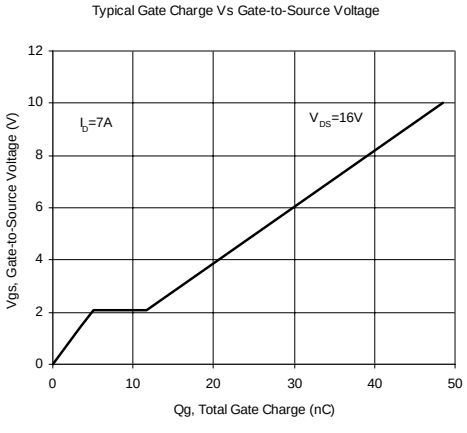


Figure 14

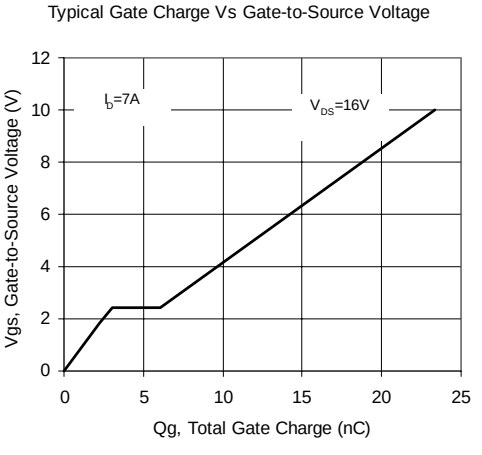
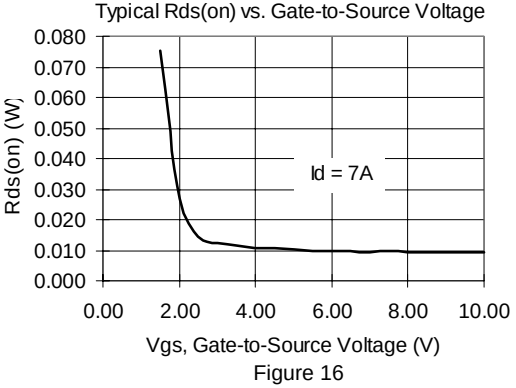


Figure 15



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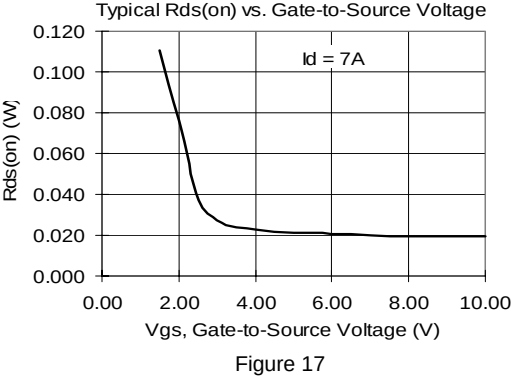


Figure 17

IRF7805

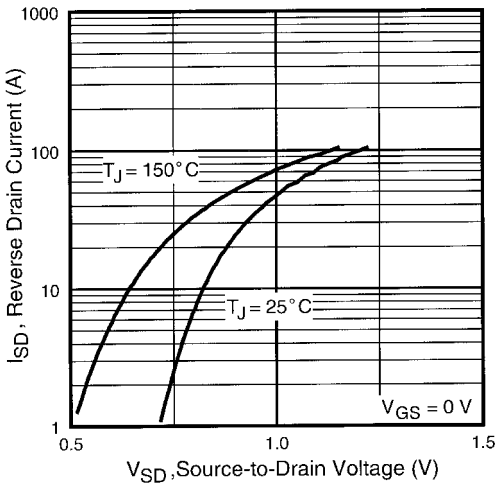
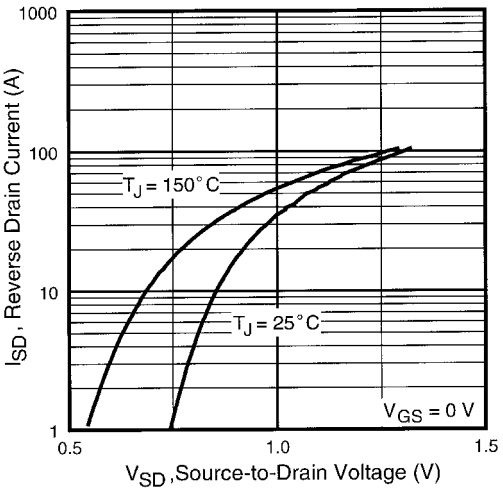


Figure 18

IRF7807



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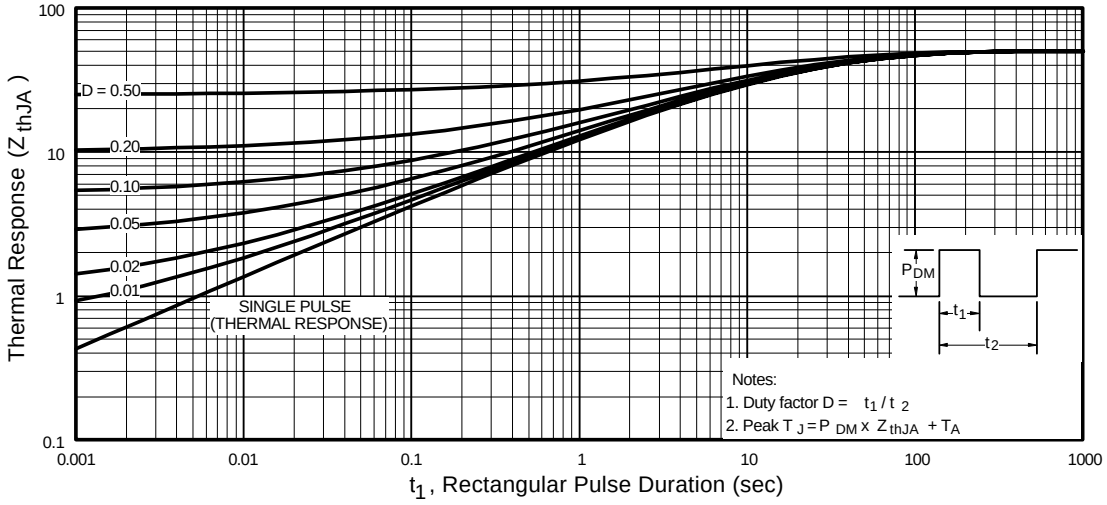

Figure 20

IRF7805/IRF7807

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```
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**************************************
*      Model Generated by MODPEX     *
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**************************************

* Model generated on Apr 14, 98
* MODEL FORMAT: SPICE3
* Symmetry POWER MOS Model (Version 1.0)
* External Node Designations
* Node 1 -> Drain
* Node 2 -> Gate
* Node 3 -> Source
M1 9 7 8 8 MM L=100u W=100u
* Default values used in MM:
* The voltage-dependent capacitances are
* not included. Other default values are:
*   RS=0 RD=0 LD=0 CBD=0 CBS=0 CGBO=0
.MODEL MM NMOS LEVEL=1 IS=1e-32
+VTO=1.84206 LAMBDA=0 KP=136.761
+CGSO=2.51072e-05 CGDO=1e-11
RS 8 3 0.0001
D1 3 1 MD
.MODEL MD D IS=5.54402e-09 RS=0.00225926 N=1.38507 BV=30
+IBV=0.00025 EG=1 XTI=4 TT=0.0001
+CJO=2.64483e-09 VJ=2.46243 M=0.500664 FC=0.5
RDS 3 1 1e+06
RD 9 1 0.00692217
RG 2 7 1.47076
D2 4 5 MD1
* Default values used in MD1:
*   RS=0 EG=1.11 XTI=3.0 TT=0
*   BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=1.56271e-09 VJ=0.5 M=0.852472 FC=1e-08
D3 0 5 MD2
* Default values used in MD2:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=0.4 RS=3.00001e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 1.56271e-09
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 0 6 MD3
* Default values used in MD3:
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*   RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=0.4
.ENDS irf7805
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IRF7805/IRF7807

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M1 9 7 8 8 MM L=100u W=100u
* Default values used in MM:
* The voltage-dependent capacitances are
* not included. Other default values are:
*   RS=0 RD=0 LD=0 CBD=0 CBS=0 CGBO=0
.MODEL MM NMOS LEVEL=1 IS=1e-32
+VTO=1.95523 LAMBDA=0.113615 KP=22.2883
+CGSO=1.1909e-05 CGDO=1.23318e-07
RS 8 3 0.00764138
D1 3 1 MD
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+IBV=0.00025 EG=1.2 XTI=3.38686 TT=0.0001
+CJO=1.25482e-09 VJ=2.6804 M=0.545484 FC=0.5
RDS 3 1 1e+06
RD 9 1 0.00122468
RG 2 7 6
D2 4 5 MD1
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*   BV=infinite IBV=1mA
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*   BV=infinite IBV=1mA
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RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 5.8552e-10
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 0 6 MD3
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IRF7805/IRF7807

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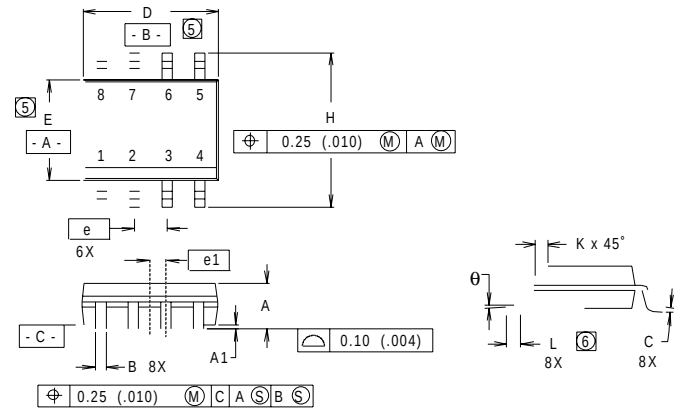
Package Outline

SO8 Outline



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
θ	0°	8°	0°	8°

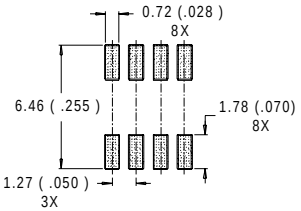
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS
MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).

(6) DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

RECOMMENDED FOOTPRINT



Part Marking Information

SO8

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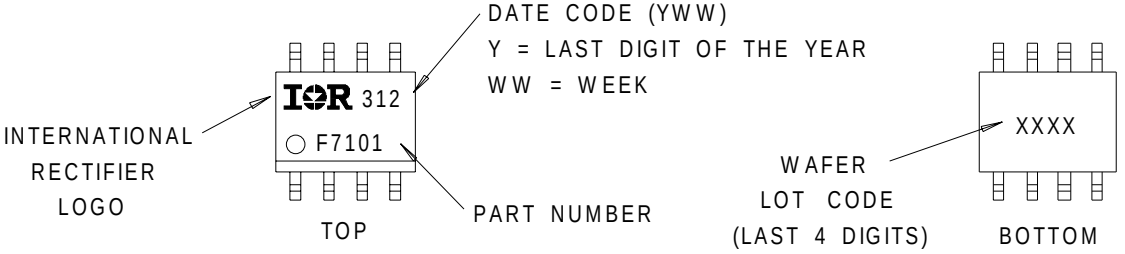

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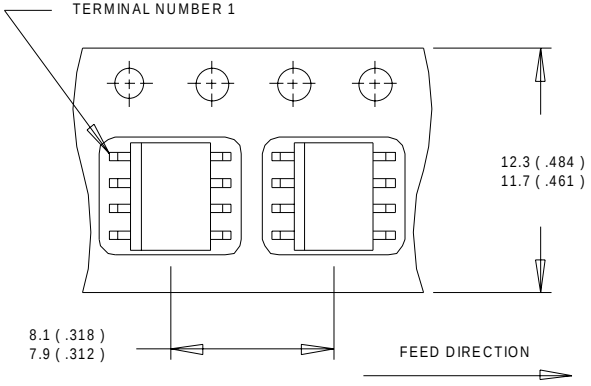
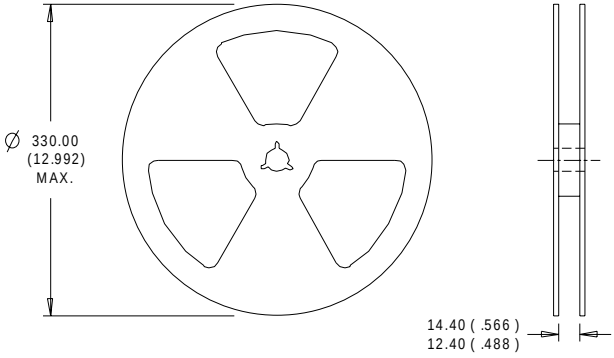
Tape & Reel Information

SO*

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

IRF7805/IRF7807

International
IOR Rectifier

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IOR Rectifier

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