

# FDS8880

## N-Channel PowerTrench® MOSFET

30V, 11.6A, 10mΩ

### Features

- $r_{DS(ON)} = 10m\Omega$ ,  $V_{GS} = 10V$ ,  $I_D = 11.6A$
- $r_{DS(ON)} = 12m\Omega$ ,  $V_{GS} = 4.5V$ ,  $I_D = 10.7A$
- High performance trench technology for extremely low  $r_{DS(ON)}$
- Low gate charge
- High power and current handling capability

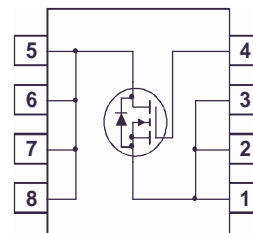
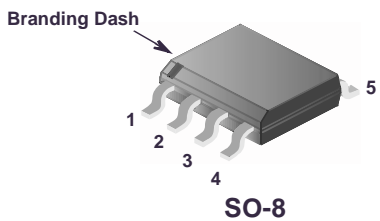
### Applications

- DC/DC converters

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(ON)}$  and fast switching speed.

FDS8880 N-Channel PowerTrench® MOSFET



**MOSFET Maximum Ratings**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current		
	Continuous ( $T_A = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ , $R_{\theta JA} = 50^\circ\text{C/W}$ )	11.6	A
	Continuous ( $T_A = 25^\circ\text{C}$ , $V_{GS} = 4.5\text{V}$ , $R_{\theta JA} = 50^\circ\text{C/W}$ )	10.7	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	82	mJ
$P_D$	Power dissipation	2.5	W
	Derate above $25^\circ\text{C}$	20	mW/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	25	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 10 seconds (Note 3)	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 1000 seconds (Note 3)	85	$^\circ\text{C/W}$

**Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8880	FDS8880	SO-8	330mm	12mm	2500 units
FDS8880	FDS8880_NL (Note 4)	SO-8	330mm	12mm	2500 units

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$T_A = 150^\circ\text{C}$	-	-	250	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	1.2	-	2.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 11.6\text{A}$ , $V_{GS} = 10\text{V}$	-	0.0079	0.010	$\Omega$
		$I_D = 10.7\text{A}$ , $V_{GS} = 4.5\text{V}$	-	0.0096	0.012	
		$I_D = 11.6\text{A}$ , $V_{GS} = 10\text{V}$ , $T_A = 150^\circ\text{C}$	-	0.0125	0.0163	

**Dynamic Characteristics**

$C_{ISS}$	Input Capacitance	$V_{DS} = 15\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	1235	-	pF	
$C_{OSS}$	Output Capacitance		-	260	-	pF	
$C_{RSS}$	Reverse Transfer Capacitance		-	150	-	pF	
$R_G$	Gate Resistance	$V_{GS} = 0.5\text{V}$ , $f = 1\text{MHz}$	0.6	2.5	4.3	$\Omega$	
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 15\text{V}$ $I_D = 11.6\text{A}$ $I_g = 1.0\text{mA}$	-	23	30	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V		-	12	16	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 1V		-	1.3	1.6	nC
$Q_{gs}$	Gate to Source Gate Charge			-	3.3	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	2.0	-	nC	
$Q_{gd}$	Gate to Drain "Miller" Charge		-	4.2	-	nC	

**Switching Characteristics** ( $V_{GS} = 10V$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 15V, I_D = 11.6A$ $V_{GS} = 10V, R_{GS} = 11\Omega$	-	-	51	ns
$t_{d(ON)}$	Turn-On Delay Time		-	7	-	ns
$t_r$	Rise Time		-	27	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	38	-	ns
$t_f$	Fall Time		-	15	-	ns
$t_{OFF}$	Turn-Off Time		-	-	80	ns

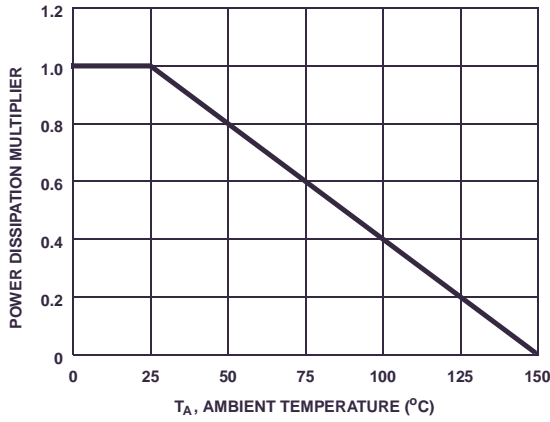
**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 11.6A$	-	-	1.25	V
		$I_{SD} = 2.1A$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 11.6A, dI_{SD}/dt=100A/\mu s$	-	-	30	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 11.6A, dI_{SD}/dt=100A/\mu s$	-	-	20	nC

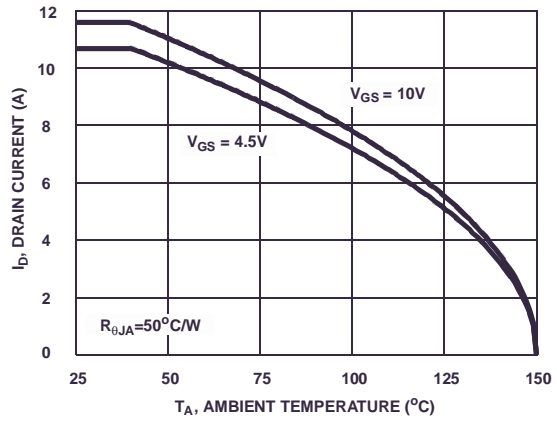
**Notes:**

- 1: Starting  $T_J = 25^\circ C, L = 1mH, I_{AS} = 12.8A, V_{DD} = 30V, V_{GS} = 10V$ .
- 2:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.
- 3:  $R_{\theta JA}$  is measured with 1.0 in<sup>2</sup> copper on FR-4 board
- 4: FDS8880\_NL is lead free product. FDS8880\_NL marking will appear on the reel label.

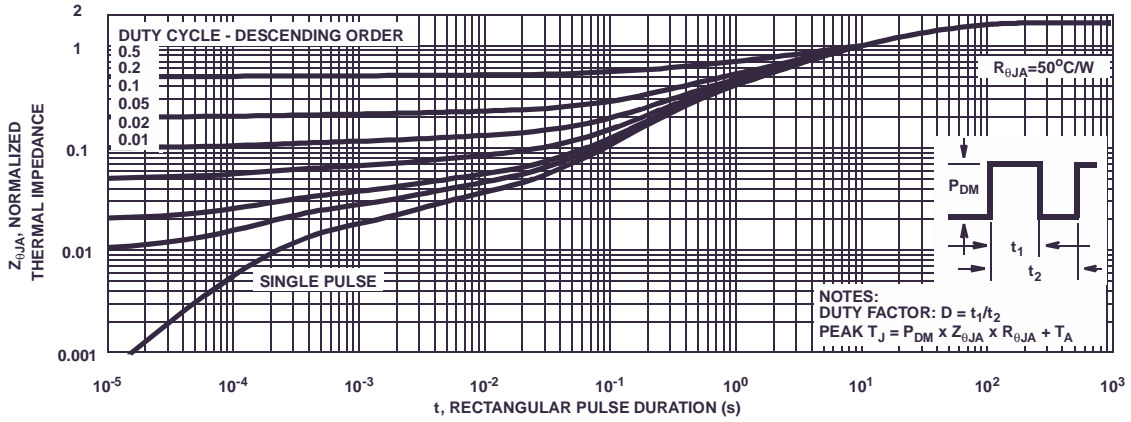
**Typical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted



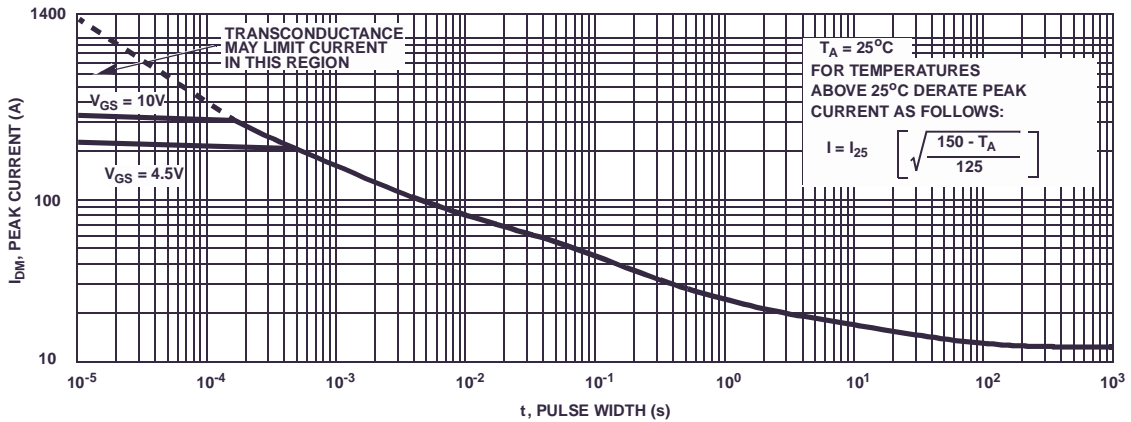
**Figure 1. Normalized Power Dissipation vs Ambient Temperature**



**Figure 2. Maximum Continuous Drain Current vs Ambient Temperature**

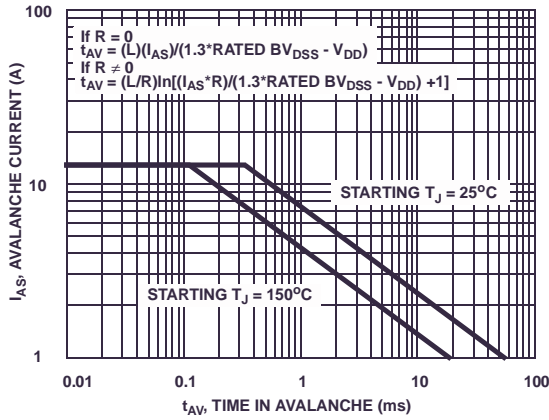


**Figure 3. Normalized Maximum Transient Thermal Impedance**

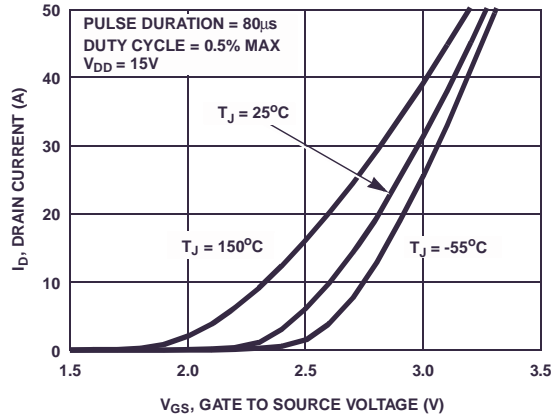


**Figure 4. Peak Current Capability**

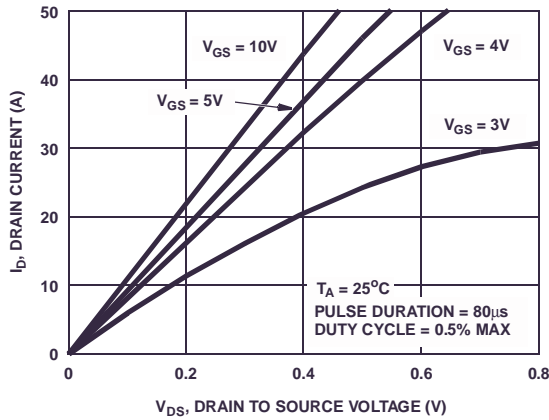
**Typical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted



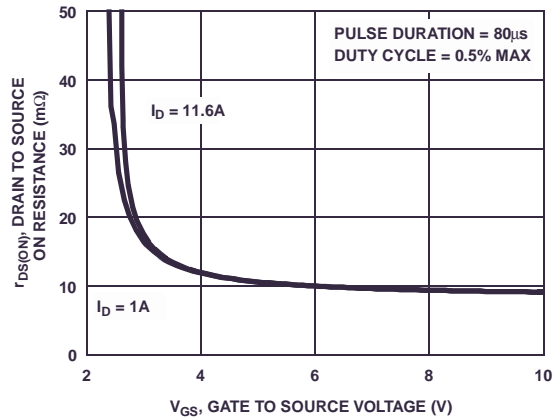
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515  
**Figure 5. Unclamped Inductive Switching Capability**



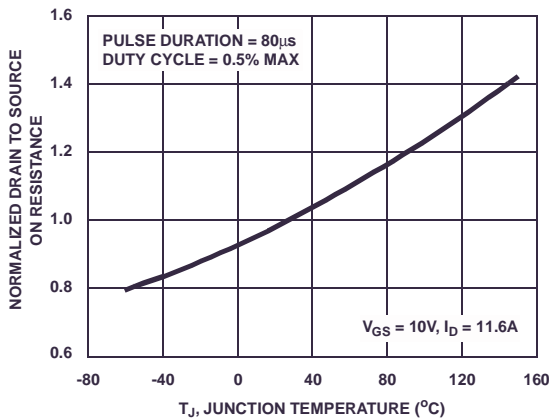
**Figure 6. Transfer Characteristics**



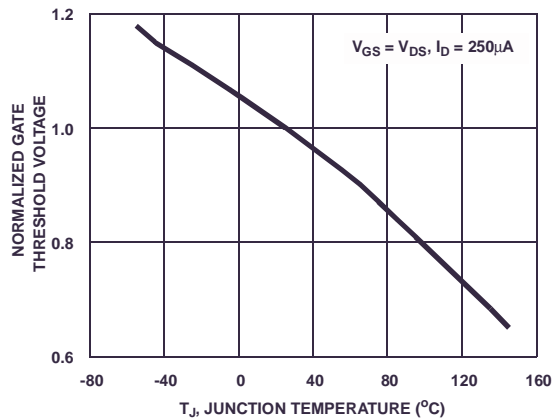
**Figure 7. Saturation Characteristics**



**Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current**

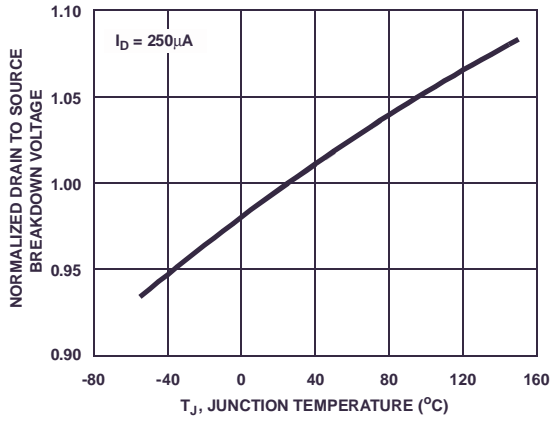


**Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature**

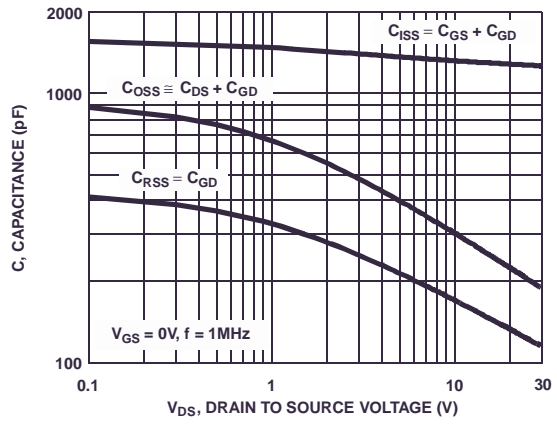


**Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature**

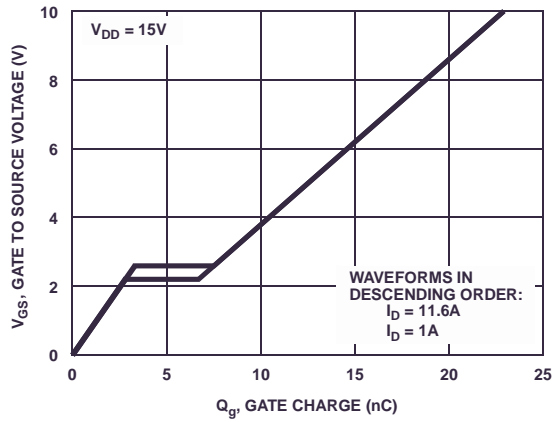
**Typical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted



**Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 12. Capacitance vs Drain to Source Voltage**



**Figure 13. Gate Charge Waveforms for Constant Gate Currents**

### Test Circuits and Waveforms

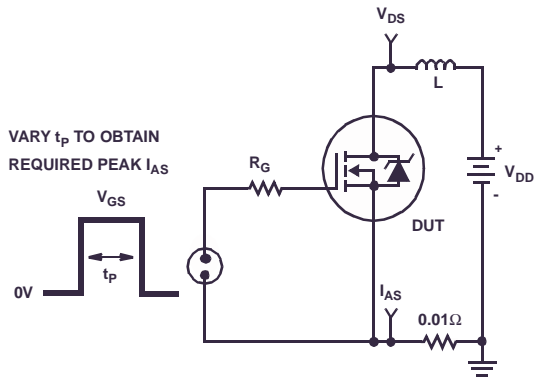


Figure 14. Unclamped Energy Test Circuit

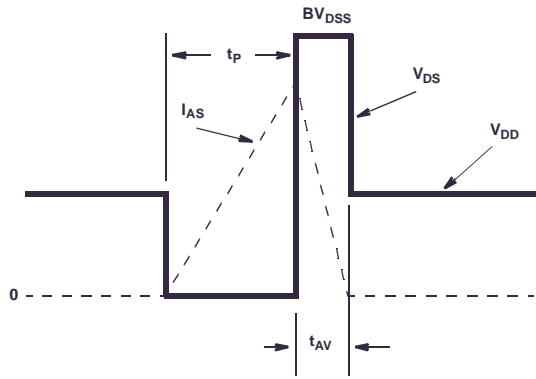


Figure 15. Unclamped Energy Waveforms

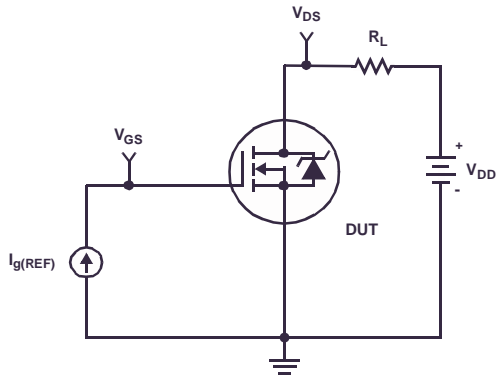


Figure 16. Gate Charge Test Circuit

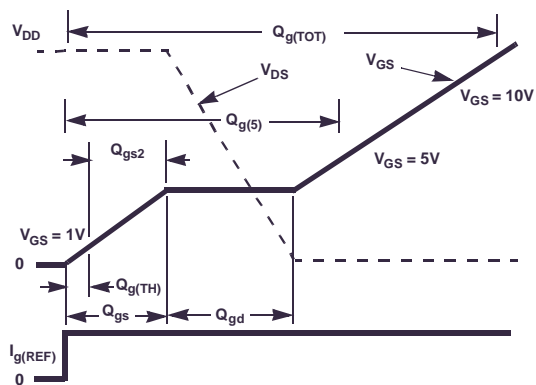


Figure 17. Gate Charge Waveforms

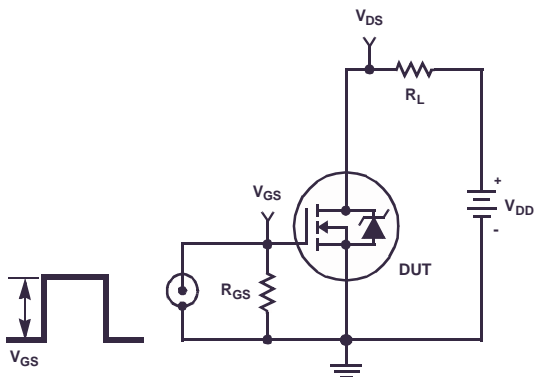


Figure 18. Switching Time Test Circuit

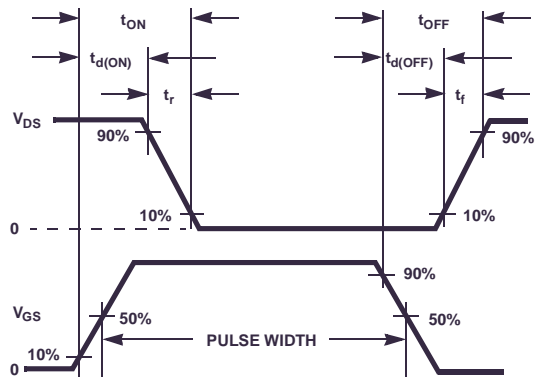


Figure 19. Switching Time Waveforms

### Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{JM}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{DM}$ , in an application. Therefore the application's ambient temperature,  $T_A$  ( $^{\circ}C$ ), and thermal resistance  $R_{\theta JA}$  ( $^{\circ}C/W$ ) must be reviewed to ensure that  $T_{JM}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of  $P_{DM}$  is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized

maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 64 + \frac{26}{0.23 + \text{Area}} \quad (\text{EQ. 2})$$

The transient thermal impedance ( $Z_{\theta JA}$ ) is also effected by varied top copper board area. Figure 22 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, C THERM1 through C THERM5 and R THERM1 through R THERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

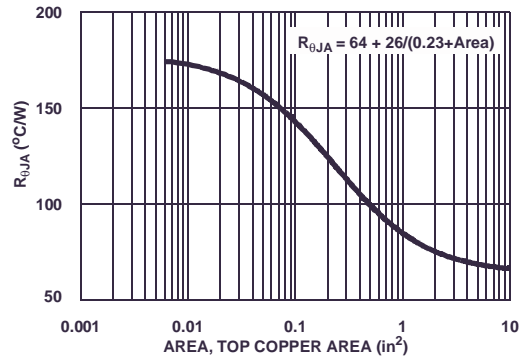


Figure 21. Thermal Resistance vs Mounting Pad Area

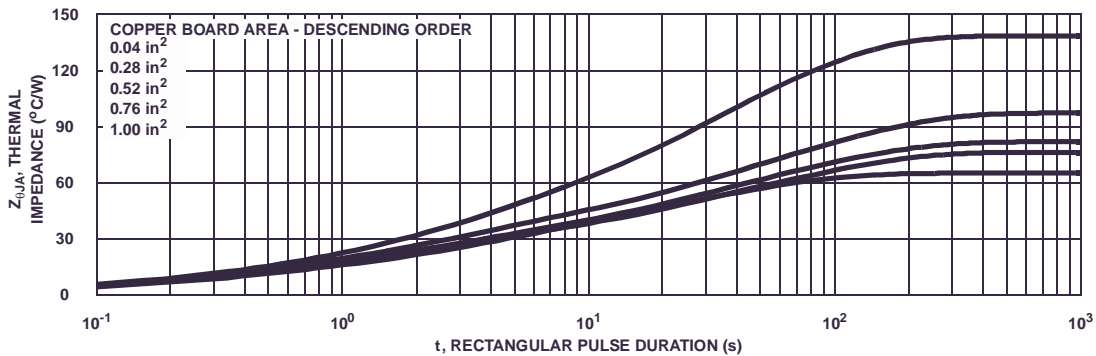


Figure 22. Thermal Impedance vs Mounting Pad Area



**PSPICE Electrical Model**

.SUBCKT FDS8880 2 1 3 ; rev August 2004  
 Ca 12 8 9.3e-10  
 Cb 15 14 9.3e-10  
 Cin 6 8 1.15e-9

Dbody 7 5 DbodyMOD  
 Dbreak 5 11 DbreakMOD  
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 33.5  
 Eds 14 8 5 8 1  
 Egs 13 8 6 8 1  
 Esg 6 10 6 8 1  
 Evthres 6 21 19 8 1  
 Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 3.6e-9  
 Ldrain 2 5 1.0e-9  
 Lsource 3 7 1.2e-10

RLgate 1 9 36  
 RLdrain 2 5 10  
 RLsource 3 7 1.2

Mmed 16 6 8 8 MmedMOD  
 Mstro 16 6 8 8 MstroMOD  
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1  
 Rdrain 50 16 RdrainMOD 2.9e-3  
 Rgate 9 20 2.5  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 Rsource 8 7 RsourceMOD 5.4e-3  
 Rvthres 22 8 RvthresMOD 1  
 Rvtemp 18 19 RvtempMOD 1  
 S1a 6 12 13 8 S1AMOD  
 S1b 13 12 13 8 S1BMOD  
 S2a 6 15 14 13 S2AMOD  
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*170),5))}}

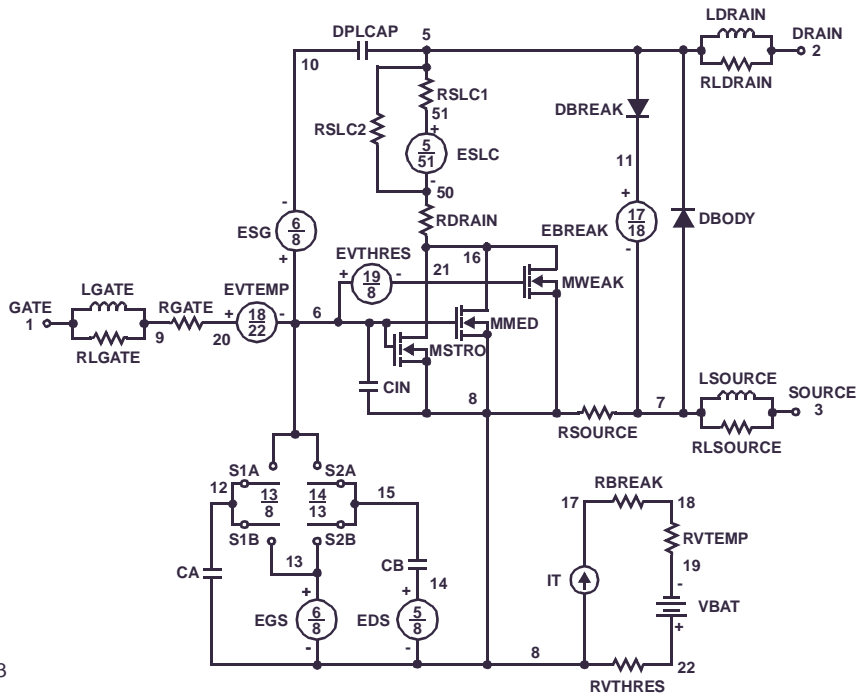
.MODEL DbodyMOD D (IS=2.6E-12 IKF=10 N=1.01 RS=5.6e-3 TRS1=8e-4 TRS2=2e-7  
 + CJO=5e-10 M=0.55 TT=1e-11 XT1=2)  
 .MODEL DbreakMOD D (RS=0.2 TRS1=1e-3 TRS2=-8.9e-6)  
 .MODEL DplcapMOD D (CJO=4.27e-10 IS=1e-30 N=10 M=0.38)  
 .MODEL MmedMOD NMOS (VTO=1.8 KP=5 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.5)  
 .MODEL MstroMOD NMOS (VTO=2.21 KP=150 IS=1e-30 N=10 TOX=1 L=1u W=1u)  
 .MODEL MweakMOD NMOS (VTO=1.53 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=25 RS=0.1)

.MODEL RbreakMOD RES (TC1=8.3e-4 TC2=-8e-7)  
 .MODEL RdrainMOD RES (TC1=5.5e-3 TC2=1.2e-5)  
 .MODEL RSLCMOD RES (TC1=1e-4 TC2=1e-6)  
 .MODEL RsourceMOD RES (TC1=1e-3 TC2=3e-6)  
 .MODEL RvthresMOD RES (TC1=-1.5e-3 TC2=-6e-6)  
 .MODEL RvtempMOD RES (TC1=-1.8e-3 TC2=2e-7)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-3.5)  
 .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-4)  
 .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-1.0)  
 .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.0 VOFF=-1.5)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





**SPICE Thermal Model**

REV August 2004  
 FDS8880  
 Copper Area =1.0 in<sup>2</sup>  
 C THERM1 TH 8 2.0e-3  
 C THERM2 8 7 5.0e-3  
 C THERM3 7 6 1.0e-2  
 C THERM4 6 5 4.0e-2  
 C THERM5 5 4 9.0e-2  
 C THERM6 4 3 2e-1  
 C THERM7 3 2 1  
 C THERM8 2 TL 3

R THERM1 TH 8 1e-1  
 R THERM2 8 7 5e-1  
 R THERM3 7 6 1  
 R THERM4 6 5 5  
 R THERM5 5 4 8  
 R THERM6 4 3 12  
 R THERM7 3 2 18  
 R THERM8 2 TL 25

**SABER Thermal Model**

Copper Area = 1.0 in<sup>2</sup>  
 template thermal\_model th tl  
 thermal\_c th, tl  
 {  
 ctherm.ctherm1 th 8 =2.0e-3  
 ctherm.ctherm2 8 7 =5.0e-3  
 ctherm.ctherm3 7 6 =1.0e-2  
 ctherm.ctherm4 6 5 =4.0e-2  
 ctherm.ctherm5 5 4 =9.0e-2  
 ctherm.ctherm6 4 3 =2e-1  
 ctherm.ctherm7 3 2 1  
 ctherm.ctherm8 2 tl 3  
  
 rtherm.rtherm1 th 8 =1e-1  
 rtherm.rtherm2 8 7 =5e-1  
 rtherm.rtherm3 7 6 =1  
 rtherm.rtherm4 6 5 =5  
 rtherm.rtherm5 5 4 =8  
 rtherm.rtherm6 4 3 =12  
 rtherm.rtherm7 3 2 =18  
 rtherm.rtherm8 2 tl =25  
 }

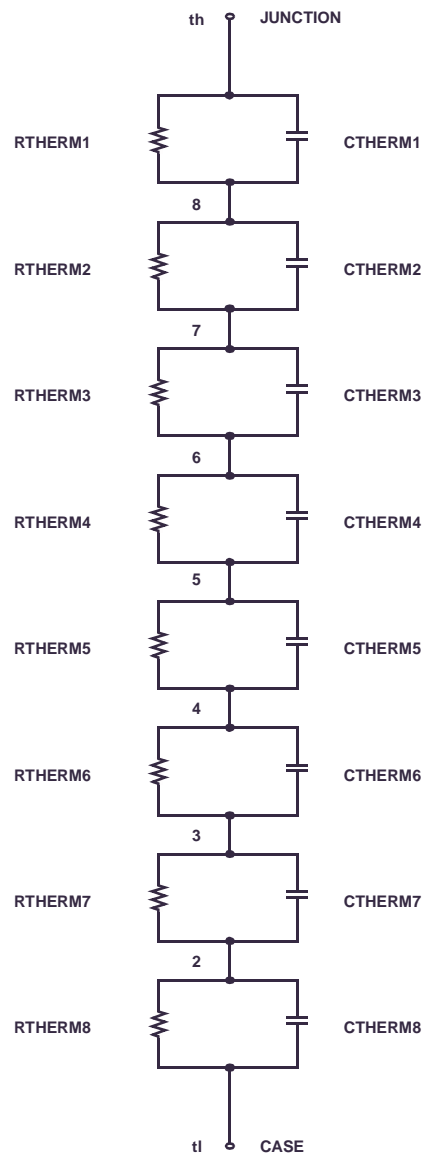


TABLE 1. THERMAL MODELS

COMPONANT	0.04 in <sup>2</sup>	0.28 in <sup>2</sup>	0.52 in <sup>2</sup>	0.76 in <sup>2</sup>	1.0 in <sup>2</sup>
C THERM6	1.2e-1	1.5e-1	2.0e-1	2.0e-1	2.0e-1
C THERM7	0.5	1.0	1.0	1.0	1.0
C THERM8	1.3	2.8	3.0	3.0	3.0
R THERM6	26	20	15	13	12
R THERM7	39	24	21	19	18
R THERM8	55	38.7	31.3	29.7	25

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CoolFET™	FPST™	LittleFET™	PowerSaver™	SuperSOT™-6
CROSSVOLT™	FRFET™	MICROCOUPLER™	PowerTrench®	SuperSOT™-8
DOVE™	GlobalOptoisolator™	MicroFET™	QFET®	SyncFET™
EcoSPARK™	GTO™	MicroPak™	QS™	TinyLogic®
E <sup>2</sup> CMOS™	HiSeC™	MICROWIRE™	QT Optoelectronics™	TINYOPTO™
EnSigna™	I <sup>2</sup> C™	MSX™	Quiet Series™	TruTranslation™
FACT™	<i>i-Lo</i> ™	MSXPro™	RapidConfigure™	UHC™
		OCX™	RapidConnect™	UltraFET®
Across the board. Around the world.™		OCXPro™	µSerDes™	UniFET™
The Power Franchise®		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	
		PACMAN™	SPM™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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