

# BF904; BF904R

N-channel dual gate MOS-FETs

Rev. 06 — 13 November 2007

Product data sheet

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NXP Semiconductors

# N-channel dual gate MOS-FETs

# BF904; BF904R

## FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

## APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

## DESCRIPTION

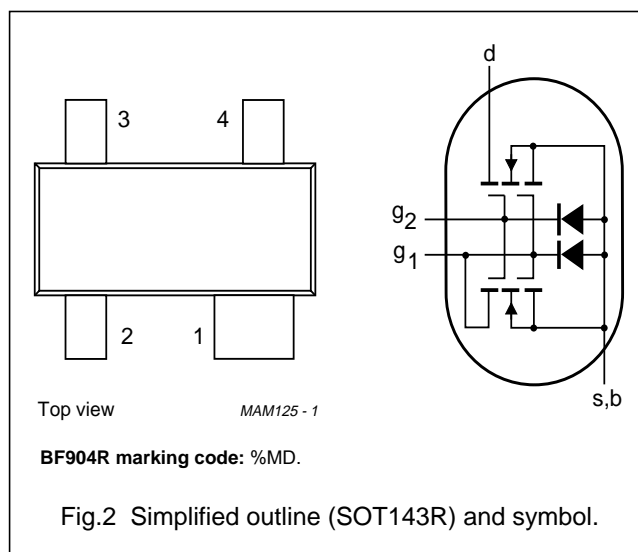
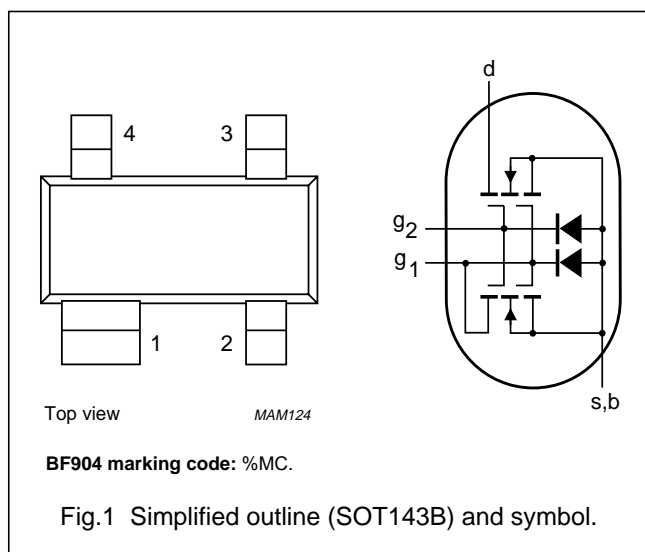
Enhancement type field-effect transistor in a plastic microminiature SOT143B and SOT143R package. The transistor consists of an amplifier MOS-FET with source

and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

<b>CAUTION</b>	
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.	

## PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g <sub>2</sub>	gate 2
4	g <sub>1</sub>	gate 1



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage		–	–	7	V
I <sub>D</sub>	drain current		–	–	30	mA
P <sub>tot</sub>	total power dissipation		–	–	200	mW
T <sub>j</sub>	operating junction temperature		–	–	150	°C
y <sub>fs</sub>	forward transfer admittance		22	25	30	mS
C <sub>ig1-s</sub>	input capacitance at gate 1		–	2.2	2.6	pF
C <sub>rs</sub>	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

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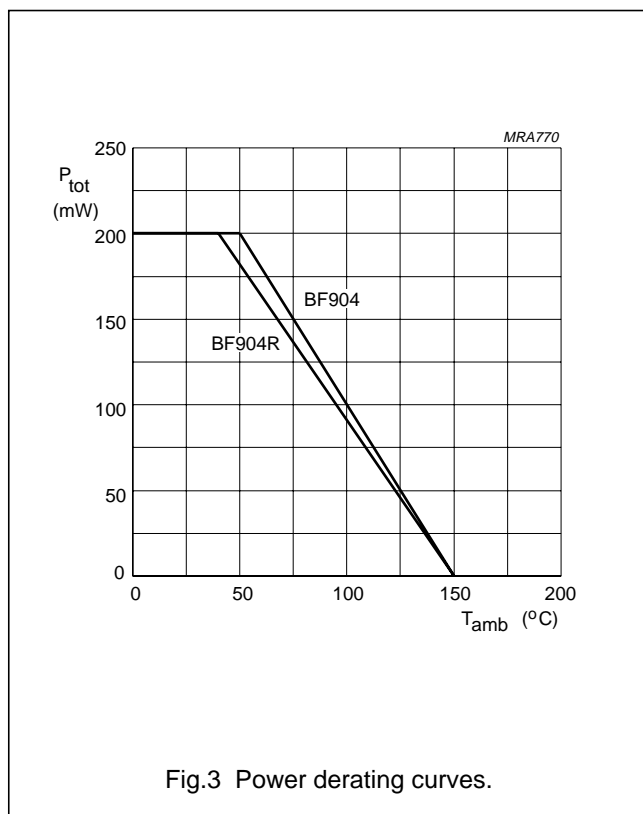
**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	7	V
$I_D$	drain current		–	30	mA
$I_{G1}$	gate 1 current		–	±10	mA
$I_{G2}$	gate 2 current		–	±10	mA
$P_{tot}$	total power dissipation BF904 BF904R	see Fig.3 $T_{amb} \leq 50\text{ °C}$ ; note 1 $T_{amb} \leq 40\text{ °C}$ ; note 1	– –	200 200	mW mW
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	operating junction temperature		–	150	°C

**Note**

1. Device mounted on a printed-circuit board.



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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	note 1	500	K/W
	BF904			
R <sub>th j-s</sub>	thermal resistance from junction to soldering point	note 2	290	K/W
	BF904			
	BF904R	T <sub>s</sub> = 78 °C	360	K/W

### Notes

1. Device mounted on a printed-circuit board.
2. T<sub>s</sub> is the temperature at the soldering point of the source lead.

## STATIC CHARACTERISTICS

T<sub>j</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>(BR)G1-SS</sub>	gate 1-source breakdown voltage	V <sub>G2-S</sub> = V <sub>DS</sub> = 0; I <sub>G1-S</sub> = 10 mA	6	15	V
V <sub>(BR)G2-SS</sub>	gate 2-source breakdown voltage	V <sub>G1-S</sub> = V <sub>DS</sub> = 0; I <sub>G2-S</sub> = 10 mA	6	15	V
V <sub>(F)S-G1</sub>	forward source-gate 1 voltage	V <sub>G2-S</sub> = V <sub>DS</sub> = 0; I <sub>S-G1</sub> = 10 mA	0.5	1.5	V
V <sub>(F)S-G2</sub>	forward source-gate 2 voltage	V <sub>G1-S</sub> = V <sub>DS</sub> = 0; I <sub>S-G2</sub> = 10 mA	0.5	1.5	V
V <sub>G1-S(th)</sub>	gate 1-source threshold voltage	V <sub>G2-S</sub> = 4 V; V <sub>DS</sub> = 5 V; I <sub>D</sub> = 20 μA	0.3	1	V
V <sub>G2-S(th)</sub>	gate 2-source threshold voltage	V <sub>G1-S</sub> = V <sub>DS</sub> = 5 V; I <sub>D</sub> = 20 μA	0.3	1.2	V
I <sub>DSX</sub>	drain-source current	V <sub>G2-S</sub> = 4 V; V <sub>DS</sub> = 5 V; R <sub>G1</sub> = 120 kΩ; note 1	8	13	mA
I <sub>G1-SS</sub>	gate 1 cut-off current	V <sub>G2-S</sub> = V <sub>DS</sub> = 0; V <sub>G1-S</sub> = 5 V	–	50	nA
I <sub>G2-SS</sub>	gate 2 cut-off current	V <sub>G1-S</sub> = V <sub>DS</sub> = 0; V <sub>G2-S</sub> = 5 V	–	50	nA

### Note

1. R<sub>G1</sub> connects gate 1 to V<sub>GG</sub> = 5 V; see Fig.20.

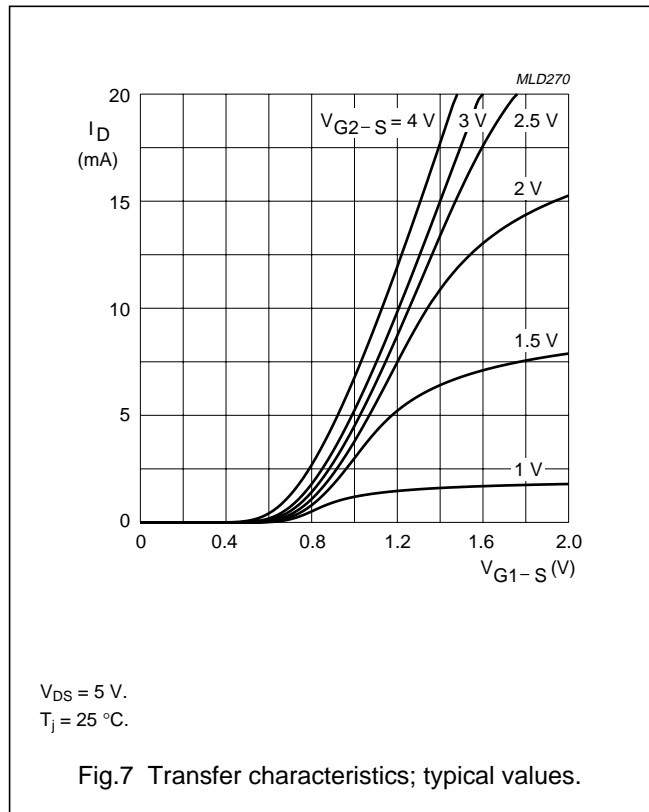
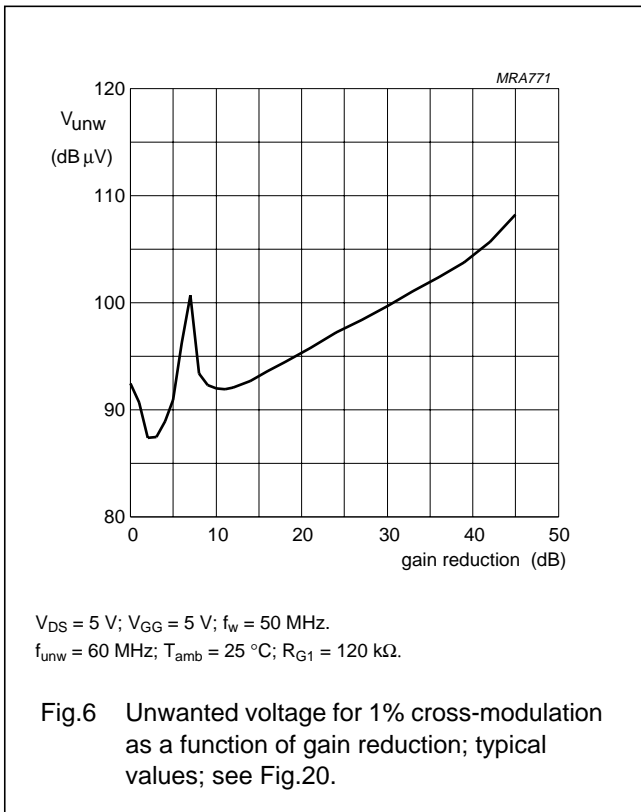
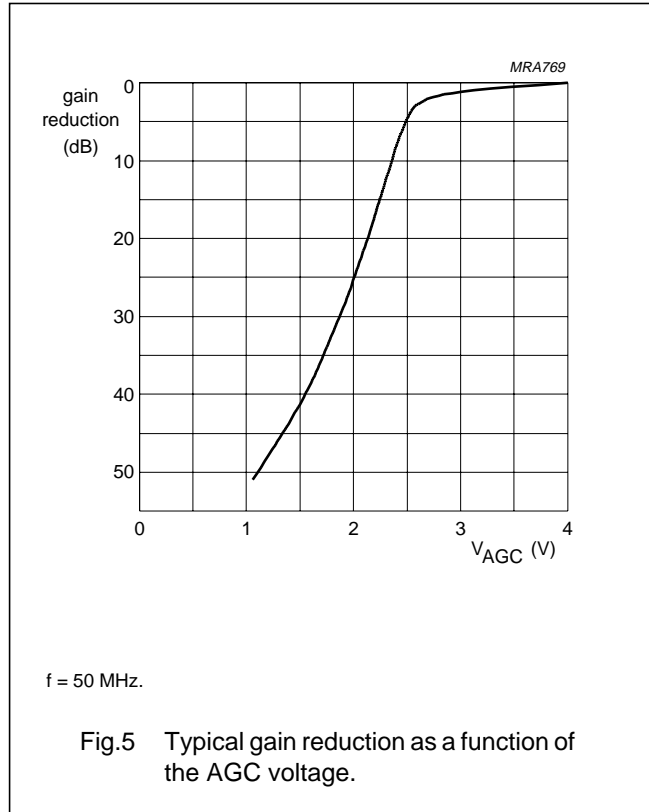
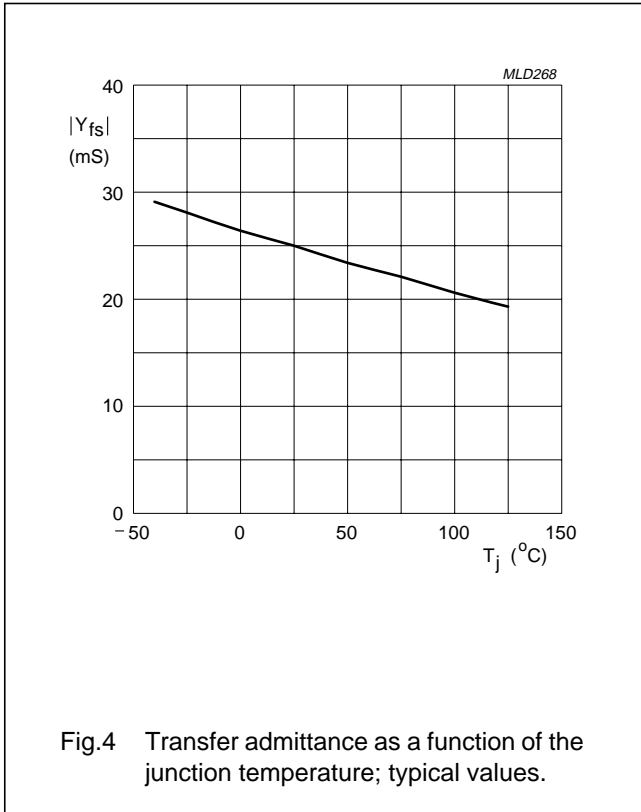
## DYNAMIC CHARACTERISTICS

Common source; T<sub>amb</sub> = 25 °C; V<sub>DS</sub> = 5 V; V<sub>G2-S</sub> = 4 V; I<sub>D</sub> = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
y <sub>fs</sub>	forward transfer admittance	pulsed; T <sub>j</sub> = 25 °C	22	25	30	mS
C <sub>ig1-s</sub>	input capacitance at gate 1	f = 1 MHz	–	2.2	2.6	pF
C <sub>ig2-s</sub>	input capacitance at gate 2	f = 1 MHz	1	1.5	2	pF
C <sub>os</sub>	drain-source capacitance	f = 1 MHz	1	1.3	1.6	pF
C <sub>rs</sub>	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 200 MHz; G <sub>S</sub> = 2 mS; B <sub>S</sub> = B <sub>Sopt</sub>	–	1	1.5	dB
		f = 800 MHz; G <sub>S</sub> = G <sub>Sopt</sub> ; B <sub>S</sub> = B <sub>Sopt</sub>	–	2	2.8	dB

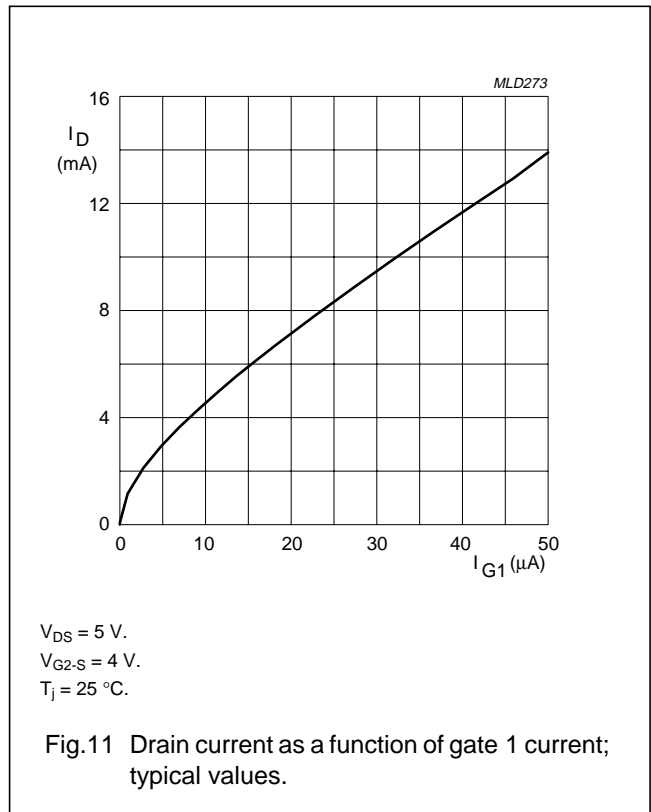
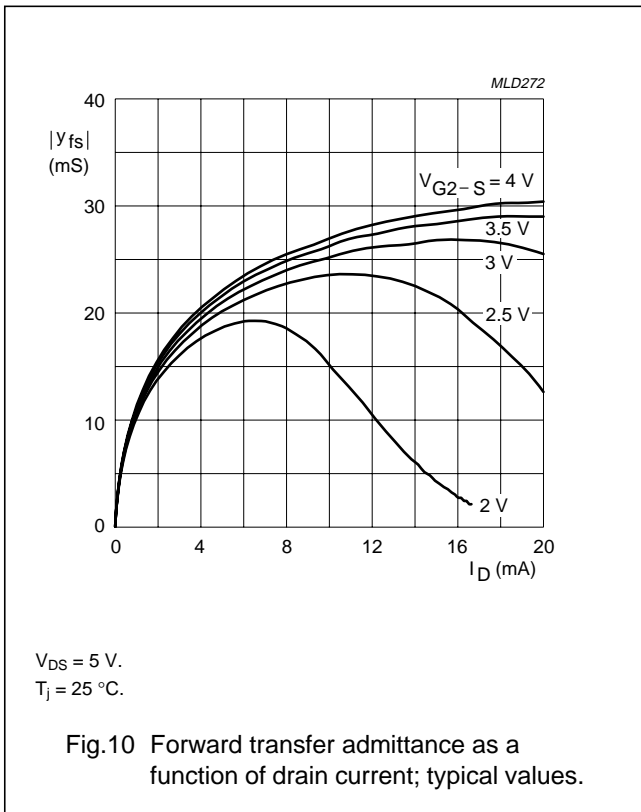
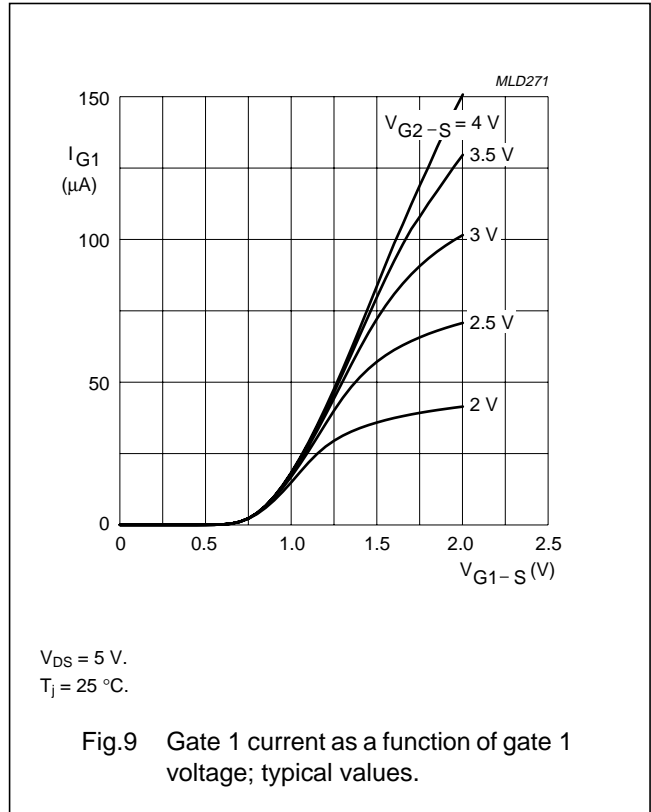
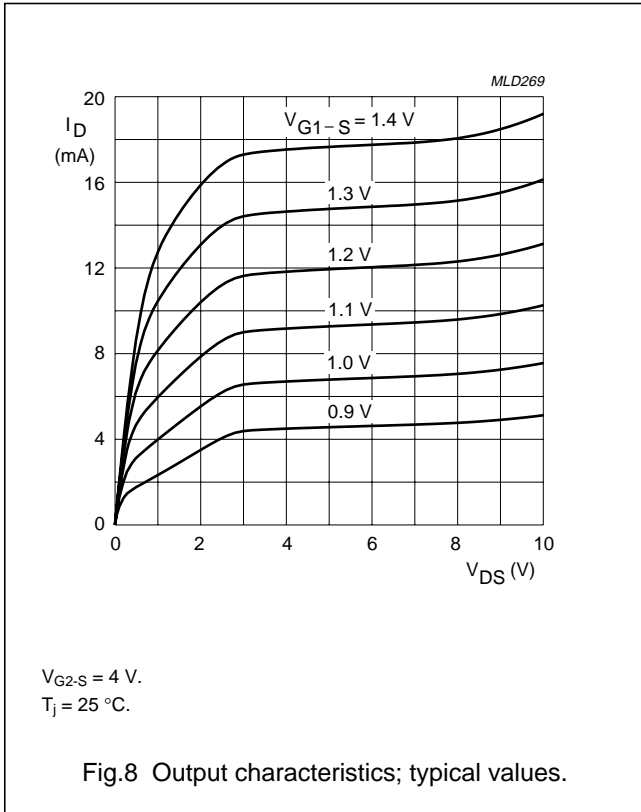
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BF904; BF904R



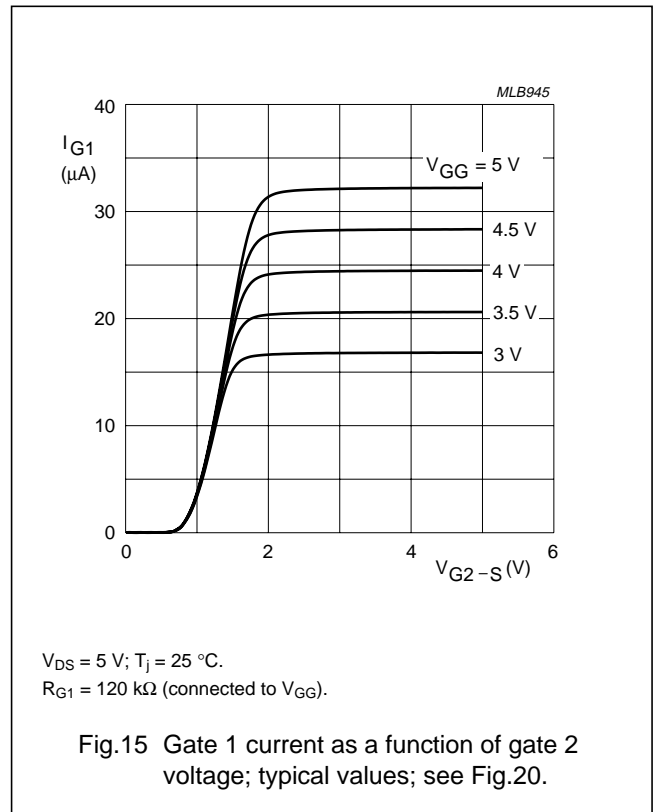
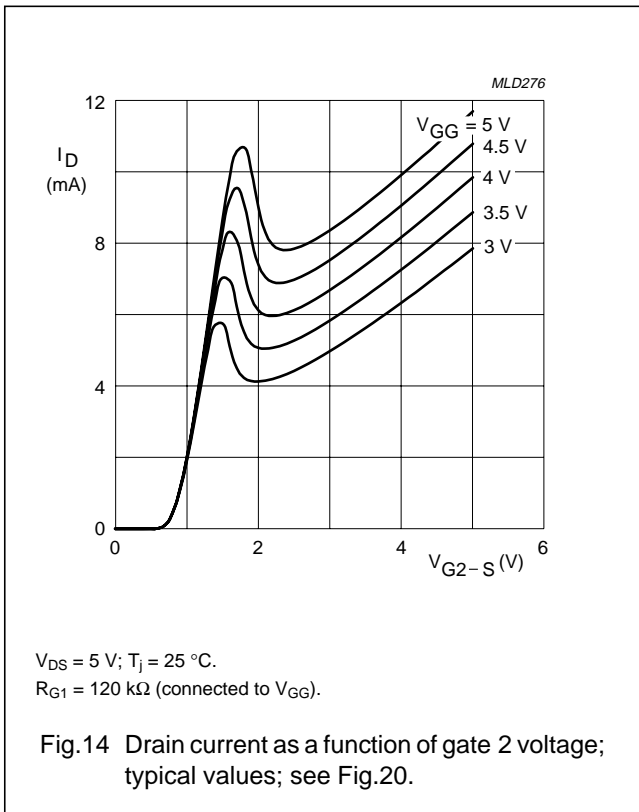
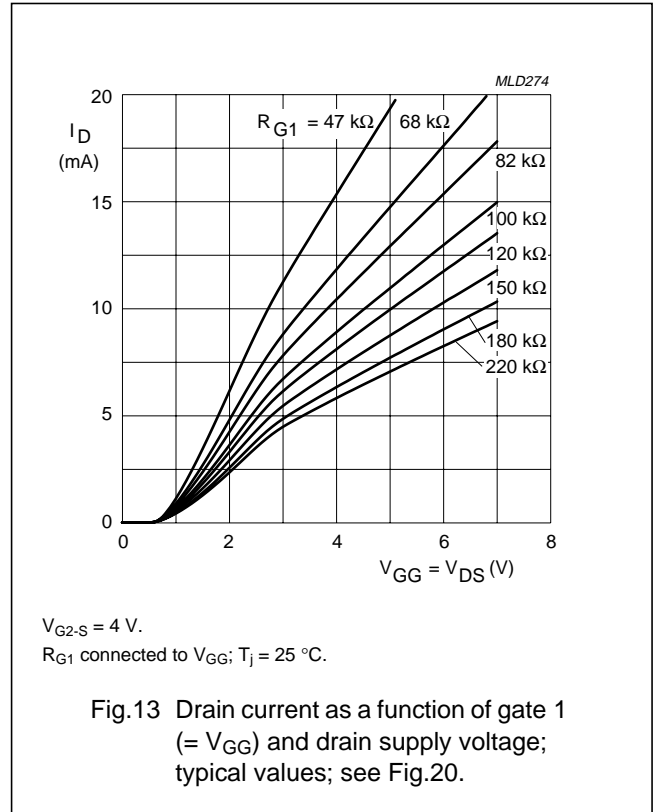
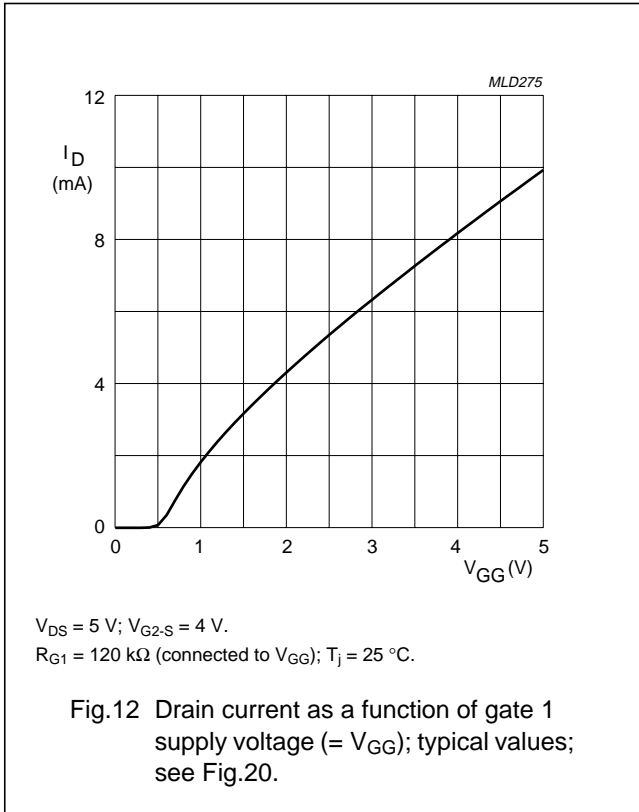
N-channel dual gate MOS-FETs

BF904; BF904R



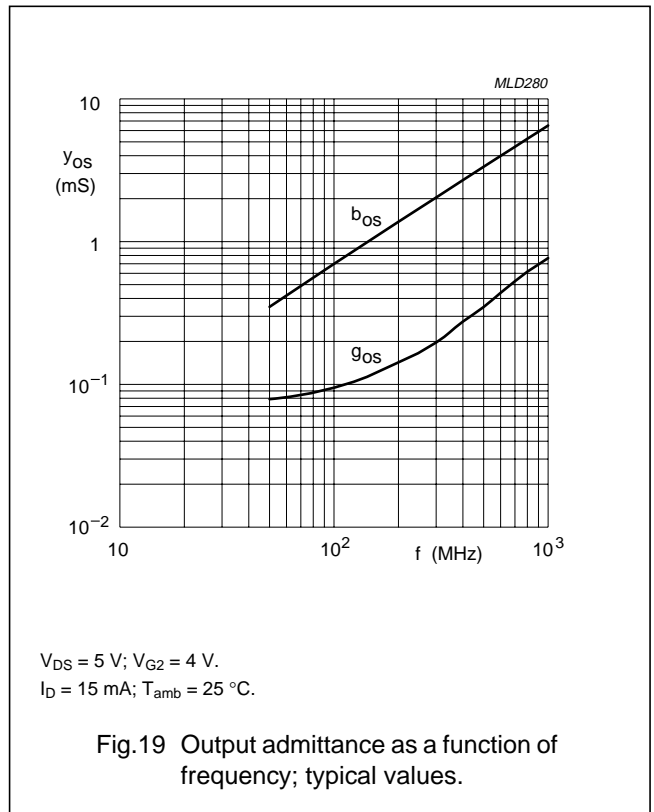
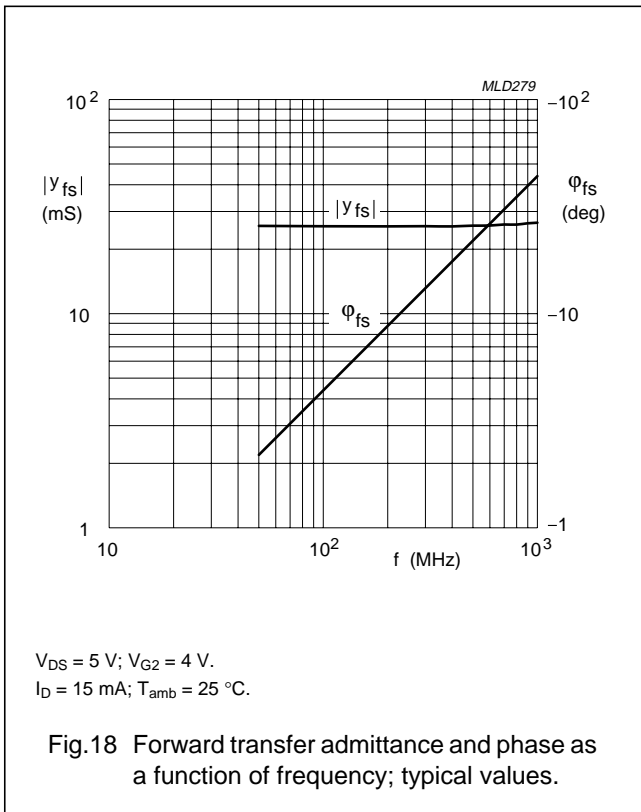
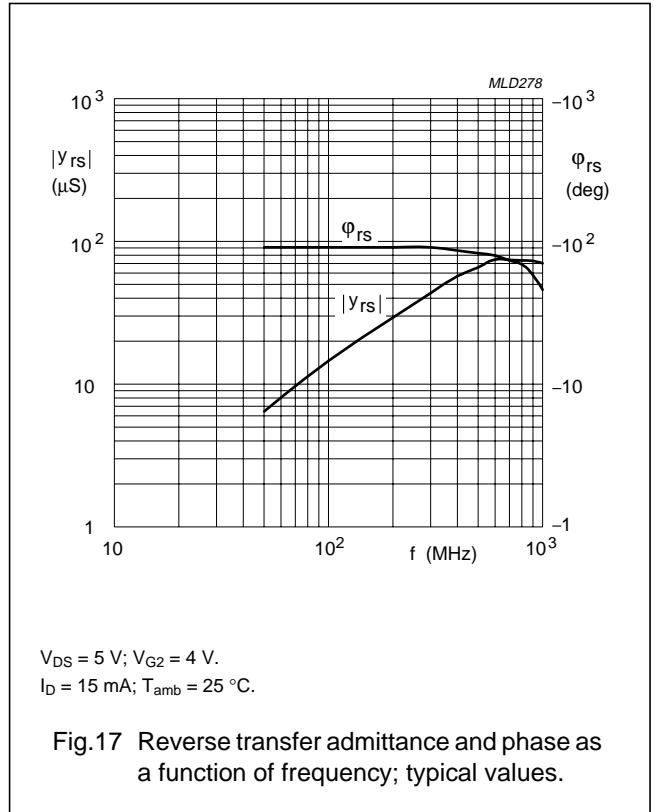
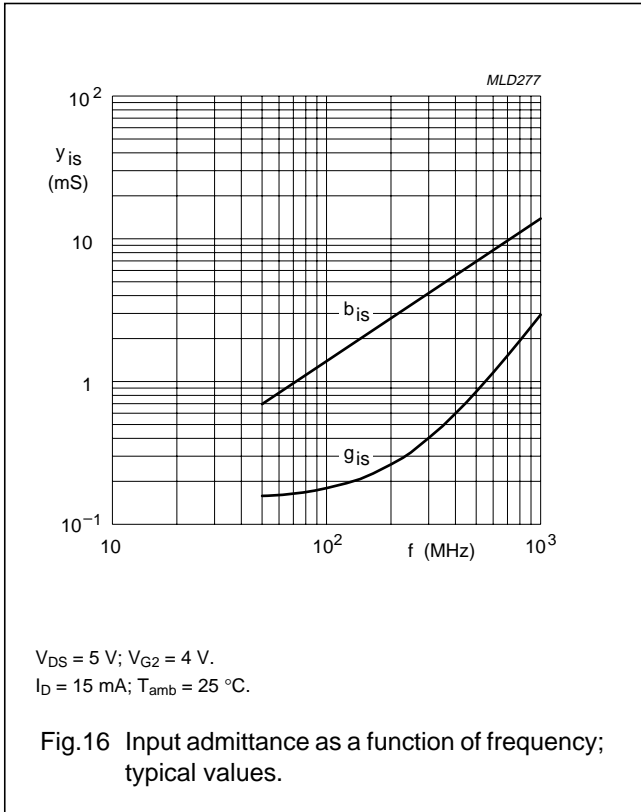
N-channel dual gate MOS-FETs

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N-channel dual gate MOS-FETs

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N-channel dual gate MOS-FETs

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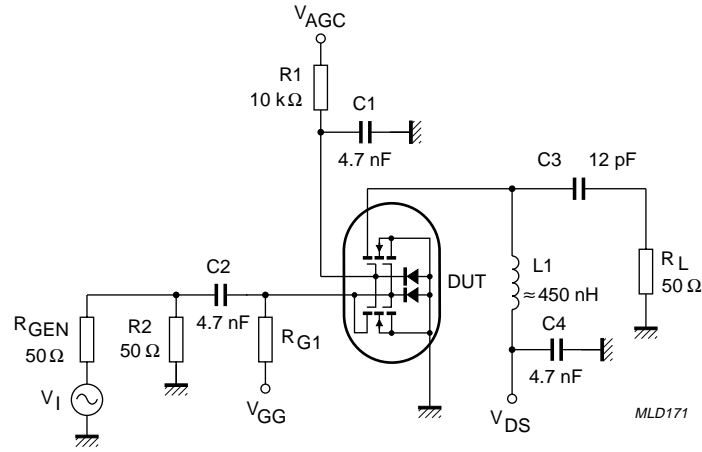


Fig.20 Cross-modulation test set-up.

## N-channel dual gate MOS-FETs

## BF904; BF904R

**Table 1** Scattering parameters:  $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 10\text{ mA}$ 

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.989	-3.4	2.420	175.7	0.000	79.9	0.993	-1.6
100	0.985	-8.3	2.414	169.1	0.001	78.3	0.992	-3.9
200	0.976	-16.4	2.368	158.8	0.003	80.3	0.987	-7.8
300	0.958	-24.1	2.301	148.5	0.004	73.7	0.980	-11.4
400	0.942	-32.0	2.251	138.8	0.005	70.7	0.974	-15.2
500	0.918	-39.3	2.170	129.5	0.005	67.2	0.966	-18.7
600	0.899	-46.0	2.080	120.7	0.005	67.8	0.958	-22.2
700	0.876	-52.6	2.001	112.1	0.005	68.6	0.951	-25.5
800	0.852	-58.8	1.924	103.2	0.005	72.9	0.944	-28.9
900	0.823	-64.9	1.829	94.7	0.005	78.7	0.937	-32.1
1000	0.800	-70.9	1.747	86.5	0.005	88.3	0.933	-35.2
1200	0.750	-82.4	1.621	70.7	0.005	120.5	0.928	-41.7
1400	0.719	-92.7	1.535	54.6	0.008	139.8	0.930	-48.4
1600	0.682	-102.5	1.424	39.4	0.010	137.8	0.924	-54.9
1800	0.642	-109.8	1.349	22.5	0.013	156.8	0.928	-62.9
2000	0.602	-116.5	1.283	1.1	0.018	175.1	0.928	-73.1
2200	0.547	-124.9	1.130	-15.1	0.014	172.6	0.887	-81.0
2400	0.596	-128.7	1.018	-49.1	0.040	-163.9	0.837	-95.8
2600	0.682	-132.6	0.979	-79.4	0.077	-164.0	0.778	-109.6
2800	0.771	-142.5	0.804	-116.2	0.120	178.8	0.629	-119.5
3000	0.793	-157.5	0.541	-153.5	0.149	158.3	0.479	-119.9

**Table 2** Noise data:  $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 10\text{ mA}$ 

f (MHz)	F <sub>min</sub> (dB)	Γ <sub>opt</sub>		r <sub>n</sub>
		(ratio)	(deg)	
800	2.00	0.686	49.6	50.40

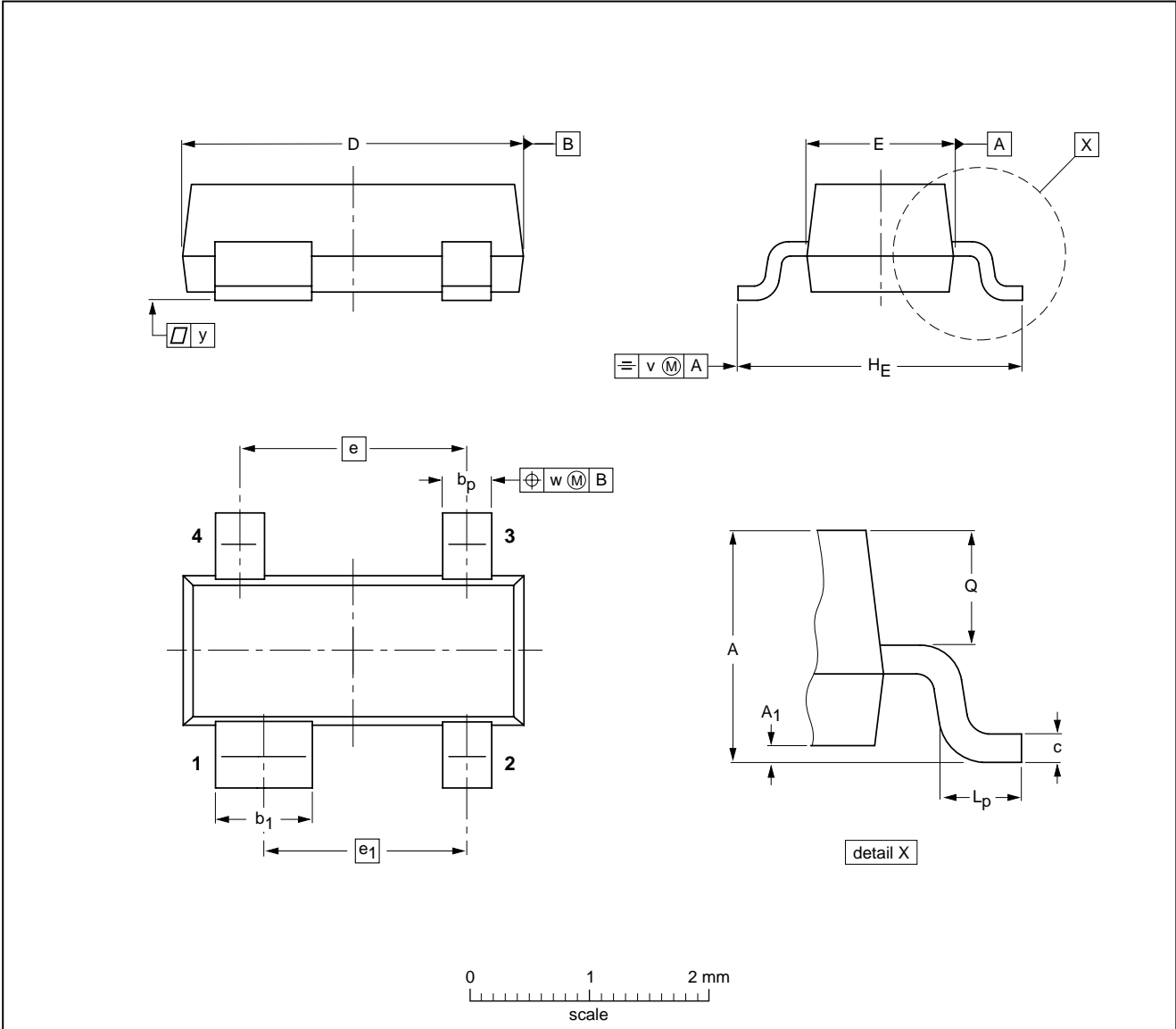
N-channel dual gate MOS-FETs

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PACKAGE OUTLINES

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

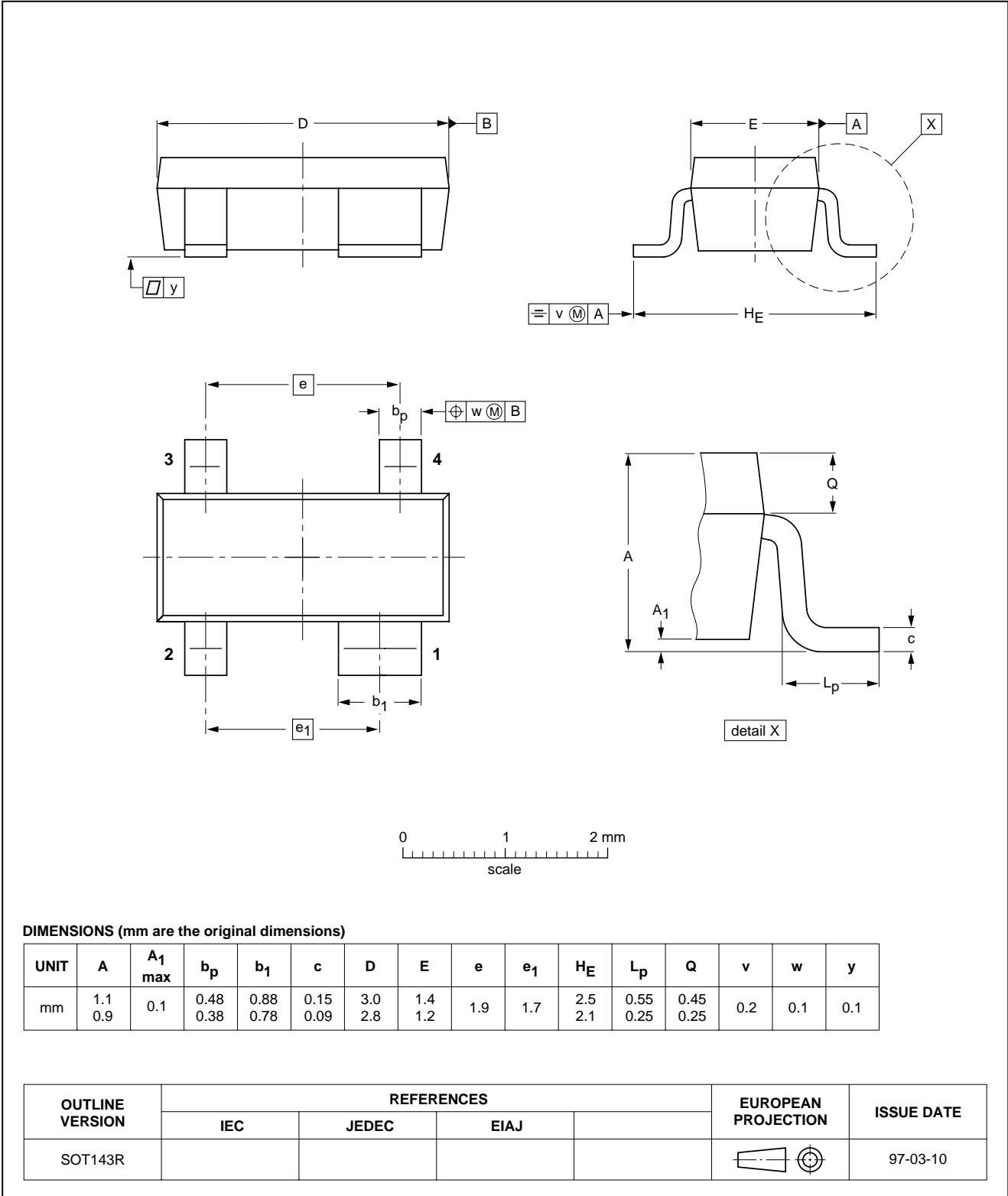
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

N-channel dual gate MOS-FETs

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Plastic surface mounted package; reverse pinning; 4 leads

SOT143R



## Legal information

### Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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## Revision history

### Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BF904_904R_N_6	20071113	Product data sheet	-	BF904_904R_5
Modifications:	<ul style="list-style-type: none"> <li>• Fig. 1 and 2 on page 2; Figure note changed</li> </ul>			
BF904_904R_5 (9397 750 05898)	19990517	Product specification	-	BF904R_4
BF904R_4 (9397 750 02668)	19970905	Product specification	-	BF904R_3
BF904R_3	19950425	Product specification	-	BF904R_2
BF904R_2	-	-	-	BF904R_1
BF904R_1	-	-	-	-

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