

### General Description

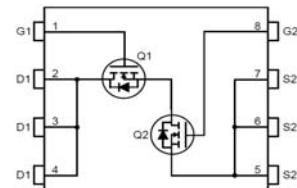
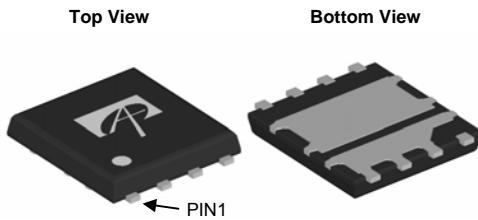
The AON6912A is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. It includes two specialized MOSFETs in a dual Power DFN5x6 package. The Q1 "High Side" MOSFET is designed to minimize switching losses. The Q2 "Low Side" MOSFET is designed for low  $R_{DS(ON)}$  to reduce conduction losses. The AON6912A is well suited for use in compact DC/DC converter applications.

### Product Summary

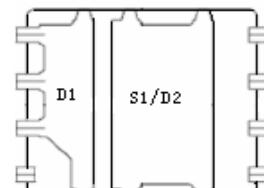
	<u>Q1</u>	<u>Q2</u>
$V_{DS}$	30V	30V
$I_D$ (at $V_{GS}=10V$ )	21A	52A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	<13.7mΩ	<7.3mΩ
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$ )	<19.3mΩ	<10.4mΩ
100% UIS Tested		
100% $R_g$ Tested		



DFN5x6



Top View



Bottom View

### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage	$V_{DS}$	30		V
Gate-Source Voltage	$V_{GS}$	$\pm 20$		V
Continuous Drain Current	$T_C=25^\circ C$	$I_D$	21	A
Current			13	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	56	130	
Continuous Drain Current	$T_A=25^\circ C$	$I_{DSM}$	9	A
Current			7.1	
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	18	28	A
Avalanche Energy L=0.1mH <sup>C</sup>	$E_{AS}, E_{AR}$	16	80	mJ
Power Dissipation <sup>B</sup>	$T_C=25^\circ C$	$P_D$	11	W
			4.4	
Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	$P_{DSM}$	1.9	W
			1.2	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient <sup>A</sup>	$t \leq 10s$	$R_{0JA}$	29	24	35	°C/W
Maximum Junction-to-Ambient <sup>AD</sup>	Steady-State		56	50	67	°C/W
Maximum Junction-to-Case	Steady-State	$R_{0JC}$	9.5	3.5	11.4	°C/W

**Q1 Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30			V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}= \pm 20\text{V}$			100	nA
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.1	1.6	2.1	V
$I_{\text{D}(\text{ON})}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	56			A
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=10\text{A}$ $T_J=125^\circ\text{C}$		11.4 17.9	13.7 21.5	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=10\text{A}$		15.4	19.3	$\text{m}\Omega$
$g_{\text{FS}}$	Forward Transconductance	$V_{DS}=5\text{V}, I_D=10\text{A}$		35		S
$V_{\text{SD}}$	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.75	1	V
$I_S$	Maximum Body-Diode Continuous Current				15	A
<b>DYNAMIC PARAMETERS</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$	460	580	700	pF
$C_{\text{oss}}$	Output Capacitance		70	100	130	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		40	65	90	pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	0.4	0.8	1.2	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=10\text{A}$	8.2	10.2	12.5	nC
$Q_g(4.5\text{V})$	Total Gate Charge		3.7	4.6	5.5	nC
$Q_{\text{gs}}$	Gate Source Charge		1.7	2.1	2.5	nC
$Q_{\text{gd}}$	Gate Drain Charge		1.4	2.4	3.4	nC
$t_{\text{D}(\text{on})}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=1.5\Omega, R_{\text{GEN}}=3\Omega$		4		ns
$t_r$	Turn-On Rise Time			2		ns
$t_{\text{D}(\text{off})}$	Turn-Off DelayTime			18.5		ns
$t_f$	Turn-Off Fall Time			2.2		ns
$t_{\text{rr}}$	Body Diode Reverse Recovery Time	$I_F=10\text{A}, dI/dt=500\text{A}/\mu\text{s}$	5.8	7.3	8.8	ns
$Q_{\text{rr}}$	Body Diode Reverse Recovery Charge	$I_F=10\text{A}, dI/dt=500\text{A}/\mu\text{s}$	6.2	7.8	9.4	nC

A. The value of  $R_{\text{JJA}}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{\text{DSM}}$  is based on  $R_{\text{JJA}}$  and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation  $P_D$  is based on  $T_{J(\text{MAX})}=150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(\text{MAX})}=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .

D. The  $R_{\text{JJA}}$  is the sum of the thermal impedance from junction to case  $R_{\text{JJC}}$  and case to ambient.

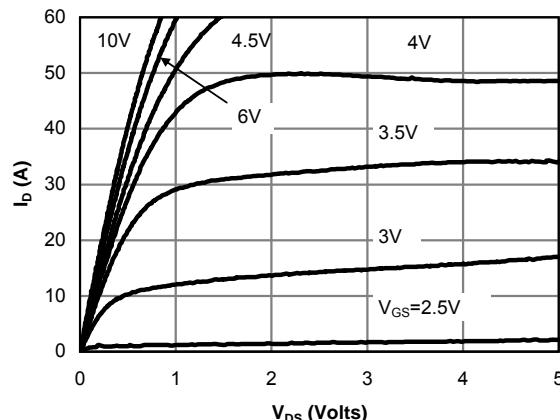
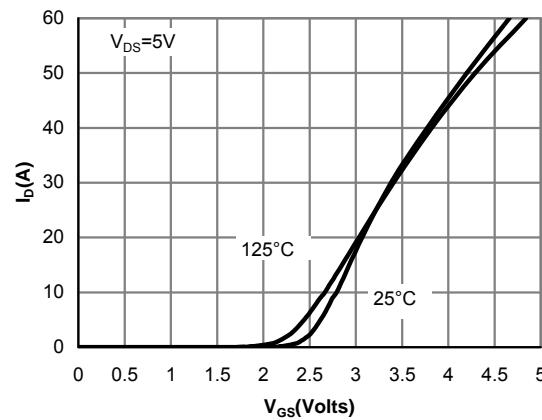
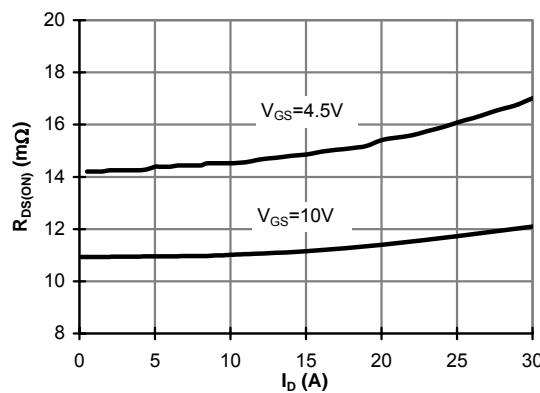
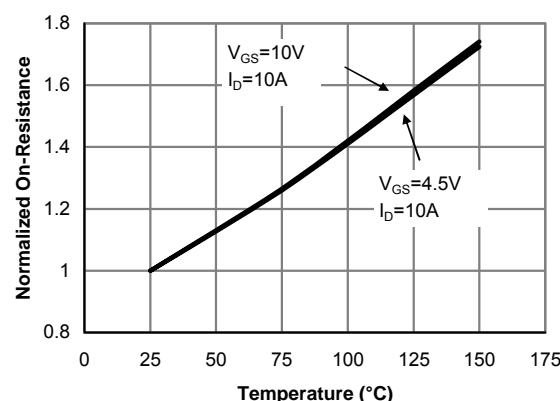
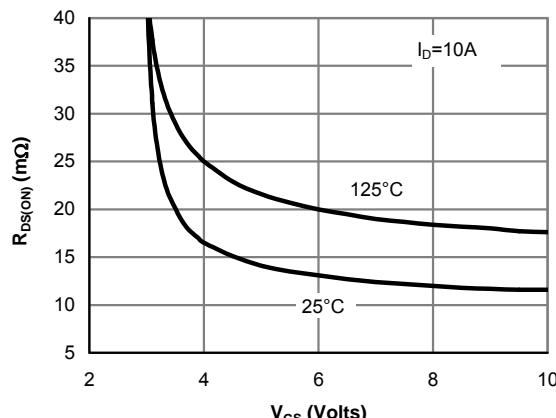
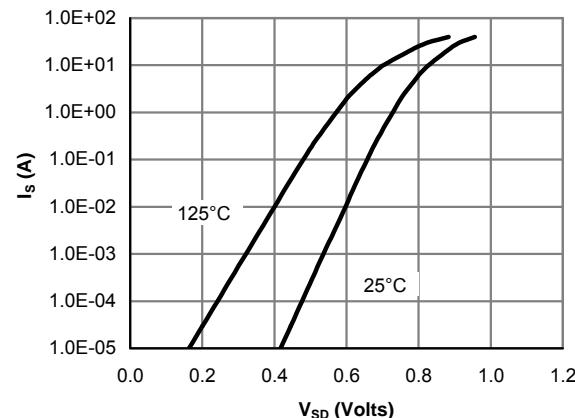
E. The static characteristics in Figures 1 to 6 are obtained using <300  $\mu\text{s}$  pulses, duty cycle 0.5% max.

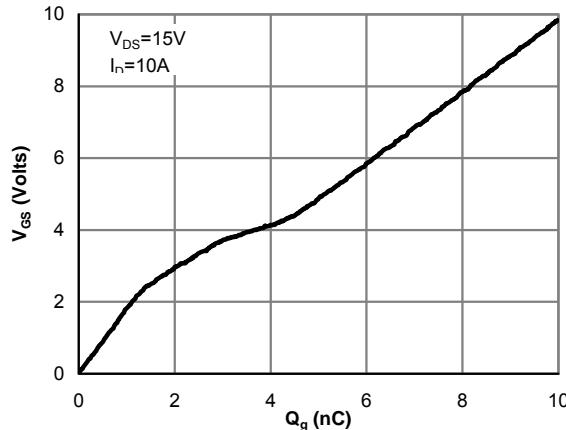
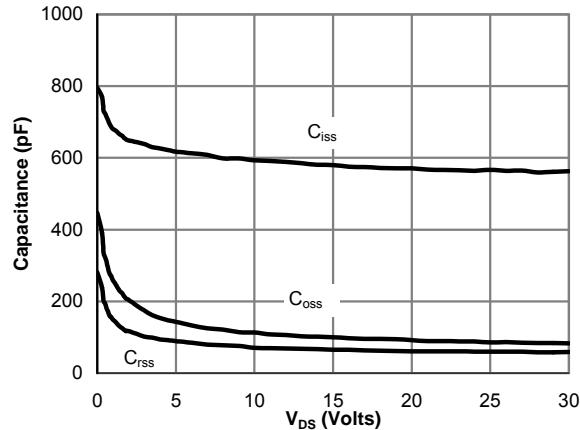
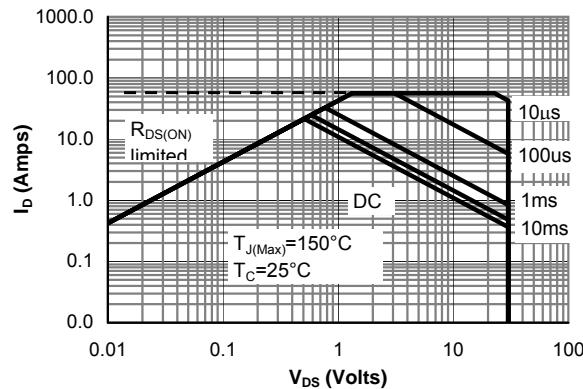
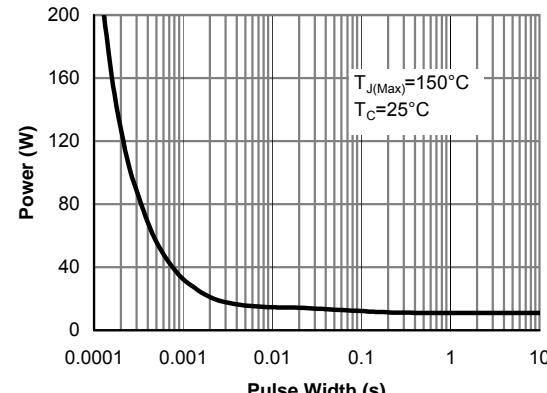
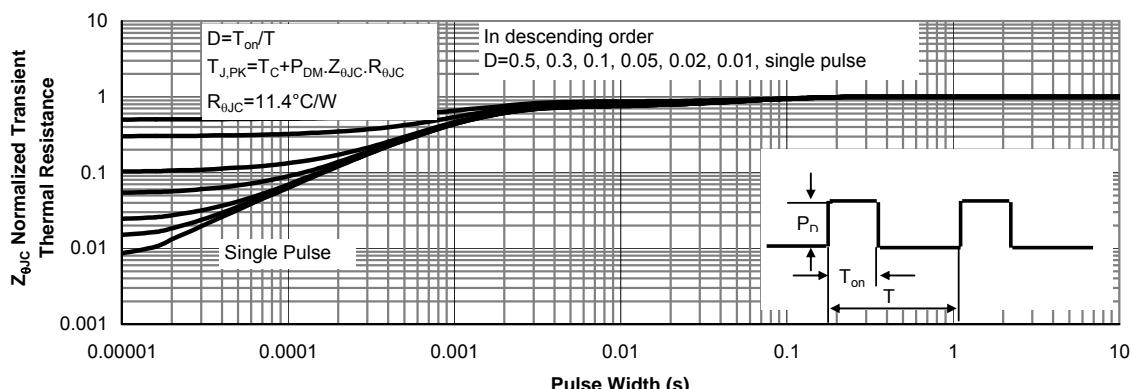
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(\text{MAX})}=150^\circ\text{C}$ . The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ .

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**Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Fig 1: On-Region Characteristics (Note E)**

**Figure 2: Transfer Characteristics (Note E)**

**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

**Figure 6: Body-Diode Characteristics (Note E)**

**Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 7: Gate-Charge Characteristics**

**Figure 8: Capacitance Characteristics**

**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

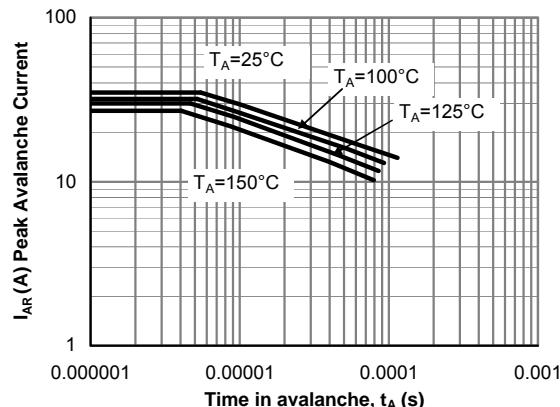
**Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Figure 12: Single Pulse Avalanche capability (Note C)

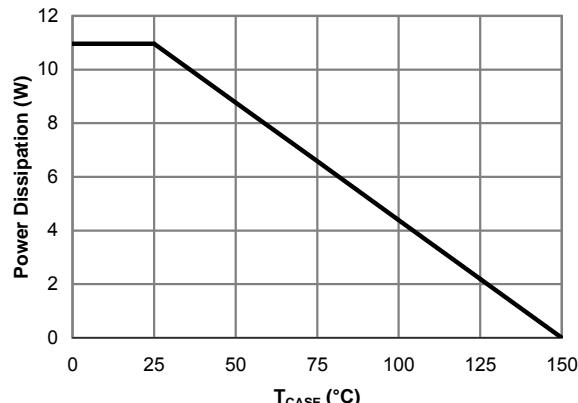


Figure 13: Power De-rating (Note F)

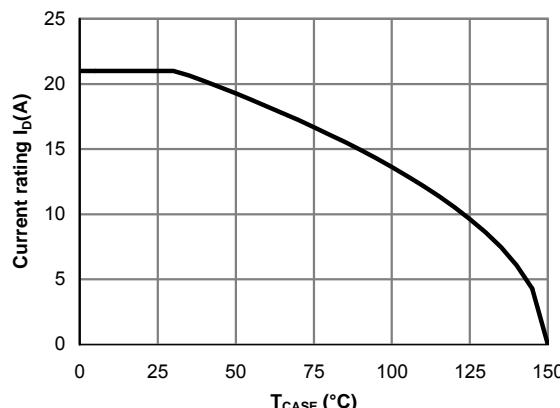


Figure 14: Current De-rating (Note F)

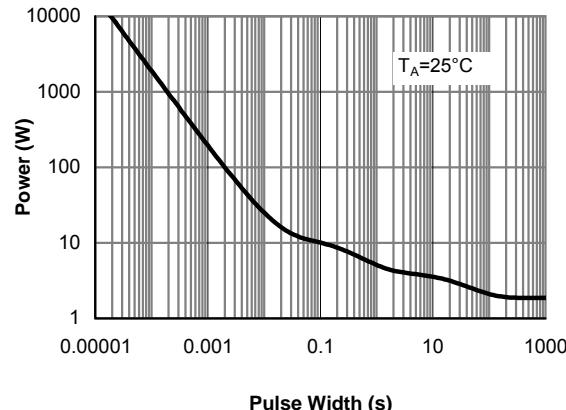


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

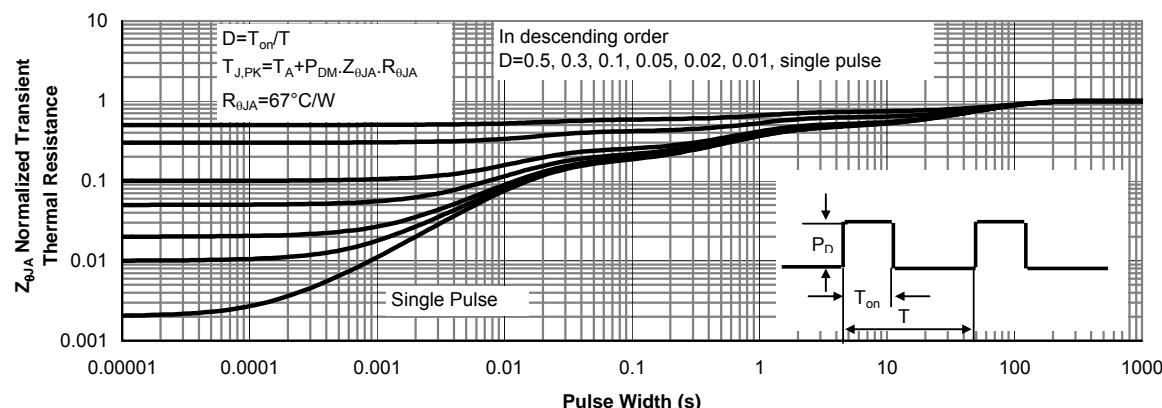


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

**Q2 Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30			V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}= \pm 20\text{V}$			100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.3	1.9	2.5	V
$I_{\text{D(ON)}}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	130			A
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$ $T_J=125^\circ\text{C}$		6.1 8.5	7.3 10.2	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=20\text{A}$		8.3	10.4	$\text{m}\Omega$
$g_{\text{FS}}$	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		60		S
$V_{\text{SD}}$	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.7	1	V
$I_S$	Maximum Body-Diode Continuous Current				35	A
<b>DYNAMIC PARAMETERS</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$	870	1090	1300	pF
$C_{\text{oss}}$	Output Capacitance		340	490	640	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		22	38	53	pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	0.4	0.9	1.4	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=20\text{A}$	12	16	20	nC
$Q_g(4.5\text{V})$	Total Gate Charge		5	7	9	nC
$Q_{\text{gs}}$	Gate Source Charge		2	2.5	3	nC
$Q_{\text{gd}}$	Gate Drain Charge		1.5	2.5	3.5	nC
$t_{\text{D(on)}}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=0.75\Omega, R_{\text{GEN}}=3\Omega$		5		ns
$t_r$	Turn-On Rise Time			2		ns
$t_{\text{D(off)}}$	Turn-Off DelayTime			16		ns
$t_f$	Turn-Off Fall Time			2		ns
$t_{\text{rr}}$	Body Diode Reverse Recovery Time	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$	10	13	16	ns
$Q_{\text{rr}}$	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$	20	25	30	nC

A. The value of  $R_{\text{JJA}}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{\text{DSM}}$  is based on  $R_{\text{JJA}}$  and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation  $P_D$  is based on  $T_{J(\text{MAX})}=150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(\text{MAX})}=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .

D. The  $R_{\text{JJA}}$  is the sum of the thermal impedance from junction to case  $R_{\text{JJC}}$  and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300  $\mu\text{s}$  pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(\text{MAX})}=150^\circ\text{C}$ . The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ .

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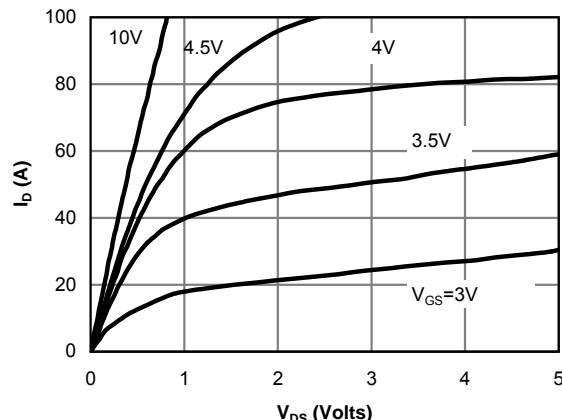
**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Fig 1: On-Region Characteristics (Note E)

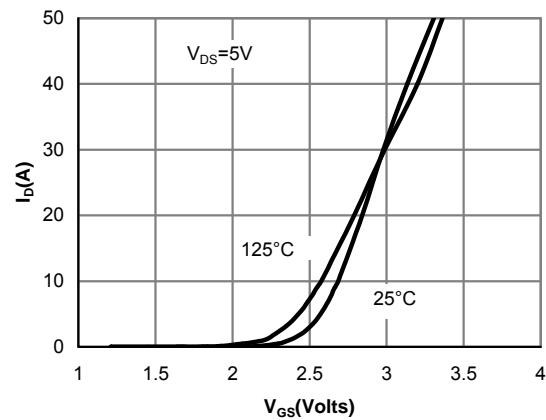


Figure 2: Transfer Characteristics (Note E)

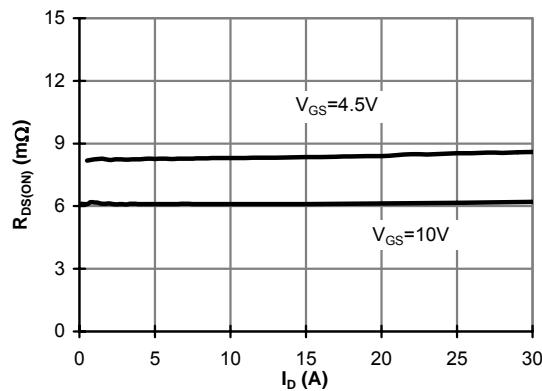


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

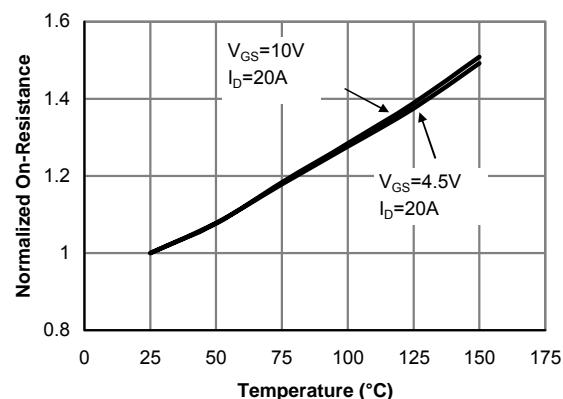


Figure 4: On-Resistance vs. Junction Temperature (Note E)

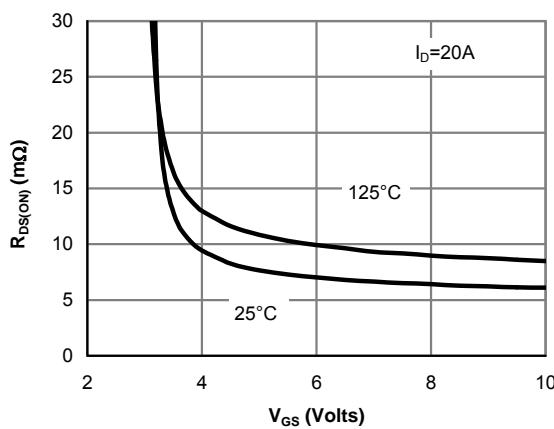


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

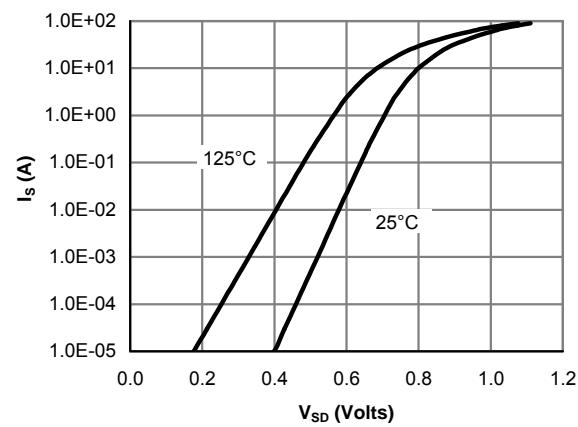
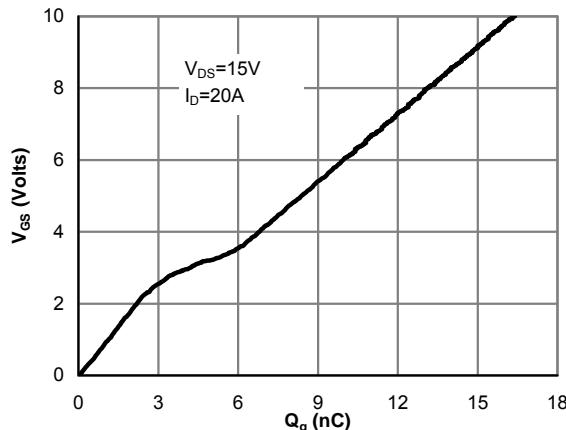
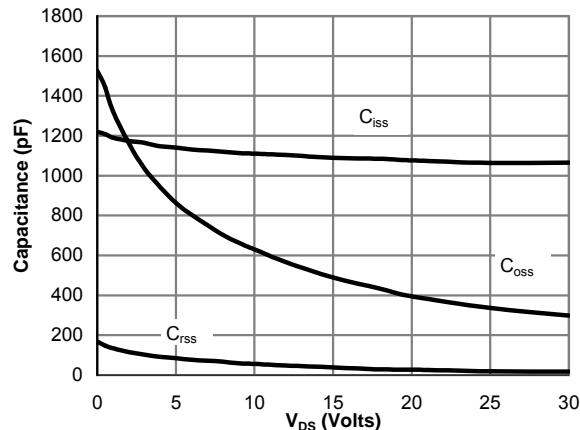
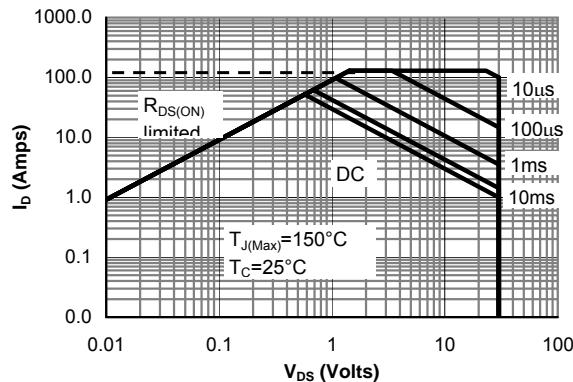
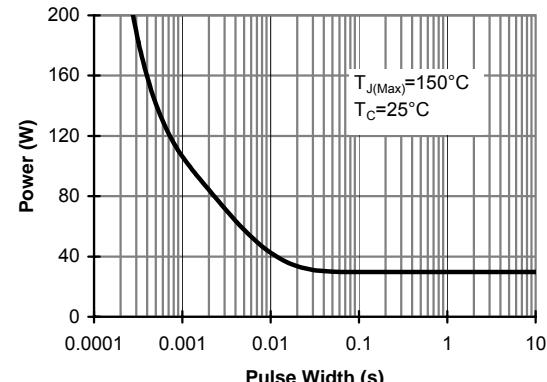
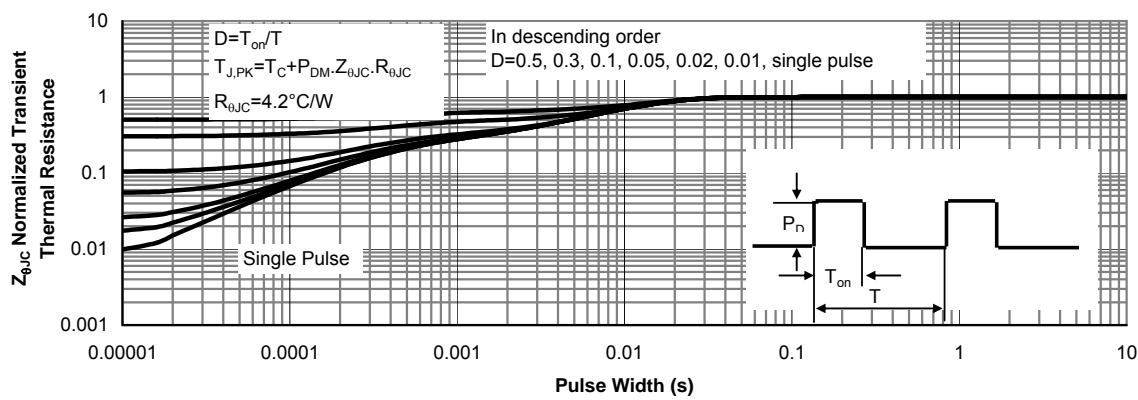


Figure 6: Body-Diode Characteristics (Note E)

**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 7: Gate-Charge Characteristics**

**Figure 8: Capacitance Characteristics**

**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

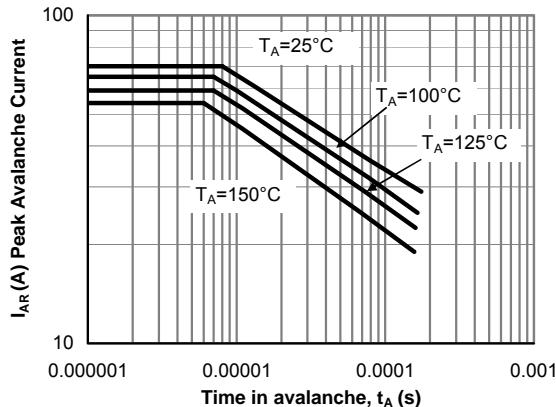
**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Figure 12: Single Pulse Avalanche capability (Note C)

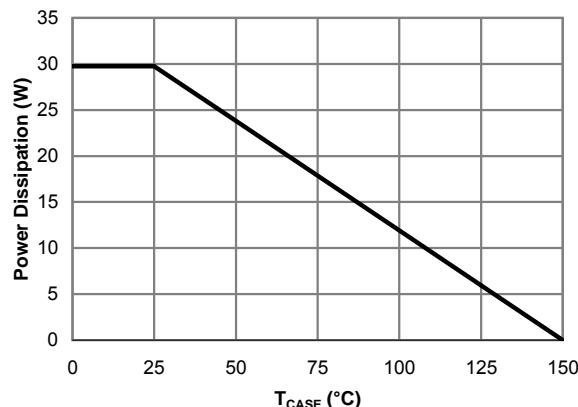


Figure 13: Power De-rating (Note F)

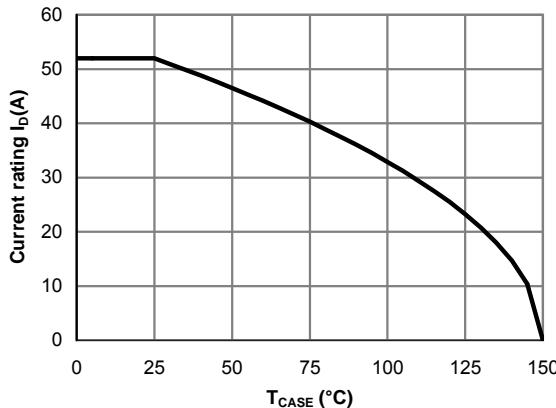


Figure 14: Current De-rating (Note F)

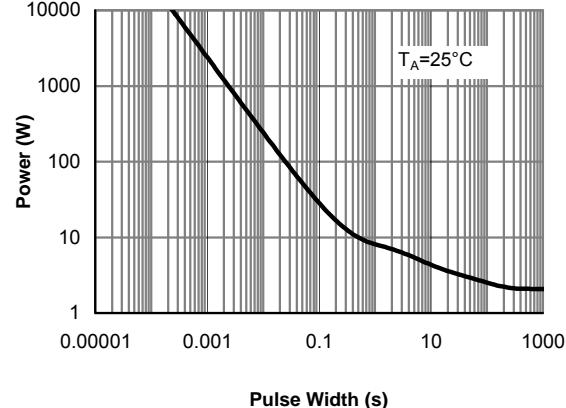


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

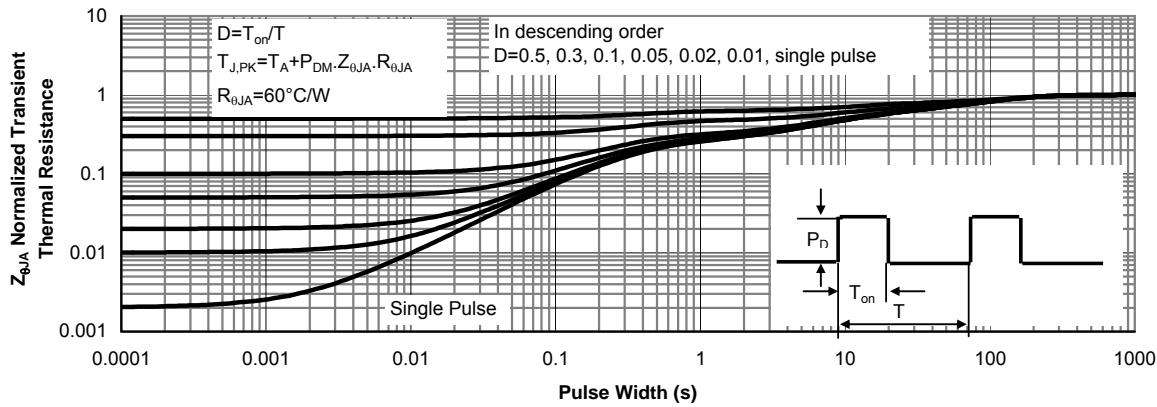
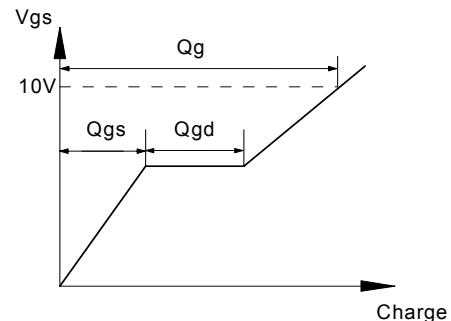
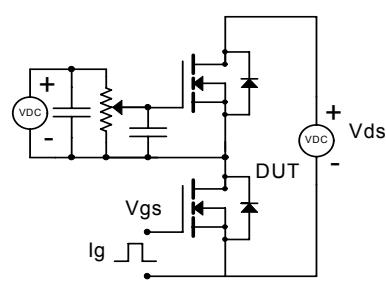
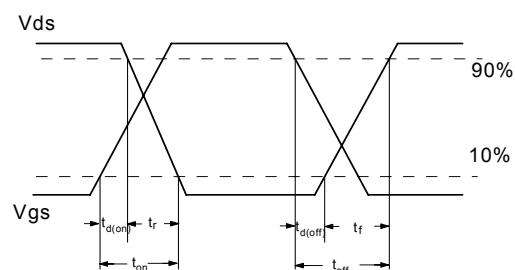
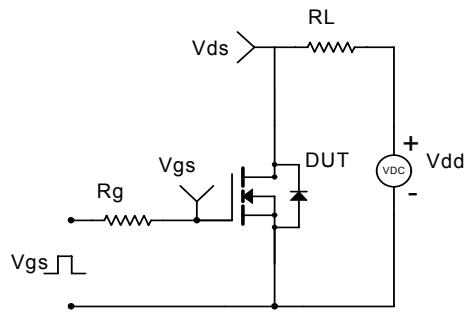
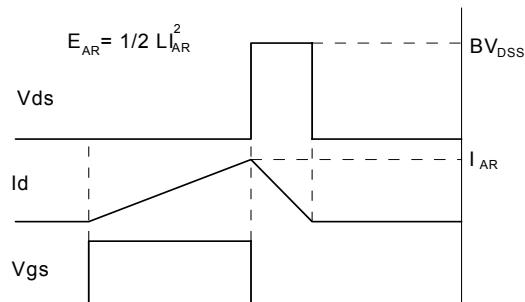
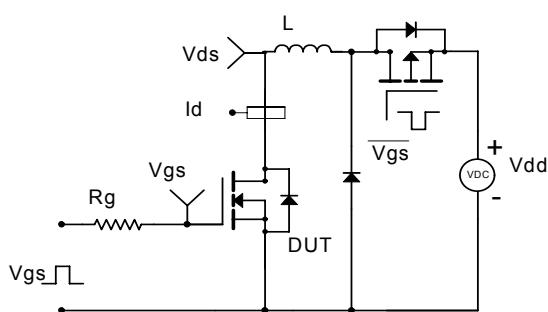


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

**Gate Charge Test Circuit & Waveform**

**Resistive Switching Test Circuit & Waveforms**

**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

**Diode Recovery Test Circuit & Waveforms**
