FAIRCHILD
SEMICONDUCTOR®

February 2008

Motion-SPM™

FSBB20CH60C
Smart Power Module

Features

- UL Certified No.E209204(SPM27-CC package)
- Very low thermal resistance due to using DBC
- Easy PCB layout due to built in bootstrap diode
- 600V-20A 3-phase IGBT inverter bridge including control ICs for gate driving and protection
- Divided negative dc-link terminals for inverter current sensing applications
- Single-grounded power supply due to built-in HVIC
- Isolation rating of 2500Vrms/min.

Applications

- AC 100V ~ 253V three-phase inverter drive for small power ac motor drives
- Home appliances applications like air conditioner and washing machine

General Description

It is an advanced motion-smart power module (Motion-SPM™) that Fairchild has newly developed and designed to provide very compact and high performance ac motor drives mainly targeting low-power inverter-driven application like air conditioner and washing machine. It combines optimized circuit protection and drive matched to low-loss IGBTs. System reliability is further enhanced by the integrated under-voltage lock-out and short-circuit protection. The high speed built-in HVIC provides opto-coupler-less single-supply IGBT gate driving capability that further reduce the overall size of the inverter system design. Each phase current of inverter can be monitored separately due to the divided negative dc terminals.

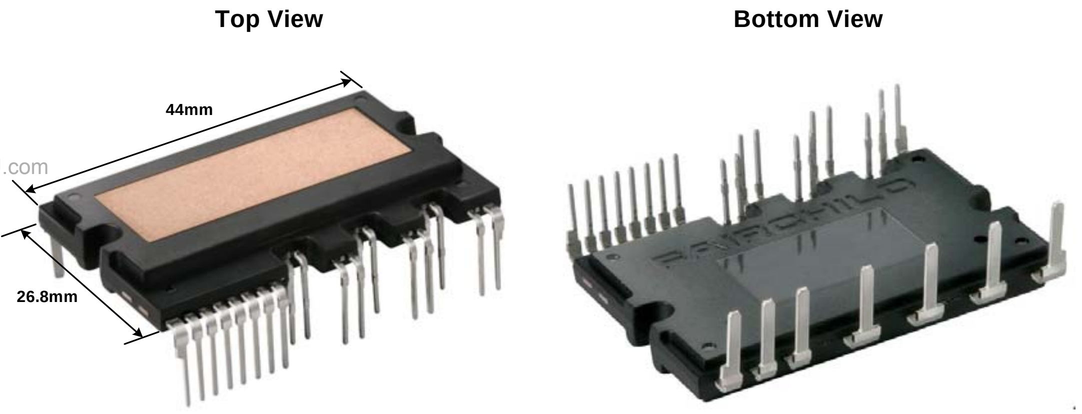

Top View
Bottom View

Figure 1.

Integrated Power Functions

- 600V-20A IGBT inverter for three-phase DC/AC power conversion (Please refer to Figure 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting
  Control circuit under-voltage (UV) protection
  Note) Available bootstrap circuit example is given in Figures 12 and 13.
- For inverter low-side IGBTs: Gate drive circuit, Short circuit protection (SC)
  Control supply circuit under-voltage (UV) protection
- Fault signaling: Corresponding to UV (Low-side supply) and SC faults
- Input interface: 3.3/5V CMOS/LSTTL compatible, Schmitt trigger input

Pin Configuration

Top View

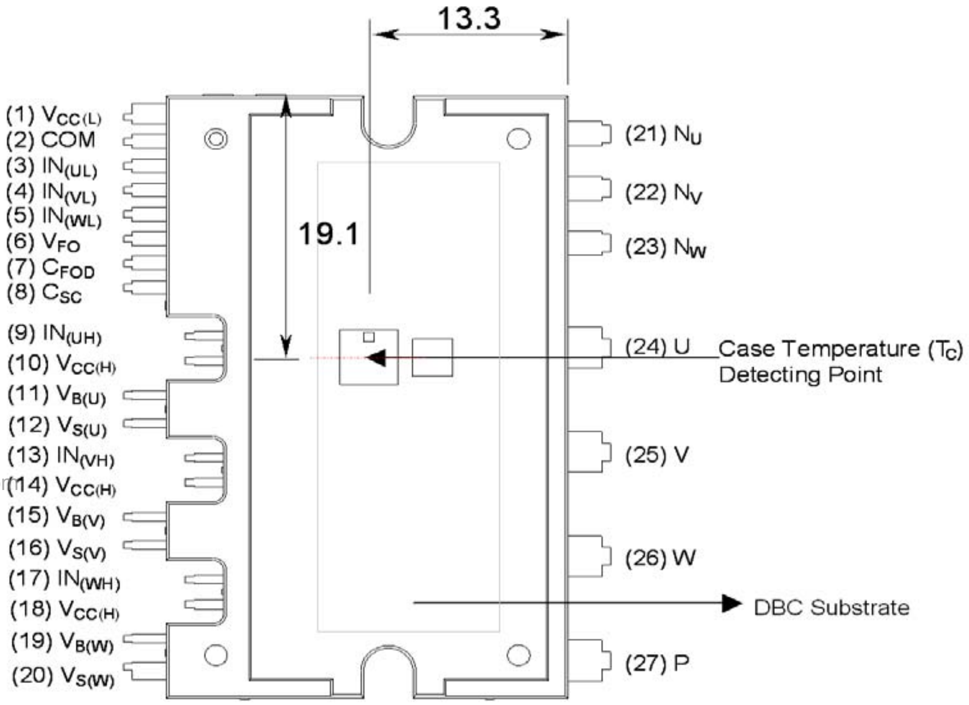
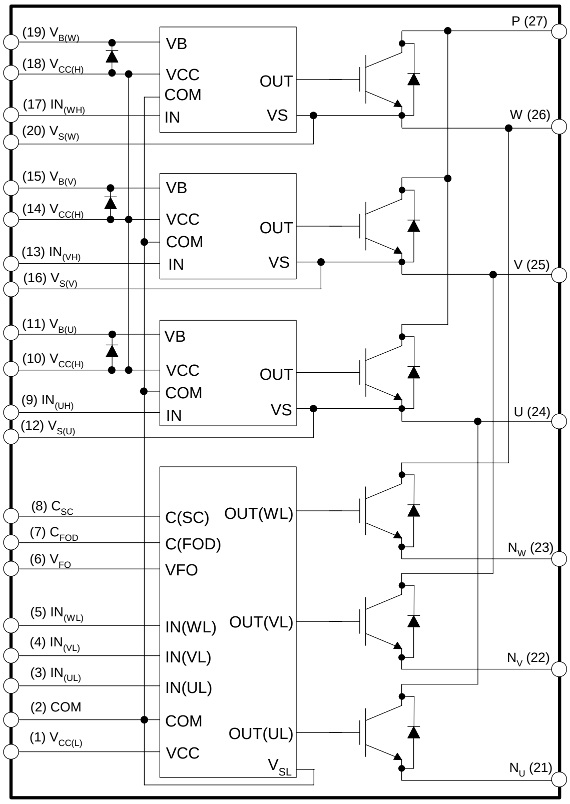

13.3
19.1
(1) VCC(L)
(2) COM
(3) IN(UL)
(4) IN(VL)
(5) IN(WL)
(6) VFO
(7) CFOD
(8) CSC
(9) IN(UH)
(10) VCC(H)
(11) VB(U)
(12) VS(U)
(13) IN(VH)
(14) VCC(H)
(15) VB(V)
(16) VS(V)
(17) IN(WH)
(18) VCC(H)
(19) VB(W)
(20) VS(W)
(21) NU
(22) NV
(23) NW
(24) U
(25) V
(26) W
(27) P
Case Temperature (TC) Detecting Point
DBC Substrate

Figure 2.

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-side U Phase
4	$IN_{(VL)}$	Signal Input for Low-side V Phase
5	$IN_{(WL)}$	Signal Input for Low-side W Phase
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault Output Duration Time Selection
8	C_{SC}	Capacitor (Low-pass Filter) for Short-Current Detection Input
9	$IN_{(UH)}$	Signal Input for High-side U Phase
10	$V_{CC(H)}$	High-side Common Bias Voltage for IC and IGBTs Driving
11	$V_{B(U)}$	High-side Bias Voltage for U Phase IGBT Driving
12	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High-side V Phase
14	$V_{CC(H)}$	High-side Common Bias Voltage for IC and IGBTs Driving
15	$V_{B(V)}$	High-side Bias Voltage for V Phase IGBT Driving
16	$V_{S(V)}$	High-side Bias Voltage Ground for V Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High-side W Phase
18	$V_{CC(H)}$	High-side Common Bias Voltage for IC and IGBTs Driving
19	$V_{B(W)}$	High-side Bias Voltage for W Phase IGBT Driving
20	$V_{S(W)}$	High-side Bias Voltage Ground for W Phase IGBT Driving
21	N_U	Negative DC–Link Input for U Phase
22	N_V	Negative DC–Link Input for V Phase
23	N_W	Negative DC–Link Input for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC–Link Input

Internal Equivalent Circuit and Input/Output Pins


(19) $V_{B(W)}$
(18) $V_{CC(H)}$
(17) $IN_{(WH)}$
(20) $V_{S(W)}$
(15) $V_{B(V)}$
(14) $V_{CC(H)}$
(13) $IN_{(VH)}$
(16) $V_{S(V)}$
(11) $V_{B(U)}$
(10) $V_{CC(H)}$
(9) $IN_{(UH)}$
(12) $V_{S(U)}$
(8) C_{SC}
(7) C_{FOD}
(6) V_{FO}
(5) $IN_{(WL)}$
(4) $IN_{(VL)}$
(3) $IN_{(UL)}$
(2) COM
(1) $V_{CC(L)}$
VB
VCC
COM
IN
OUT
VS
C(SC)
C(FOD)
VFO
IN(WL)
IN(VL)
IN(UL)
COM
VCC
OUT(WL)
OUT(VL)
OUT(UL)
V_{SL}
P (27)
W (26)
V (25)
U (24)
N_W (23)
N_V (22)
N_U (21)

Note:

1. Inverter low-side is composed of three IGBTs, freewheeling diodes for each IGBT and one control IC. It has gate drive and protection functions.
2. Inverter power side is composed of four inverter dc-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three IGBTs, freewheeling diodes and three drive ICs for each IGBT.

Figure 3.

Absolute Maximum Ratings (T_J = 25°C, Unless Otherwise Specified)

Inverter Part

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	Supply Voltage	Applied between P- N_U, N_V, N_W	450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P- N_U, N_V, N_W	500	V
V_{CES}	Collector-emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	T_C = 25°C	20	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C = 25°C, Under 1ms Pulse Width	40	A
P_C	Collector Dissipation	T_C = 25°C per One Chip	62	W
T_J	Operating Junction Temperature	(Note 1)	-40 ~ 150	°C

Note:

1. The maximum junction temperature rating of the power chips integrated within the SPM is 150°C(@$T_C \leq$ 125°C).

Control Part

Symbol	Parameter	Conditions	Rating	Units
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ - COM	20	V
V_{BS}	High-side Control Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM	-0.3~17	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} - COM	-0.3~V_{CC}+0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} Pin	5	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} - COM	-0.3~V_{CC}+0.3	V

Bootstrap Diode Part

Symbol	Parameter	Conditions	Rating	Units
V_{RRM}	Maximum Repetitive Reverse Voltage		600	V
I_F	Forward Current	T_C = 25°C	0.5	A
I_{FP}	Forward Current (Peak)	T_C = 25°C, Under 1ms Pulse Width	2	A
T_J	Operating Junction Temperature		-40 ~ 150	°C

Total System

Symbol	Parameter	Conditions	Rating	Units
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	V_{CC} = V_{BS} = 13.5 ~ 16.5V T_J = 150°C, Non-repetitive, less than 2μs	400	V
T_C	Module Case Operation Temperature	-40°C$\leq T_J \leq$ 150°C, See Figure 2	-40 ~ 125	°C
T_{STG}	Storage Temperature		-40 ~ 150	°C
V_{ISO}	Isolation Voltage	60Hz, Sinusoidal, AC 1 minute, Connection Pins to heat sink plate	2500	V_{rms}

Thermal Resistance

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance	Inverter IGBT part (per 1/6 module)	-	-	2.0	°C/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	-	-	3.0	°C/W

Note:

2. For the measurement point of case temperature(T_C), please refer to Figure 2.

Electrical Characteristics (T_J = 25°C, Unless Otherwise Specified)

Inverter Part

Symbol		Parameter	Conditions		Min.	Typ.	Max.	Units
$V_{CE(SAT)}$		Collector-Emitter Saturation Voltage	$V_{CC} = V_{BS}$ = 15V V_{IN} = 5V	I_C = 20A, T_J = 25°C	-	-	2.0	V
V_F		FWD Forward Voltage	V_{IN} = 0V	I_F = 20A, T_J = 25°C	-	-	2.2	V
HS	t_{ON}	Switching Times	V_{PN} = 300V, $V_{CC} = V_{BS}$ = 15V I_C = 20A V_{IN} = 0V ↔ 5V, Inductive Load (Note 3)		-	0.75	-	μs
	$t_{C(ON)}$				-	0.2	-	μs
	t_{OFF}				-	0.45	-	μs
	$t_{C(OFF)}$				-	0.15	-	μs
	t_{rr}				-	0.1	-	μs
LS	t_{ON}		V_{PN} = 300V, $V_{CC} = V_{BS}$ = 15V I_C = 20A V_{IN} = 0V ↔ 5V, Inductive Load (Note 3)		-	0.5	-	μs
	$t_{C(ON)}$				-	0.3	-	μs
	t_{OFF}				-	0.45	-	μs
	$t_{C(OFF)}$				-	0.15	-	μs
	t_{rr}				-	0.1	-	μs
I_{CES}		Collector-Emitter Leakage Current	$V_{CE} = V_{CES}$		-	-	1	mA

Note:

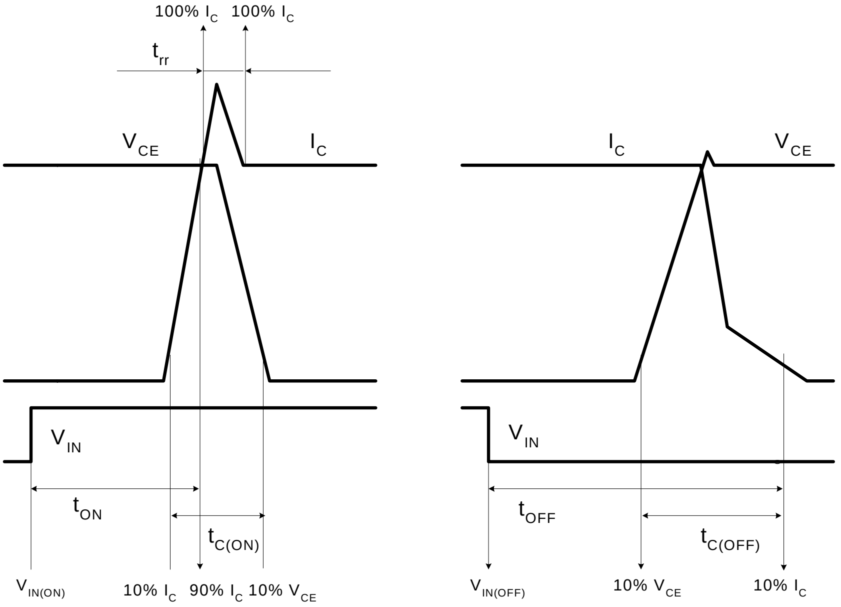
3. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

Control Part

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
I_{QCCL}	Quiescent V_{CC} Supply Current	V_{CC} = 15V $IN_{(UL, VL, WL)}$ = 0V	$V_{CC(L)}$ - COM	-	-	23	mA
I_{QCCH}		V_{CC} = 15V $IN_{(UH, VH, WH)}$ = 0V	$V_{CC(H)}$ - COM	-	-	600	μA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15V $IN_{(UH, VH, WH)}$ = 0V	$V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	-	-	500	μA
V_{FOH}	Fault Output Voltage	V_{SC} = 0V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up		4.5	-	-	V
V_{FOL}		V_{SC} = 1V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up		-	-	0.8	V
$V_{SC(ref)}$	Short Circuit Trip Level	V_{CC} = 15V (Note 4)		0.45	0.5	0.55	V
TSD	Over-temperature protection	Temperature at LVIC		-	160	-	°C
ΔTSD	Over-temperature protection hysterisis	Temperature at LVIC		-	5	-	°C
UV_{CCD}	Supply Circuit Under-Voltage Protection	Detection Level		10.7	11.9	13.0	V
UV_{CCR}		Reset Level		11.2	12.4	13.4	V
UV_{BSD}		Detection Level		10	11	12	V
UV_{BSR}		Reset Level		10.5	11.5	12.5	V
t_{FOD}	Fault-out Pulse Width	C_{FOD} = 33nF (Note 5)		1.0	1.8	-	ms
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM		2.8	-	-	V
$V_{IN(OFF)}$	OFF Threshold Voltage			-	-	0.8	V

Note:

4. Short-circuit current protection is functioning only at the low-sides.
5. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}$[F]


100% I_C
100% I_C
t_{rr}
V_{CE}
I_C
V_{IN}
t_{ON}
$t_{C(ON)}$
$V_{IN(ON)}$
10% I_C
90% I_C
10% V_{CE}
I_C
V_{CE}
V_{IN}
t_{OFF}
$t_{C(OFF)}$
$V_{IN(OFF)}$
10% V_{CE}
10% I_C

(a) turn-on

(b) turn-off

Figure 4. Switching Time Definition

Switching Loss (Typical)

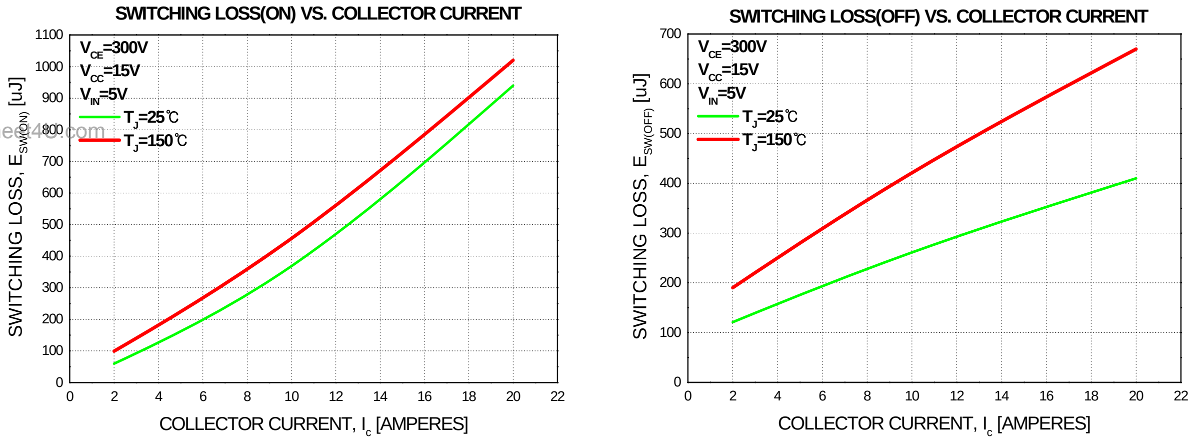
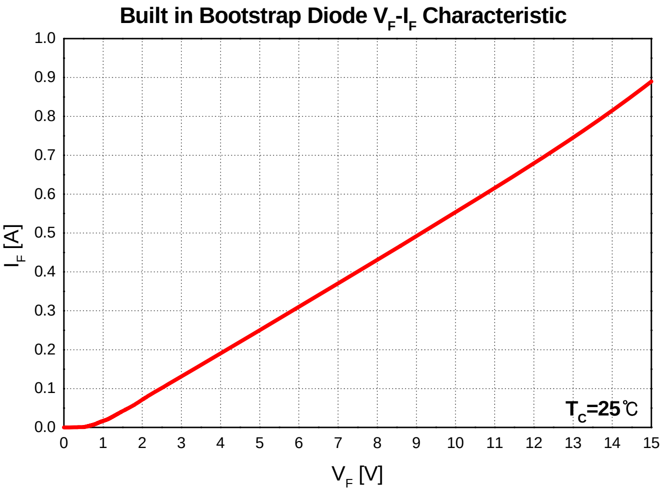


Figure 5. Switching Loss Characteristics

Bootstrap Diode Part

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_F	Forward Voltage	I_F = 0.1A, T_C = 25°C	-	2.5	-	V
t_{rr}	Reverse Recovery Time	I_F = 0.1A, T_C = 25°C	-	80	-	ns



Note:

6. Built in bootstrap diode includes around 15Ω resistance characteristic.

Figure 6. Built in Bootstrap Diode Characteristics

Recommended Operating Conditions

Symbol	Parameter	Conditions	Value			Units
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W	-	300	400	V
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$- COM	13.5	15	16.5	V
V_{BS}	High-side Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	13.0	15	18.5	V
dV_{CC}/dt, dV_{BS}/dt	Control supply variation		-1	-	1	V/µs
t_{dead}	Blanking Time for Preventing Arm-short	For Each Input Signal	2.0	-	-	µs
f_{PWM}	PWM Input Signal	-40°C ≤ T_C ≤ 125°C, -40°C ≤ T_J ≤ 150°C	-	-	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W - COM (Including surge voltage)	-4		4	V

Mechanical Characteristics and Ratings

Parameter	Conditions		Limits			Units
			Min.	Typ.	Max.	
Mounting Torque	Mounting Screw: - M3	Recommended 0.62N•m	0.51	0.62	0.80	N•m
Device Flatness		Note Figure 5	0	-	+120	µm
Weight			-	15.00	-	g

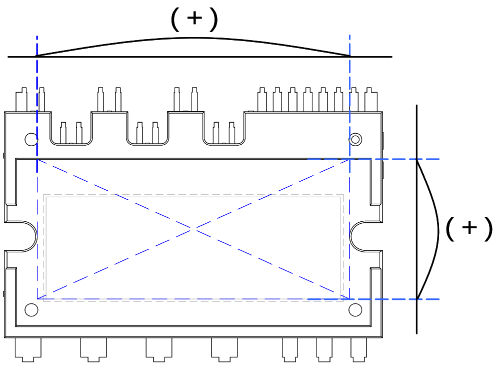
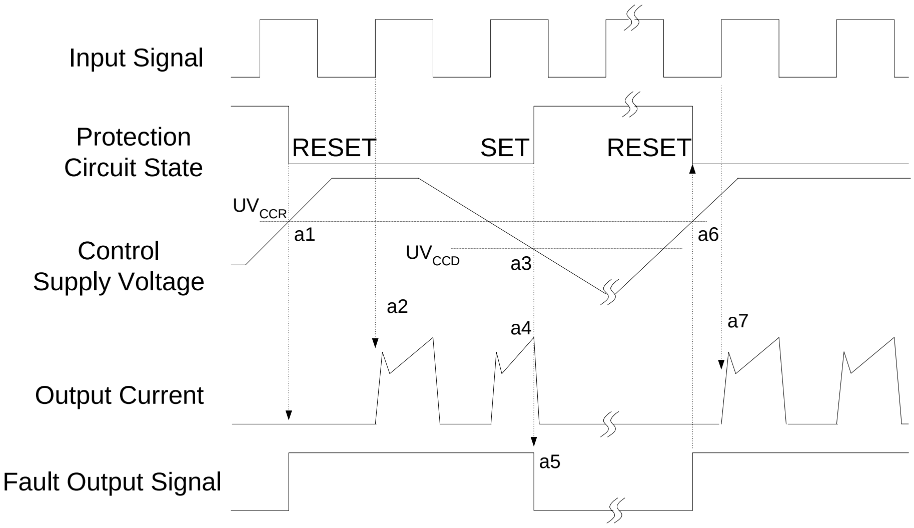


Figure 7. Flatness Measurement Position

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FSBB20CH60C	FSBB20CH60C	SPM27-CC	-	-	10

Time Charts of SPMs Protective Function


Input Signal
Protection Circuit State
RESET
SET
RESET
UV_{CCR}
a1
UV_{CCD}
a3
a6
Control Supply Voltage
a2
a4
a7
Output Current
Fault Output Signal
a5

a1 : Control supply voltage rises: After the voltage rises UV_{CCR}, the circuits start to operate when next input is applied.

a2 : Normal operation: IGBT ON and carrying current.

a3 : Under voltage detection (UV_{CCD}).

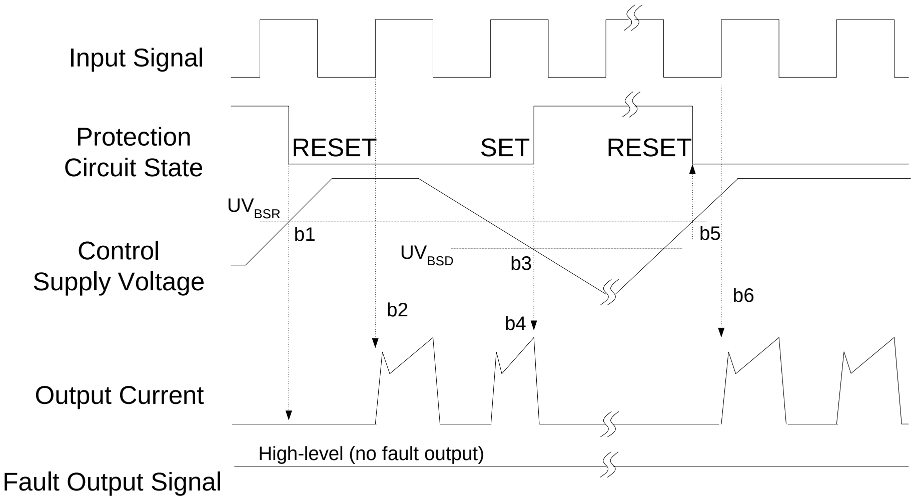
a4 : IGBT OFF in spite of control input condition.

a5 : Fault output operation starts.

a6 : Under voltage reset (UV_{CCR}).

a7 : Normal operation: IGBT ON and carrying current.

Figure 8. Under-Voltage Protection (Low-side)


Input Signal
Protection Circuit State
RESET
SET
RESET
UV_{BSR}
b1
UV_{BSD}
b3
b5
Control Supply Voltage
b2
b4
b6
Output Current
High-level (no fault output)
Fault Output Signal

b1 : Control supply voltage rises: After the voltage reaches UV_{BSR}, the circuits start to operate when next input is applied.

b2 : Normal operation: IGBT ON and carrying current.

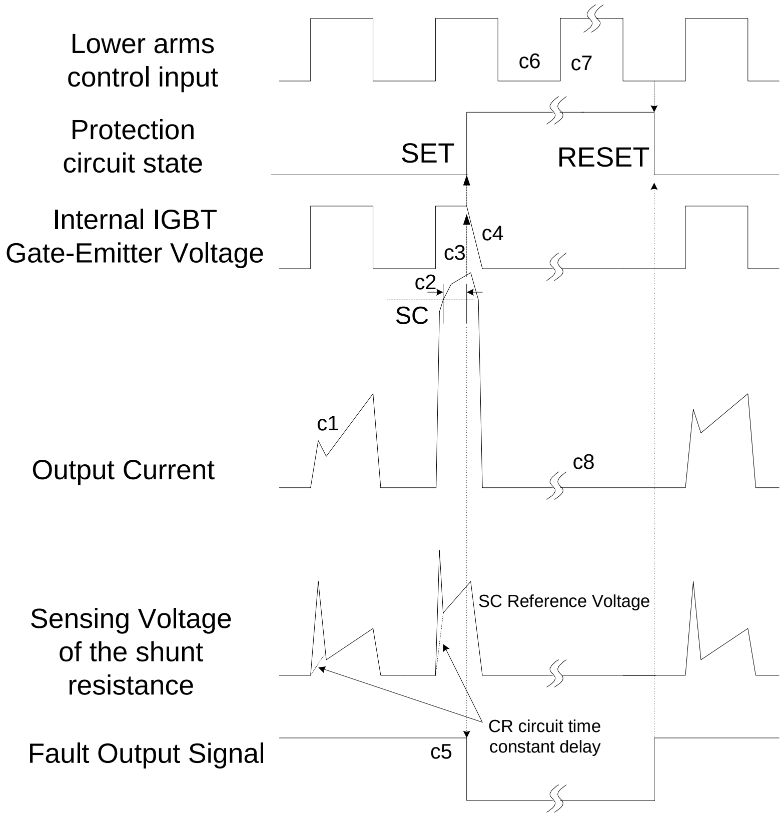
b3 : Under voltage detection (UV_{BSD}).

b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.

b5 : Under voltage reset (UV_{BSR})

b6 : Normal operation: IGBT ON and carrying current

Figure 9. Under-Voltage Protection (High-side)


Lower arms control input
Protection circuit state
Internal IGBT Gate-Emitter Voltage
Output Current
Sensing Voltage of the shunt resistance
Fault Output Signal
c6
c7
SET
RESET
c4
c3
c2
SC
c1
c8
SC Reference Voltage
CR circuit time constant delay
c5

(with the external shunt resistance and CR connection)

c1 : Normal operation: IGBT ON and carrying current.

c2 : Short circuit current detection (SC trigger).

c3 : Hard IGBT gate interrupt.

c4 : IGBT turns OFF.

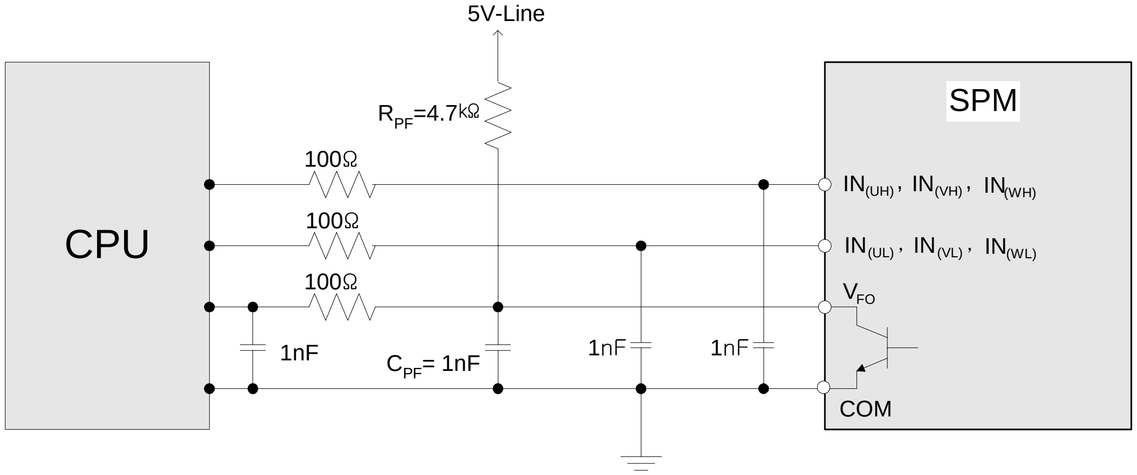
c5 : Fault output timer operation starts: The pulse width of the fault output signal is set by the external capacitor C_{FO}.

c6 : Input “L” : IGBT OFF state.

c7 : Input “H”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.

c8 : IGBT OFF state

Figure 10. Short-Circuit Current Protection (Low-side Operation only)

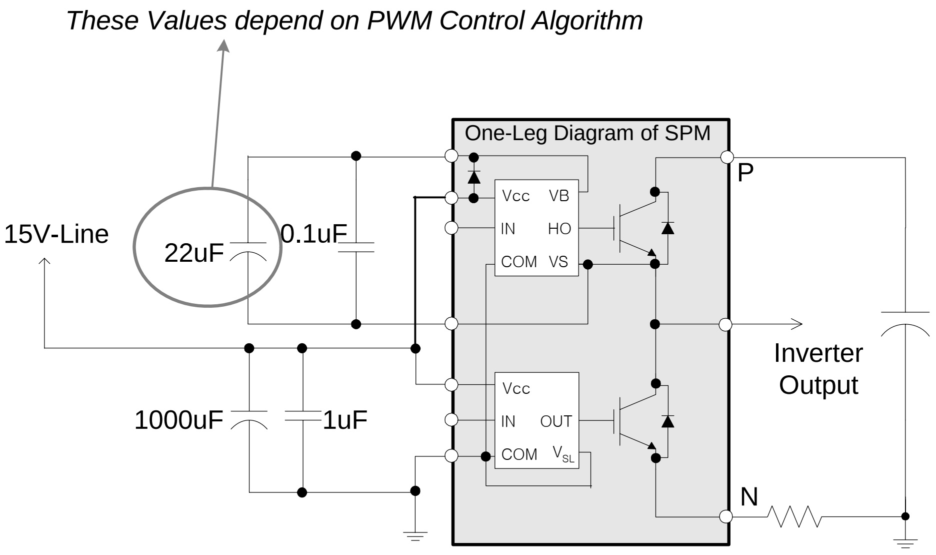

5V-Line
R_PF=4.7kΩ
100Ω
100Ω
100Ω
CPU
SPM
IN(UH), IN(VH), IN(WH)
IN(UL), IN(VL), IN(WL)
VFO
COM
1nF
CPF= 1nF
1nF
1nF

Note:

1) RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The SPM input signal section integrates 5kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

2) The logic input is compatible with standard CMOS or LSTTL outputs.

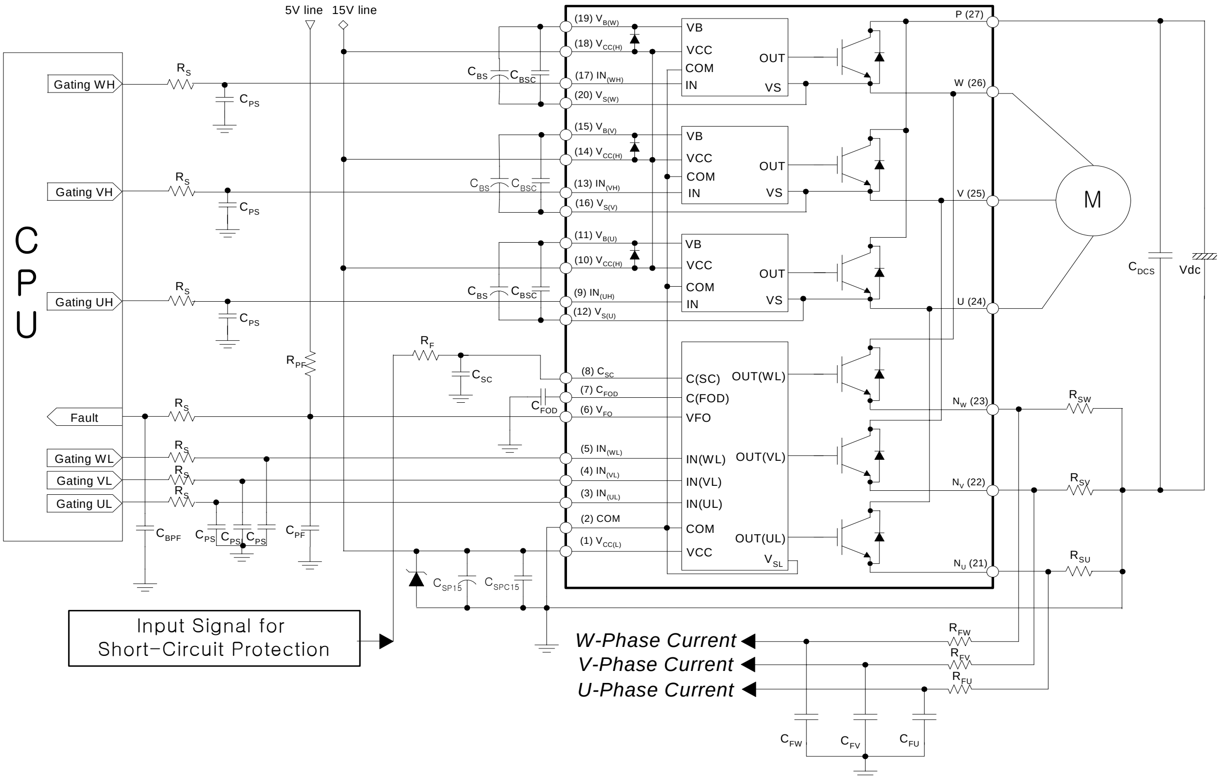
Figure 11. Recommended CPU I/O Interface Circuit


These Values depend on PWM Control Algorithm
One-Leg Diagram of SPM
15V-Line
22uF
0.1uF
1000uF
1uF
Vcc
VB
IN
HO
COM
VS
Vcc
IN
OUT
COM
VSL
P
N
Inverter
Output

Note:

1) The ceramic capacitor placed between V_{CC}-COM should be over 1uF and mounted as close to the pins of the SPM as possible.

Figure 12. Recommended Bootstrap Operation Circuit and Parameters


5V line
15V line
C
P
U
Gating WH
Gating VH
Gating UH
Fault
Gating WL
Gating VL
Gating UL
R_S
C_{PS}
R_{PF}
C_{BPF}
C_{PF}
R_F
C_{SC}
C_{FOD}
C_{BS}
C_{BSC}
C_{SP15}
C_{SPC15}
(19) $V_{B(W)}$
(18) $V_{CC(H)}$
(17) $IN_{(WH)}$
(20) $V_{S(W)}$
(15) $V_{B(V)}$
(14) $V_{CC(H)}$
(13) $IN_{(VH)}$
(16) $V_{S(V)}$
(11) $V_{B(U)}$
(10) $V_{CC(H)}$
(9) $IN_{(UH)}$
(12) $V_{S(U)}$
(8) C_{SC}
(7) C_{FOD}
(6) V_{FO}
(5) $IN_{(WL)}$
(4) $IN_{(VL)}$
(3) $IN_{(UL)}$
(2) COM
(1) $V_{CC(L)}$
VB
VCC
COM
IN
OUT
VS
C(SC)
C(FOD)
VFO
IN(WL)
IN(VL)
IN(UL)
OUT(WL)
OUT(VL)
OUT(UL)
V_{SL}
P (27)
W (26)
V (25)
U (24)
N_W (23)
N_V (22)
N_U (21)
M
C_{DCS}
Vdc
R_{SW}
R_{SV}
R_{SU}
R_{FW}
R_{FV}
R_{FU}
C_{FW}
C_{FV}
C_{FU}
Input Signal for Short-Circuit Protection
W-Phase Current
V-Phase Current
U-Phase Current

Note:

1) To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)

2) By virtue of integrating an application specific type HVIC inside the SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

3) V_{FO} output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7kΩ resistance. Please refer to Figure11.

4) C_{SP15} of around 7 times larger than bootstrap capacitor C_{BS} is recommended.

5) V_{FO} output pulse width should be determined by connecting an external capacitor(C_{FOD}) between C_{FOD}(pin7) and COM(pin2). (Example : if C_{FOD} = 33 nF, then t_{FO} = 1.8ms (typ.)) Please refer to the note 5 for calculation method.

6) Input signal is High-Active type. There is a 5kΩ resistor inside the IC to pull down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. R_SC_{PS} time constant should be selected in the range 50~150ns. C_{PS} should not be less than 1nF.(Recommended R_S=100Ω , C_{PS}=1nF)

7) To prevent errors of the protection function, the wiring around R_F and C_{SC} should be as short as possible.

8) In the short-circuit protection circuit, please select the R_FC_{SC} time constant in the range 1.5~2μs.

9) Each capacitor should be mounted as close to the pins of the SPM as possible.

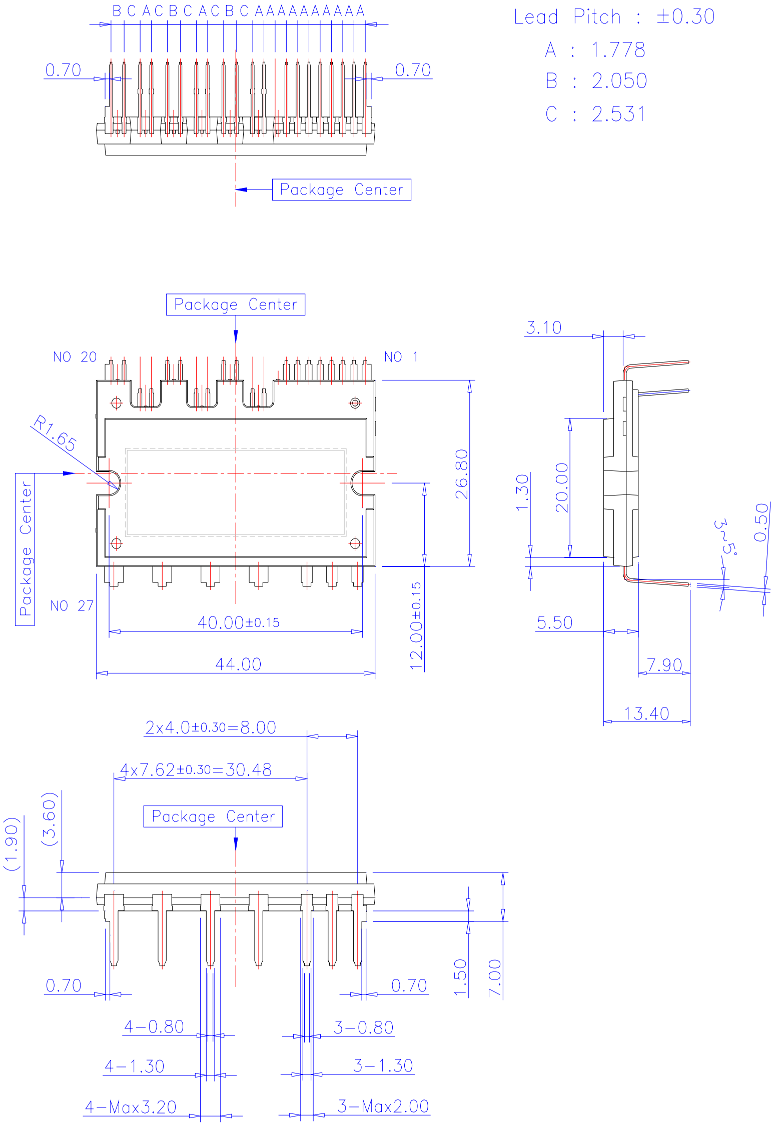
10) To prevent surge destruction, the wiring between the smoothing capacitor and the P&GND pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22μF between the P&GND pins is recommended.

11) Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays.

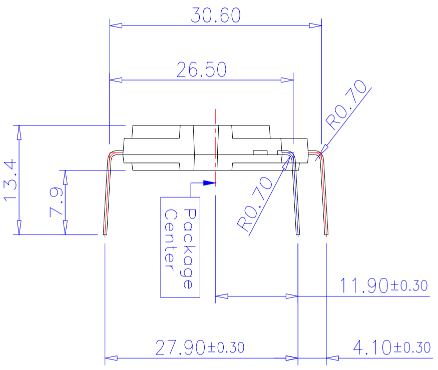
12) C_{SPC15} should be over 1μF and mounted as close to the pins of the SPM as possible.

Figure 13. Typical Application Circuit

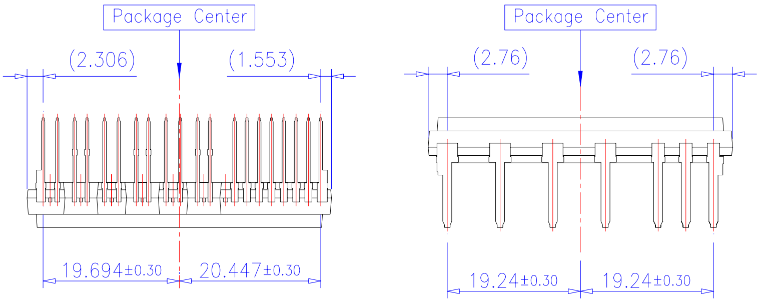
Detailed Package Outline Drawings


B C A C B C A C B C A A A A A A A A A A
0.70
0.70
Lead Pitch : ±0.30
A : 1.778
B : 2.050
C : 2.531
Package Center
Package Center
NO 20
NO 1
R1.65
Package Center
NO 27
26.80
40.00±0.15
44.00
12.00±0.15
3.10
1.30
20.00
3~5°
0.50
5.50
7.90
13.40
2x4.0±0.30=8.00
4x7.62±0.30=30.48
Package Center
(1.90)
(3.60)
0.70
0.70
1.50
7.00
4-0.80
3-0.80
4-1.30
3-1.30
4-Max3.20
3-Max2.00

Detailed Package Outline Drawings (Continued)

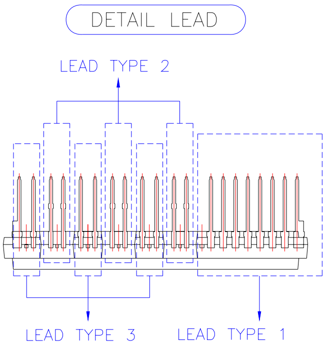

30.60
26.50
R0.70
R0.70
13.4
7.9
Package Center
11.90±0.30
27.90±0.30
4.10±0.30

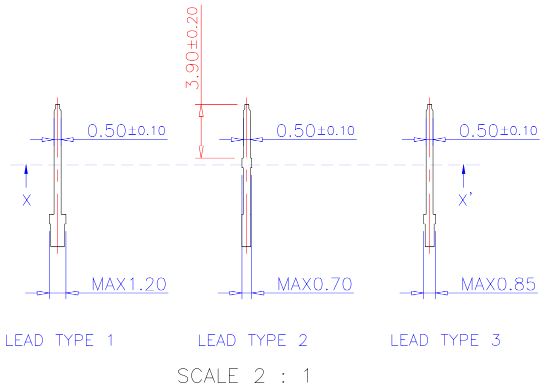
Lead Forming Dimension

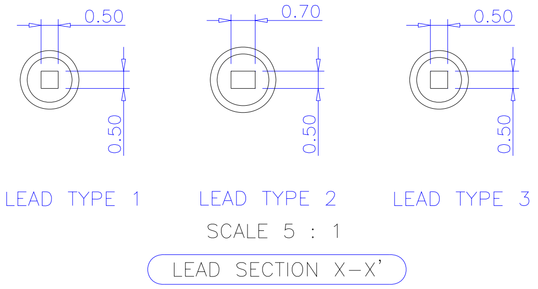

Package Center
(2.306)
(1.553)
19.694±0.30
20.447±0.30
Package Center
(2.76)
(2.76)
19.24±0.30
19.24±0.30

PKG Center to Lead Distance

Detailed Package Outline Drawings (Continued)


DETAIL LEAD
LEAD TYPE 2
LEAD TYPE 3
LEAD TYPE 1


3.90±0.20
0.50±0.10
0.50±0.10
0.50±0.10
X
X'
MAX1.20
MAX0.70
MAX0.85
LEAD TYPE 1
LEAD TYPE 2
LEAD TYPE 3
SCALE 2 : 1


0.50
0.70
0.50
0.50
0.50
0.50
LEAD TYPE 1
LEAD TYPE 2
LEAD TYPE 3
SCALE 5 : 1
LEAD SECTION X-X'

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TinyBoost™
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TinyLogic®
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