

MMBF4391LT1, MMBF4392LT1, MMBF4393LT1

JFET Switching Transistors N-Channel

Features

- Pb-Free Packages are Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	50	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 1) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

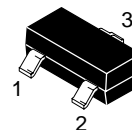
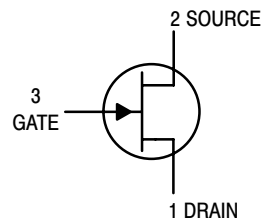
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR-5 = $1.0 \times 0.75 \times 0.062$ in.



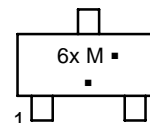
ON Semiconductor®

<http://onsemi.com>



SOT-23
CASE 318
STYLE 10

MARKING DIAGRAM



- 6x = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2 of this data sheet.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

MMBF4391LT1, MMBF4392LT1, MMBF4393LT1

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate–Source Breakdown Voltage (I _G = 1.0 μAdc, V _{DS} = 0)	V _{(BR)GSS}	30	–	Vdc
Gate Reverse Current (V _{GS} = 15 Vdc, V _{DS} = 0, T _A = 25°C) (V _{GS} = 15 Vdc, V _{DS} = 0, T _A = 100°C)	I _{GSS}	– –	1.0 0.20	nAdc μAdc
Gate–Source Cutoff Voltage (V _{DS} = 15 Vdc, I _D = 10 nAdc)	V _{GS(off)}	–4.0 –2.0 –0.5	–10 –5.0 –3.0	Vdc
Off–State Drain Current (V _{DS} = 15 Vdc, V _{GS} = –12 Vdc) (V _{DS} = 15 Vdc, V _{GS} = –12 Vdc, T _A = 100°C)	I _{D(off)}	– –	1.0 1.0	nAdc μAdc
ON CHARACTERISTICS				
Zero–Gate–Voltage Drain Current (V _{DS} = 15 Vdc, V _{GS} = 0)	I _{DSS}	50 25 5.0	150 75 30	mAdc
Drain–Source On–Voltage (I _D = 12 mAdc, V _{GS} = 0) (I _D = 6.0 mAdc, V _{GS} = 0) (I _D = 3.0 mAdc, V _{GS} = 0)	V _{DS(on)}	– – –	0.4 0.4 0.4	Vdc
Static Drain–Source On–Resistance (I _D = 1.0 mAdc, V _{GS} = 0)	r _{DS(on)}	– – –	30 60 100	Ω
SMALL–SIGNAL CHARACTERISTICS				
Input Capacitance (V _{DS} = 15 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{iss}	–	14	pF
Reverse Transfer Capacitance (V _{DS} = 0, V _{GS} = 12 Vdc, f = 1.0 MHz)	C _{rss}	–	3.5	pF

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MMBF4391LT1	6J	SOT–23	3000 / Tape & Reel
MMBF4391LT1G	6J	SOT–23 (Pb–Free)	
MMBF4392LT1	6K	SOT–23	
MMBF4392LT1G	6K	SOT–23 (Pb–Free)	
MMBF4393LT1	6G	SOT–23	
MMBF4393LT1G	6G	SOT–23 (Pb–Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MMBF4391LT1, MMBF4392LT1, MMBF4393LT1

TYPICAL CHARACTERISTICS

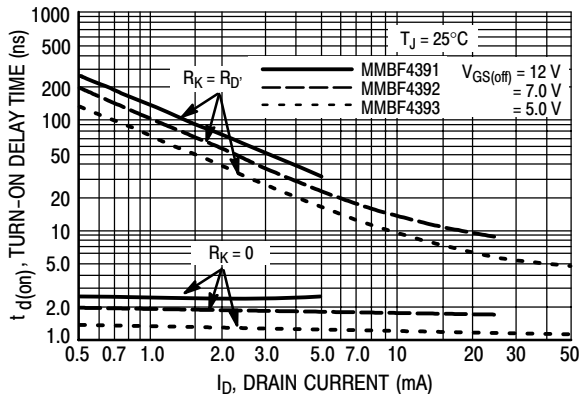


Figure 1. Turn-On Delay Time

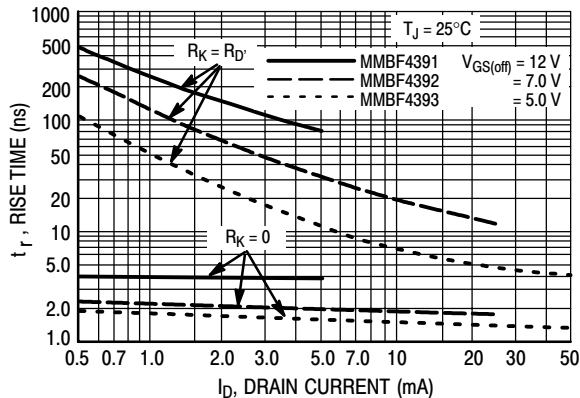


Figure 2. Rise Time

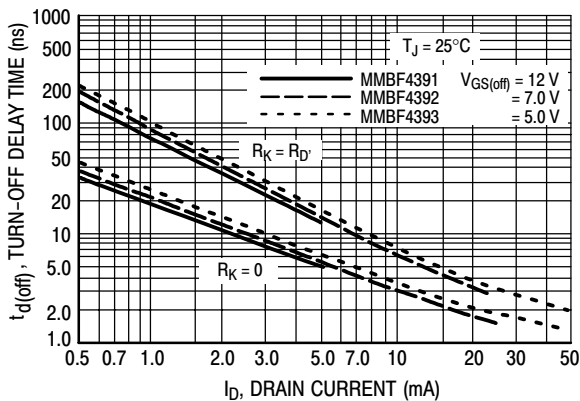


Figure 3. Turn-Off Delay Time

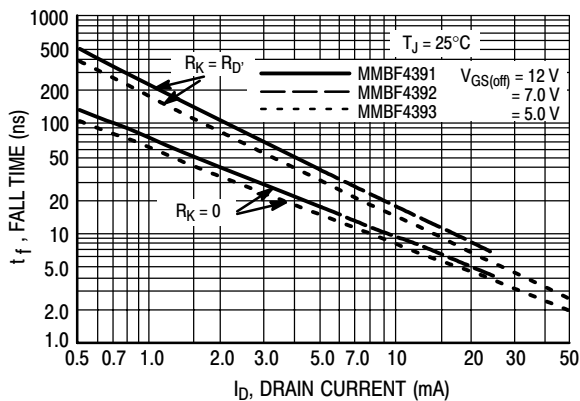


Figure 4. Fall Time

NOTE 1

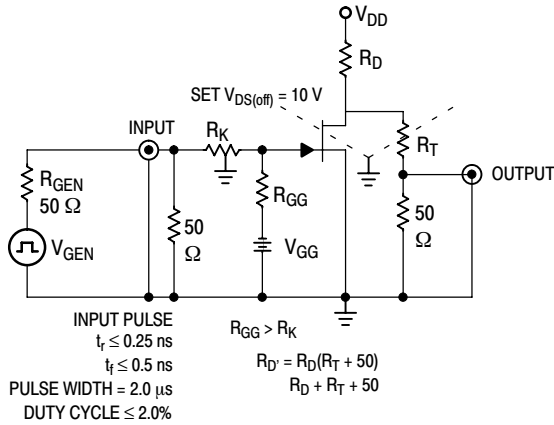


Figure 5. Switching Time Test Circuit

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($-V_{GG}$). The Drain-Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) of Gate-Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn-on interval, Gate-Source Capacitance (C_{gs}) discharges through the series combination of R_{GEN} and R_K . C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain-Source Resistance (r_{DS}). During the turn-off, this charge flow is reversed.

Predicting turn-on time is somewhat difficult as the channel resistance r_{DS} is a function of the gate-source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{DS} decreases. Since C_{gd} discharges through r_{DS} , turn-on time is non-linear. During turn-off, the situation is reversed with r_{DS} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to R_D' which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

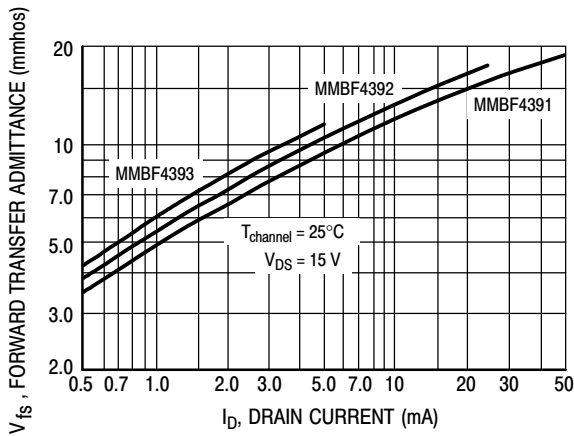


Figure 6. Typical Forward Transfer Admittance

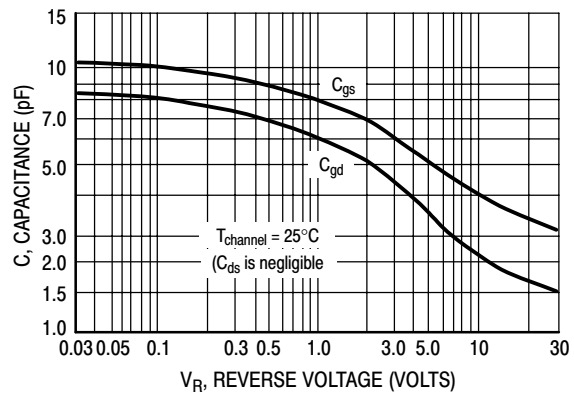


Figure 7. Typical Capacitance

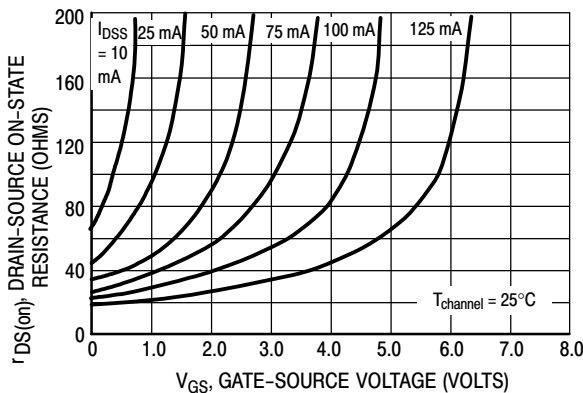


Figure 8. Effect of Gate-Source Voltage on Drain-Source Resistance

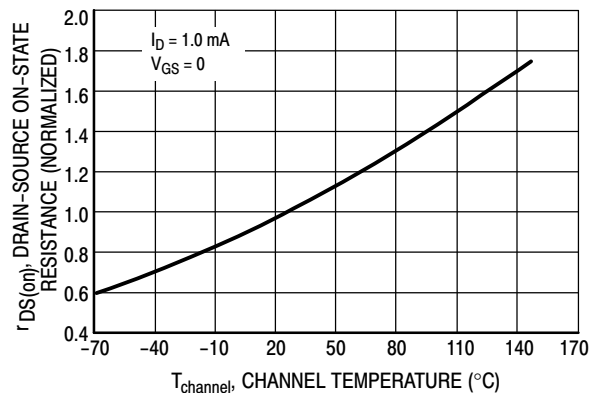


Figure 9. Effect of Temperature on Drain-Source On-State Resistance

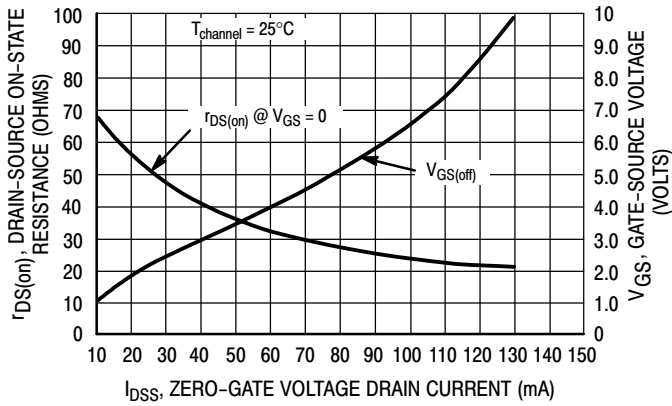


Figure 10. Effect of I_{DSS} on Drain-Source Resistance and Gate-Source Voltage

NOTE 2

The Zero-Gate-Voltage Drain Current (I_{DSS}) is the principle determinant of other J-FET characteristics. Figure 10 shows the relationship of Gate-Source Off Voltage ($V_{GS(off)}$) and Drain-Source On Resistance ($r_{DS(on)}$) to I_{DSS} . Most of the devices will be within $\pm 10\%$ of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

For example:

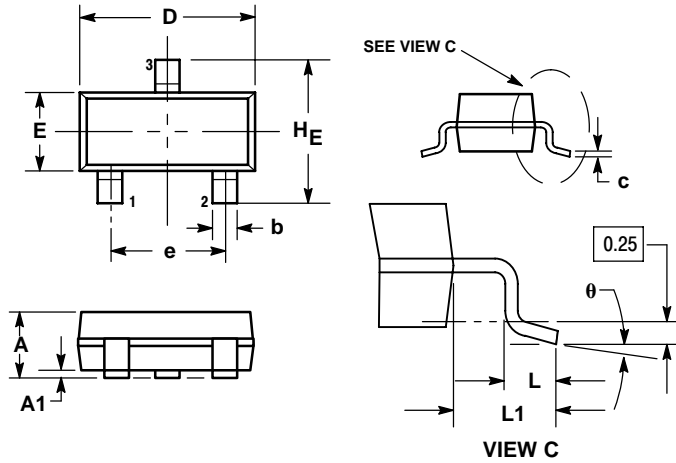
Unknown

$r_{DS(on)}$ and V_{GS} range for an MMBF4392

The electrical characteristics table indicates that an MMBF4392 has an I_{DSS} range of 25 to 75 mA. Figure 10 shows $r_{DS(on)} = 52 \Omega$ for $I_{DSS} = 25$ mA and 30Ω for $I_{DSS} = 75$ mA. The corresponding V_{GS} values are 2.2 V and 4.8 V.

MMBF4391LT1, MMBF4392LT1, MMBF4393LT1

PACKAGE DIMENSIONS SOT-23 (TO-236) CASE 318-08 ISSUE AN



NOTES:

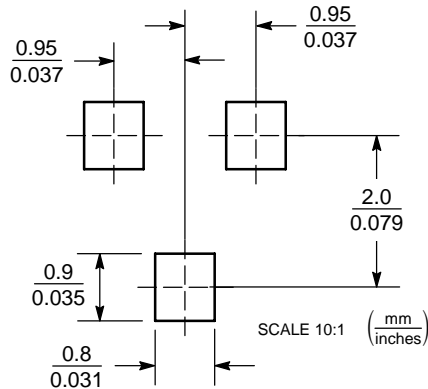
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104


STYLE 10:

1. DRAIN
2. SOURCE
3. GATE

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.