UM74HCT646

Octal Bus Transceivers and Registers

Features

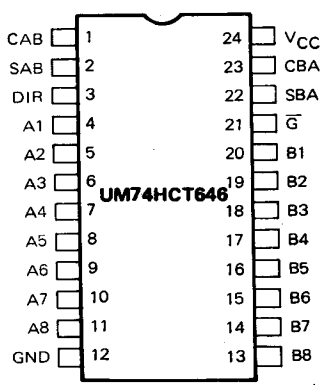
- 8 bi-directional data bus
- Transmits directly real-time data or stored data in either direction
- 3-state outputs with driving capability for direct bus interface
- Low power consumption with function, pin-out, speed and drive compatibility with 74LS logic family and interfaces directly with TTL, NMOS and CMOS devices

General Description

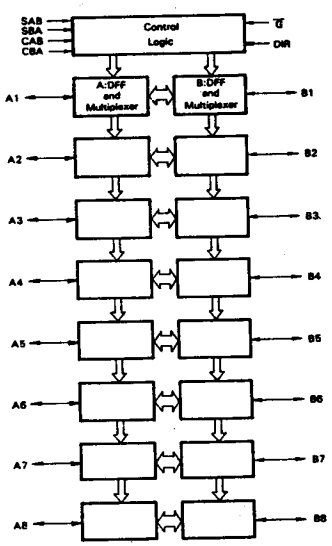
The UM74HCT646, fabricated using UMC silicon gate CMOS process, is a bi-directional bus transceiver with D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC} 7V

Operating Free-Air Temperature Range . . . . . 0°C to 70°C

Storage Temperature Range . . . . . −55°C to 125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics (V_{CC} = 5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	High-Level Input Voltage	2.0	–	–	V	
V_{IL}	Low-Level Input Voltage	–	0.5	0.8	V	
I_I	Input Current (all except I/O pins)	–	0.01	0.1	μA	V_I = 0V ~ 5V
V_{OH}	High-Level Output Voltage	4.8	–	–	V	$\lvert I_{OH} \rvert$ = 20 μA
		3.0	–	–	V	$\lvert I_{OH} \rvert$ = Max
V_{OL}	Low-Level Output Voltage	–	–	0.1	V	I_{OL} = 20 μA
		–	–	0.5	V	I_{OL} = 24 mA
I_{OZ}	3-state Leakage Current When Output is Disabled	–	–	0.5	μA	V_O = 0 ~ 5V
I_{CC}	Quiescent Supply Current	–	–	8	μA	V_{IN} = 0U or V_{CC} with No Load

AC Electrical Characteristics (Input t_r, $t_f \leq$ 2 ns)

Symbol	Parameter	Conditions†		T_A = 25°C, V_{CC} = 5.0V			Unit
				Min.	Typ.	Max.	
f_{max}	Maximum Clock Frequency	C_L = 50 pF		30	45	–	MHz
t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	C_L = 50 pF		–	12	25	ns
t_{PHL}		C_L = 50 pF		–	12	25	
t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	C_L = 50 pF		–	16	35	ns
t_{PHL}		C_L = 50 pF		–	16	35	
t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B High)	C_L = 50 pF		–	16	35	ns
t_{PHL}		C_L = 50 pF		–	16	35	
t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B High)	C_L = 50 pF		–	16	35	ns
t_{PHL}		C_L = 50 pF		–	16	35	
t_{PZL}	Maximum Output Enable Time, G or DIR Input to A or B Output	R_L = 1 kΩ	C_L = 50 pF	–	20	45	ns
t_{PZH}			C_L = 50 pF	–	20	45	
t_{PHZ}	Maximum Output Disable Time, G or DIR Input to A or B Output	R_L = 1 kΩ, C_L = 50 pF		–	20	45	ns
t_{PLZ}				–	20	45	
t_w	Pulse Duration, Clock High or Low			12	–	–	ns
t_{SU}	Setup Time, A before CAB ↑ or B before CAB ↑			15	–	–	ns

Pin Description

Symbol	Function
$A_1 \sim A_8$	Bi-directional data bus and register input
$B_1 \sim B_8$	Bi-directional data bus and register input
$\overline{G}$	Output enable. This pin is an active low pin, when high all outputs are disabled and A and B ports are isolated.
DIR	Direction control. This pin is used to determine the direction of data flow. When DIR = 1 ⇒ From A → B DIR = 0 ⇒ From B → A
SAB SBA	Determines whether data transmitted is from the data inputs or the register associated with those pins. When SAB (SBA) = 1 ⇒ Register → B (A) Bus. SAB (SBA) = 1 ⇒ A (B) → B (A)
CAB CBA	Positive trigger clock. When rising edge is triggered, data from A (B) input are loadeo into their associated register.

Transceiver function can work only when $\overline{G}$ is active low (G = 0). DIR determines the direction of data flow. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

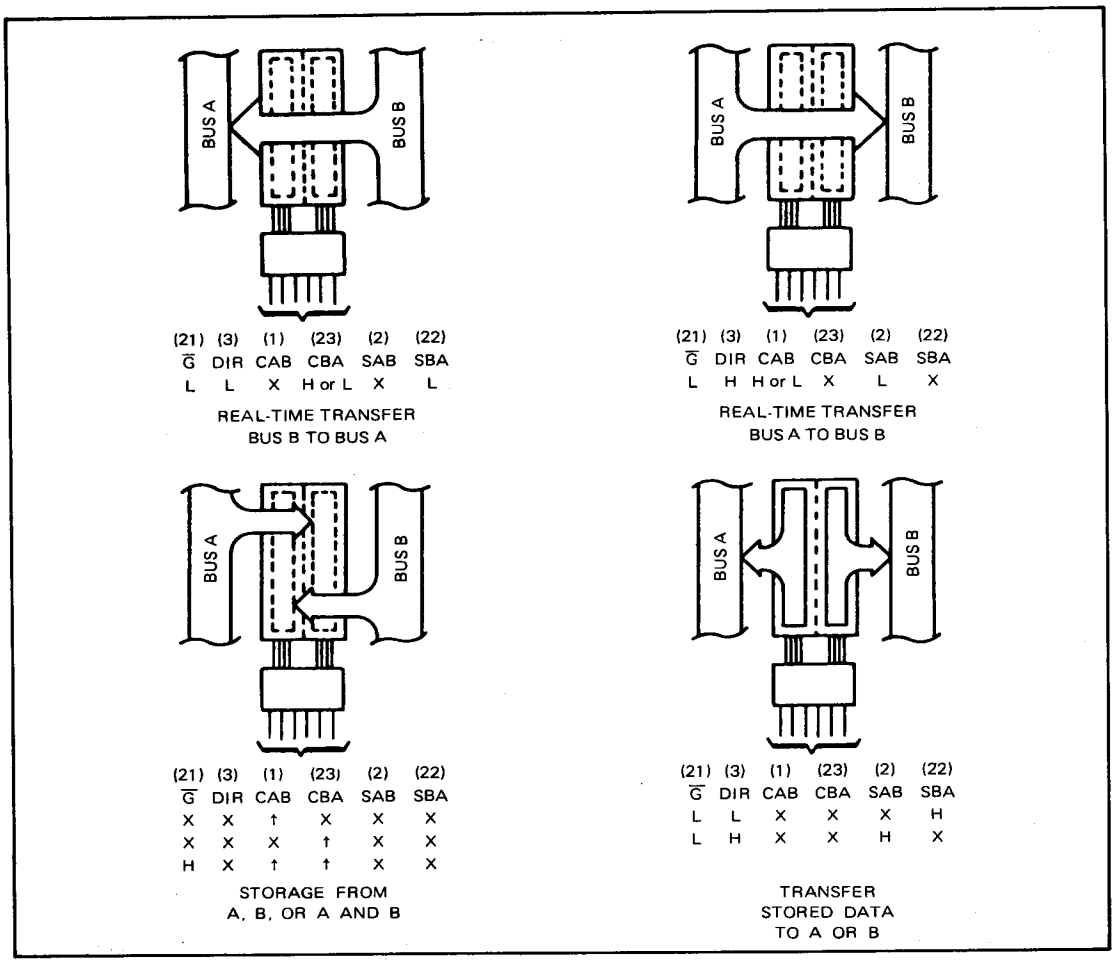
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Function Table

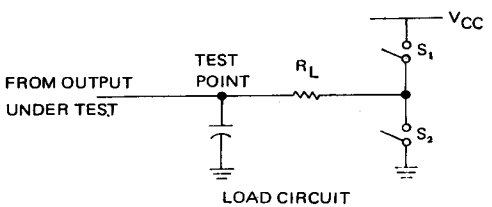
Inputs						Data I/O†		Operation or Function	
G	DIR	CAB	CBA	SAB	SBA	A1 Thru A8	B1 Thru B8	LS646, LS647	LS648, LS649
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	H or L	X	L	Output	Input	Real-time B Data to A Bus	Real-time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	H or L	X	L	X	Input	Output	Real-time A Data to B Bus	Real-time $\overline{A}$ Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

† The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Description

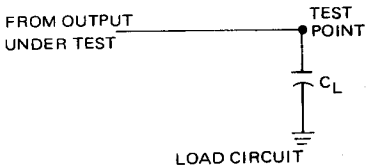


Parameter Measurement Information



Parameter		R_L	C_L	S_1	S_2
t_{en}	t_{PZH}	1 KΩ	50 pF	OPEN	CLOSED
	t_{PZL}			CLOSED	OPEN
t_{dis}	t_{PHZ}	1 KΩ	50 pF	OPEN	CLOSED
	t_{PLZ}			CLOSED	OPEN

Figure 1. 3-state Outputs



Parameter		C_L
t_{pd} or t_t	Standard outputs	50 pF
	High-current outputs	50 pF

Figure 2. Totem-Pole Outputs

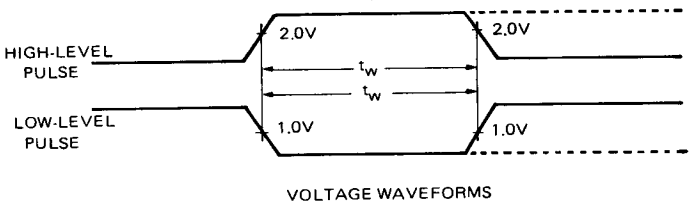


Figure 3. Pulse Durations

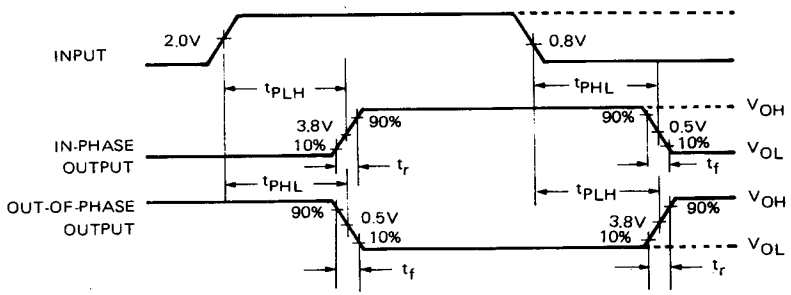


Figure 4. Propagation Delay Times and Output Transition Times

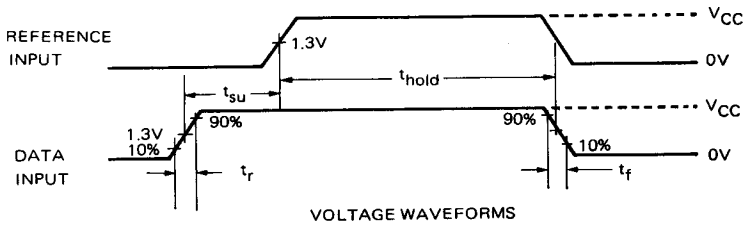


Figure 5. Setup and Hold Times and Input Rise and Fall Time

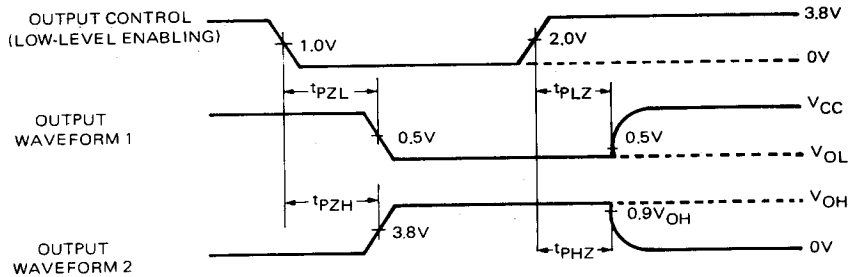


Figure 6. Enable and Disable Times for 3-state Outputs