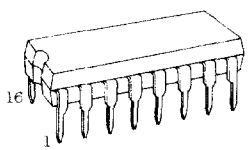
TC74HC4049 P/ F HEX BUFFER/CONVERTER (INVERTING)

TC74HC4050 P/ F HEX BUFFER CONVERTER

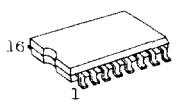
The TC74HC4049 and the TC74HC4050 are high speed CMOS HEX BUFFER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC4049 is an inverting buffer, while the TC74HC4050 is a non-inverting buffer.
The internal circuit is composed of 3-stage or 2-stage inverters, which enables high noise immunity and stable output.
Input protection circuits are different from those of the high speed CMOS IC's.
They eliminate diodes of V_{CC} side and enable logic-level conversion from high-level voltage (up to 15V) to low-level voltage.
These IC's are useful for battery back up circuits, because input voltage can be appled on IC's which is not biased by V_{CC}.

FEATURES:

- High Speed.....t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=6mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 4049B, 4050B.

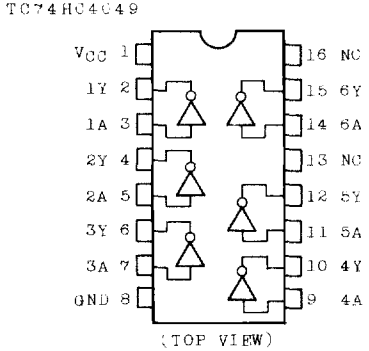


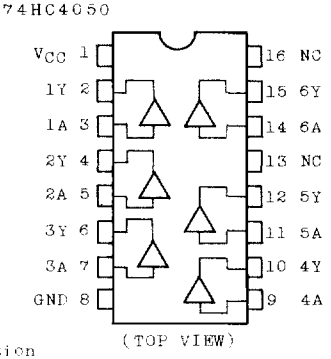
DIP16(3D16A-P)



MFP16(F16GC-P)

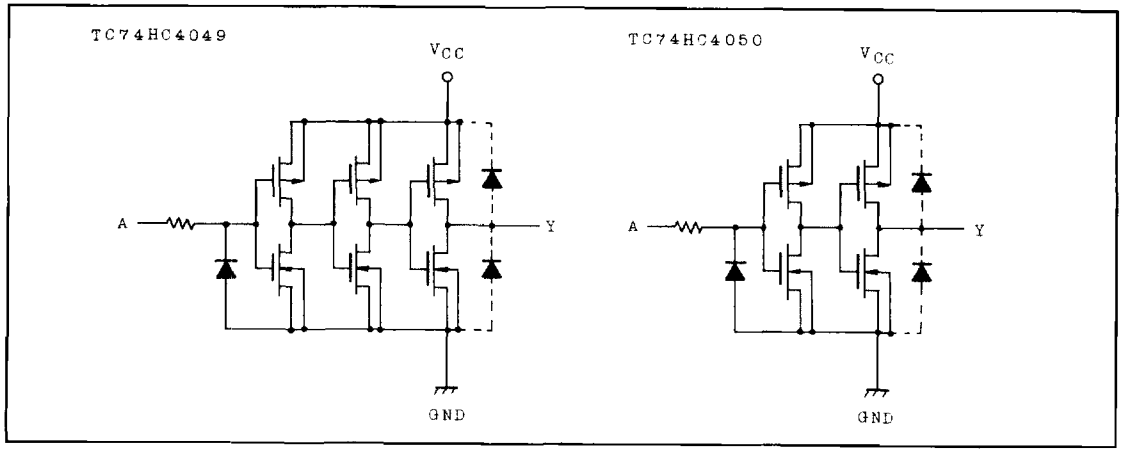
PIN ASSIGNMENT





NC : No Connection

CIRCUIT SCHEMATIC (per Gate)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ 18*	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)**/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

Note.
*DC input voltage is able to impress -0.5V to 18V based on GND without any relation to voltage of V_{CC}. Recommended operating condition is from 0V to 15V and it is possible to vonvert logic-level from 15V to 5V or 5V to 2V.

**500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ 15	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

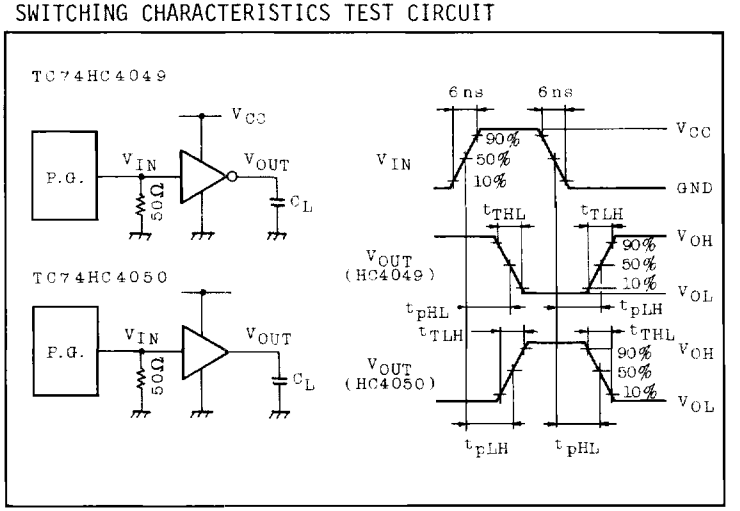
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

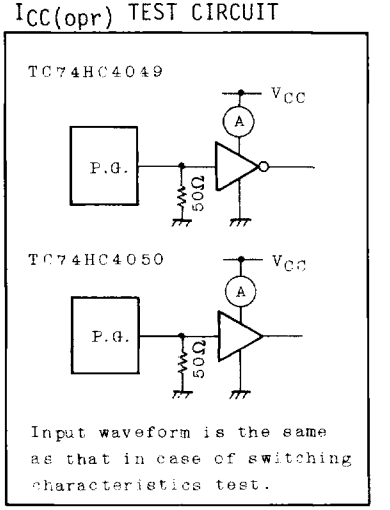
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	6	12	-	15	
			6.0	-	5	10	-	13	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	ns
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	25	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/6$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.