TC74HC195AP/AF 4-Bit Shift Register

The TC74HC195A is a high speed CMOS 4-BIT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The HC195A consists of parallel inputs, parallel outputs, two serial inputs (J, $\overline{K}$), and a SHIFT/$\overline{LOAD}$ input to control the device. When S/$\overline{L}$ is held low, the parallel data inputs are enabled, synchronous loading occurs and these data appear at the outputs on the next positive going edge of CLOCK.

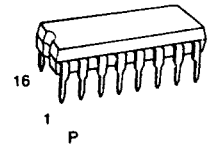
When S/$\overline{L}$ is held high, the serial data inputs are enabled, and the four flip-flops perform serial shifting on the positive going edge of each clock pulse.

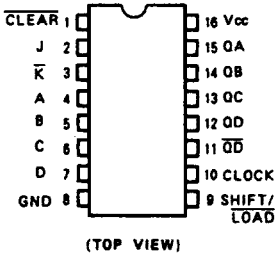
The $\overline{CLEAR}$ input overrides all other inputs, including the clock, and sets all flip-flops low.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

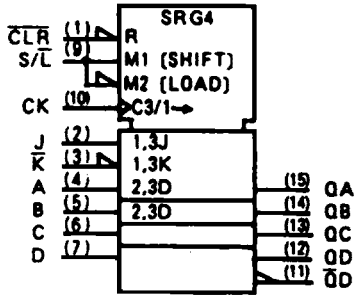
Features

- High Speed: f_{MAX} = 69MHz(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28%V_{CC}(Min.)
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS195





Pin Assignment



IEC Logic Symbol

Truth Table

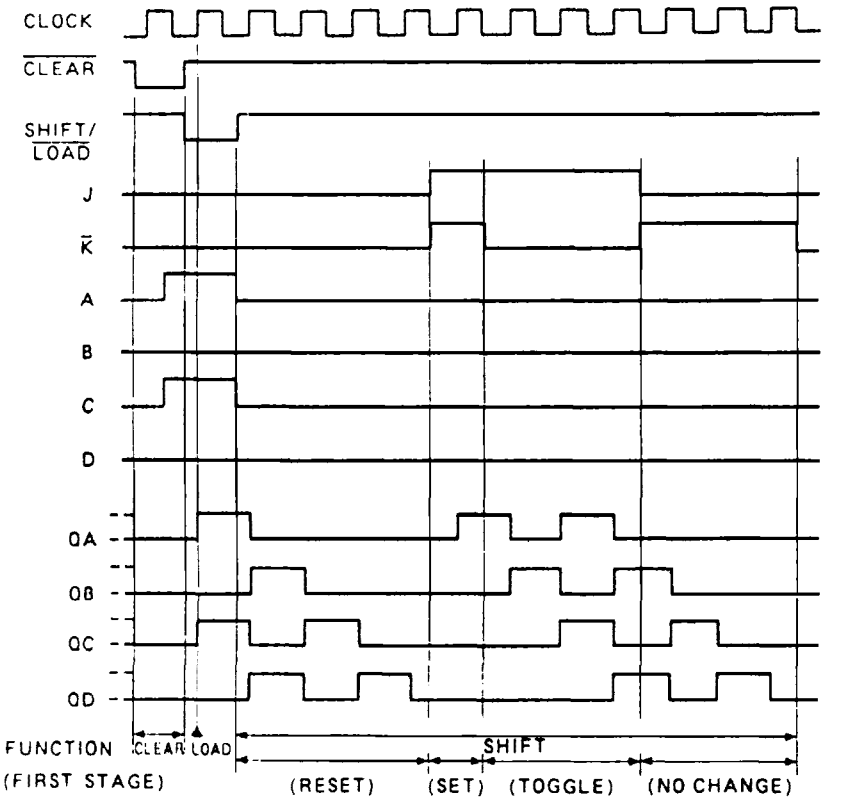
Inputs									Outputs				
$\overline{CLEAR}$	SHIFT/ LOAD	CLOCK	Serial		Parallel				QA	QB	QC	QD	$\overline{QD}$
			J	K	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	X	↓	X	X	X	X	X	X	QA0	QB0	QC0	QC0	$\overline{Q}$D0
H	H	↑	L	H	X	X	X	X	QAn	QAn	QBn	QCn	$\overline{Q}$Cn
H	H	↑	L	L	X	X	X	X	L	QAn	QBn	QCn	$\overline{Q}$Cn
H	H	↑	H	H	X	X	X	X	H	QAn	QBn	QCn	$\overline{Q}$Cn
H	H	↑	H	L	X	X	X	X	$\overline{Q}$An	QAn	QBn	QCn	$\overline{Q}$Cn

Note X: Don't Care

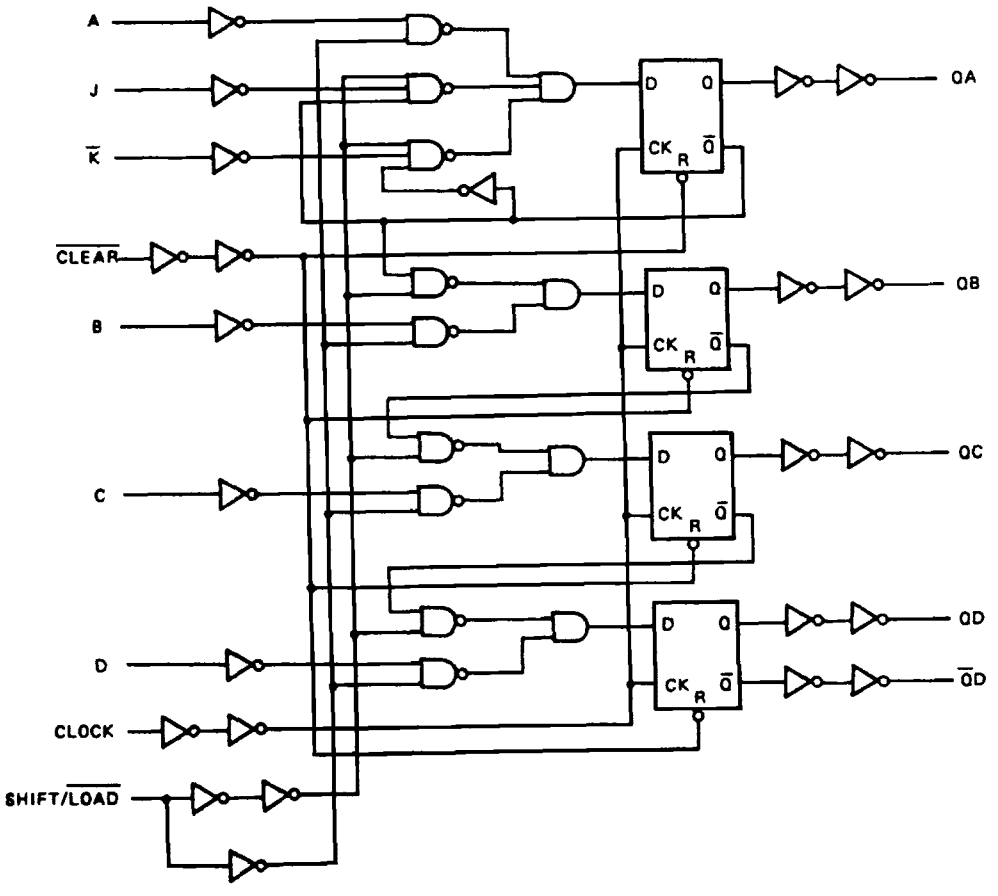
QA0 ~ AD0: No change

AQn ~ ADn: The level of QA, AB, QC, respectively, before the most recent positive transition of the clock.

a...d, $\overline{d}$: The level of steady state input voltage at inputs A ~ D respectively.



Timing Chart



Logic Diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		Ta = 25°C				Ta = -40 ~ 85°C		Unit
				V_{CC}	Min.	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
			I_{OH} = -4 mA I_{OH} = -5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	- -	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	4.0	–	40.0	

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ	Limit	Limit	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$	–	2.0	–	75	95	ns
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$	–	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Setup Time (SI, PI)	t_s	–	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Setup Time (S0, S1)	t_s	-	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Hold Time	t_h	–	2.0	–	0	0	
			4.5	–	0	0	
			6.0	–	0	0	
Minimum Removal Time	t_{rem}	–	2.0	–	5	5	
			4.5	–	5	5	
			6.0	–	5	5	
Clock Frequency	f	–	2.0	–	7	6	MHz
			4.5	–	38	30	
			6.0	–	45	35	

AC Electrical Characteristics (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	4	8	ns
Propagation Delay Time (CLOCK-Qn, $\overline{Qn}$)	t_{pLH} t_{pHL}	–	–	13	21	
Propagation Delay Time ($\overline{CLEAR}$-Qn, $\overline{Qn}$)	t_{pHL}	–	–	14	21	
Maximum Clock Frequency	f_{MAX}	–	41	68	–	MHz

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (CLOCK-Q)	t_{pLH} t_{pHL}	–	2.0	–	47	125	–	155	
			4.5	–	16	25	–	31	
			6.0	–	13	21	–	26	
Propagation Delay Time ($\overline{CLEAR}$-Q	t_{pLH} t_{pHL}	–	2.0	–	49	125	–	155	
			4.5	–	17	25	–	31	
			6.0	–	14	21	–	26	
Maximum Clock Frequency	f_{MAX}	–	2.0	7	15	–	6	–	MHz
			4.5	38	60	–	30	–	
			6.0	45	75	–	35	–	
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	–		–	76	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$