

TYPES SN5474, SN54H74, SN54L74, SN54LS74A, SN54S74, SN7474, SN74H74, SN74LS74A, SN74S74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

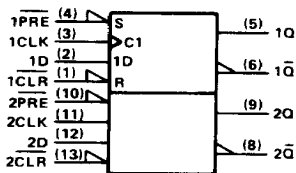
The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [†]	H [†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	\bar{Q}_0

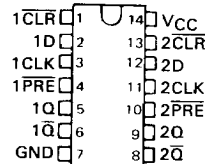
[†] The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

logic symbol

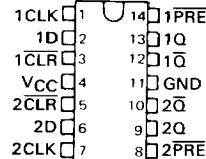


Pin numbers shown on logic notation are for D, J or N packages.

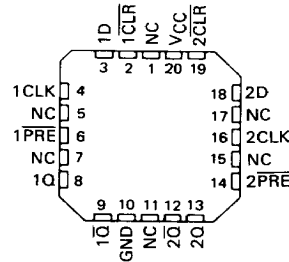
SN5474, SN54H74, SN54L74 ... J PACKAGE
 SN54LS74A, SN54S74 ... J OR W PACKAGE
 SN7474, SN74H74 ... J OR N PACKAGE
 SN74LS74A, SN74S74 ... D, J OR N PACKAGE
 (TOP VIEW)



SN5474, SN54H74 ... W PACKAGE
 (TOP VIEW)

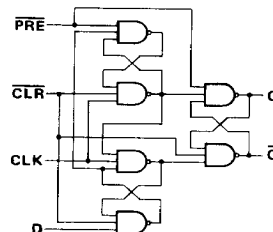


SN54LS74A, SN54S74 ... FK PACKAGE
 SN74LS74A, SN74S74 ... FN PACKAGE
 (TOP VIEW)



NC - No internal connection

logic diagram



PRODUCTION DATA
 This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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3-295

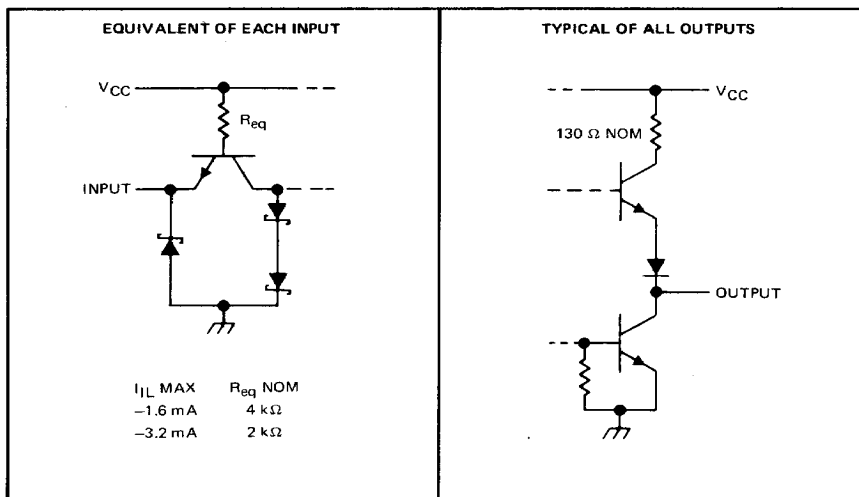
3

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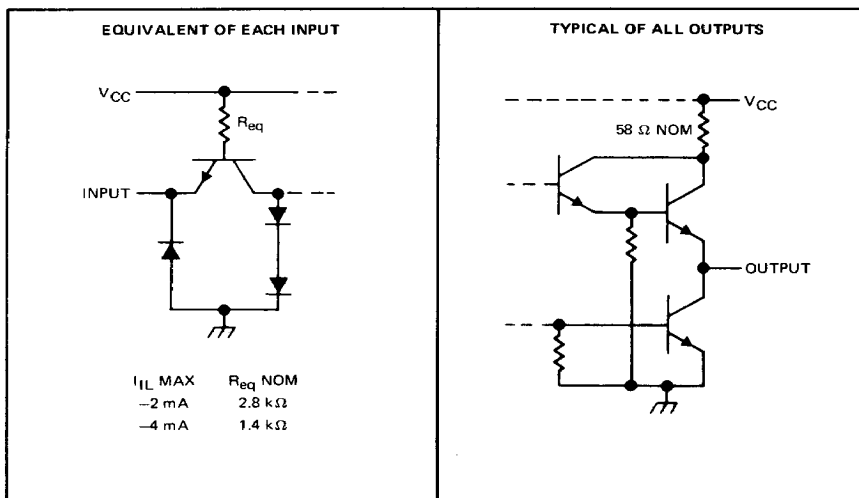
TYPES SN5474, SN54H74, SN7474, SN74H74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematics of inputs and outputs

74



'H74



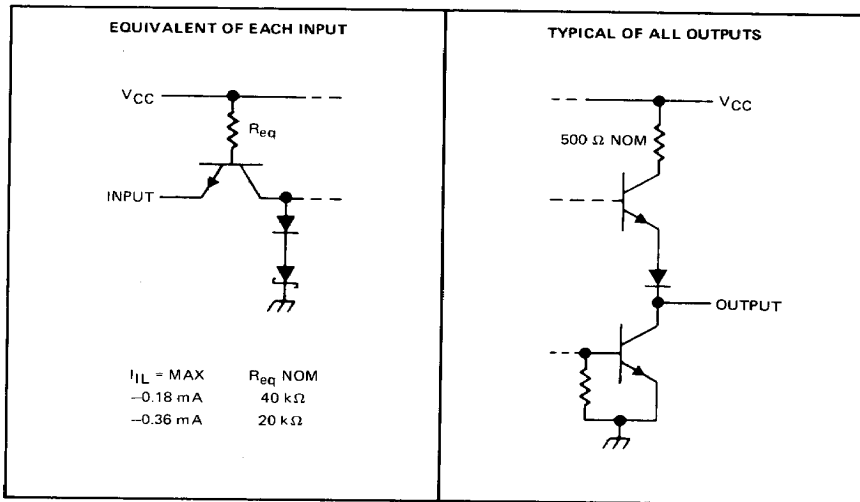
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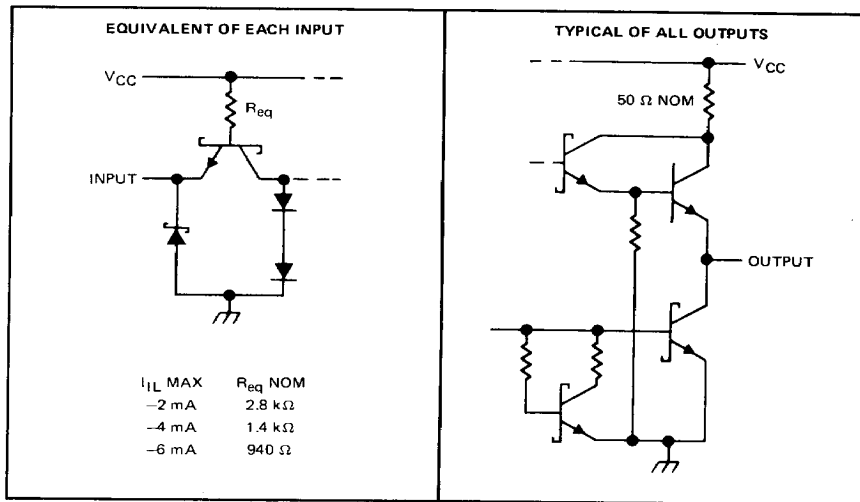
TYPES SN54L74, SN54S74, SN74S74
 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematics of inputs and outputs (continued)

'L74



'S74



3

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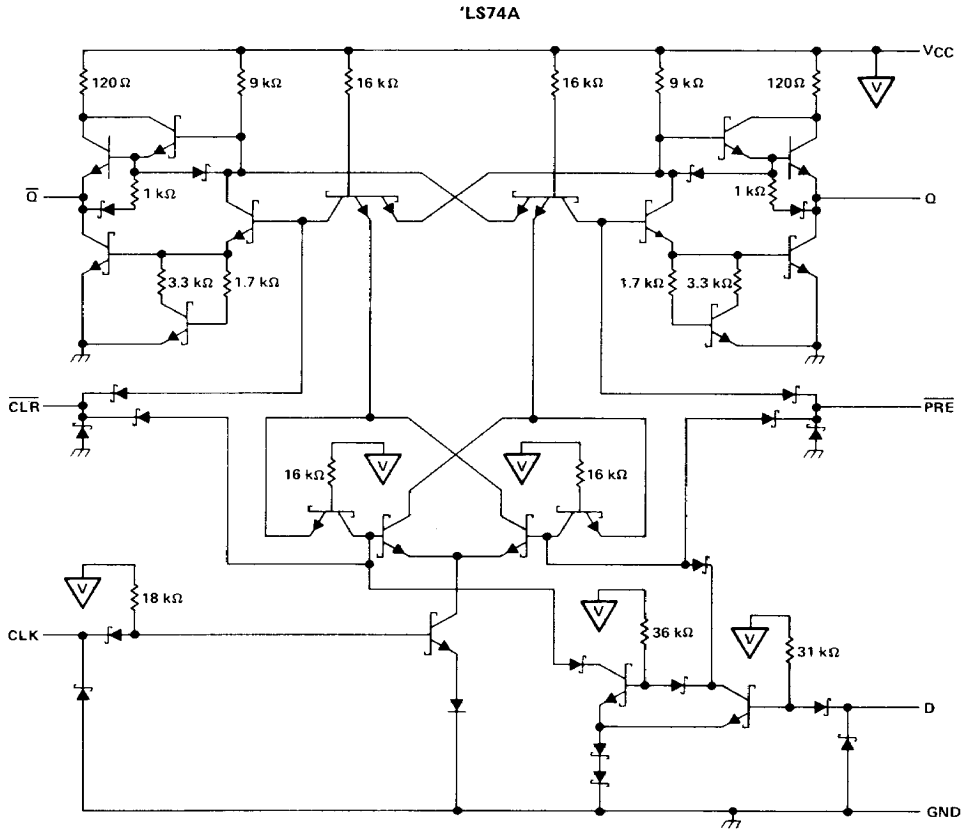
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3-297

TYPES SN5474, SN54H74, SN54L74, SN54LS74A, SN54S74,
 SN7474, SN74H74, SN74LS74A, SN74S74
 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematic



3
 TTL DEVICES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '74, 'H74, 'L74, 'S74	5.5 V
'LS74A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3-298


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TYPES SN5474, SN7474

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

		SN5474			SN7474			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			16			16	mA
t _w	Pulse duration	CLK high		30		30		ns
		CLK low		37		37		
		PRE or CLR low		30		30		
t _{su}	Input setup time before CLK †			20		20		ns
t _h	Input hold time-data after CLK †			5		5		ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5474			SN7474			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.2	0.4		0.2	0.4		V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	D			40			40	mA
	CLR			120			120	
	All Other	V _{CC} = MAX, V _I = 2.4 V			80			
I _{IL}	D			-1.6			-1.6	mA
	PRE*	V _{CC} = MAX, V _I = 0.4 V					-1.6	
	CLR*						-3.2	
	CLK						-3.2	
I _{OS} §	V _{CC} = MAX	-20		-57	-18		-57	mA
I _{CC}	V _{CC} = MAX, See Note 2	8.5	15		8.5	15		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

* Clear is tested with preset high and preset is tested with clear high.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
t _{max}			R _L = 400 Ω, C _L = 15 pF		15	25		MHz	
t _{PLH}	PRE or CLR	Q or \bar{Q}						25	ns
t _{PHL}		Q or \bar{Q}						40	ns
t _{PLH}	CLK	Q or \bar{Q}					14	25	ns
t _{PHL}		Q or \bar{Q}					20	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

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TYPES SN54H74, SN74H74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

	SN54H74			SN74H74			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-1			-1	mA
I _{OL} Low-level output current			20			20	mA
t _w Pulse duration	CLK high	15		15			ns
	CLK low	13.5		13.5			
	CLR or PRE low	25		25			
t _{su} Setup time-before CLK †	High-level data	10		10			ns
	Low-level data	15		15			
t _h Hold time - data after CLK †		5		5			ns
T _A Operating free-air temperature		-55	125		0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54H74			SN74H74			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -8 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	D			50			50	μA
	CLR	V _{CC} = MAX, V _I = 2.4 V		150			150	
	PRE or CLK			100			100	
I _{IL}	D	V _{CC} = MAX, V _I = 0.4 V		-2			-2	mA
	CLR*			-4			-4	
	PRE*			-2			-2	
	CLK			-4			-4	
I _{OS} §	V _{CC} = MAX		-40	-100		-40	-100	mA
I _{CC}	V _{CC} = MAX, See Note 2		15	21		15	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

* Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				35	43		MHz
t _{PLH}	\overline{PRE} or \overline{CLR}	Q or \bar{Q}	R _L = 280 Ω, C _L = 25 pF			20	ns
t _{PHL}						30	ns
t _{PLH}	CLK	Q or \bar{Q}			8.5	15	ns
t _{PHL}					13	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

TYPE SN54L74

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.7	V
I _{OH}	High-level output current			-0.1	mA
I _{OL}	Low-level output current			2	mA
t _w	Pulse duration	CLK high or low		200	ns
		CLR or PRE low		100	
t _{su}	Setup time before CLK †		50		ns
t _h	Hold time data after CLK †		15		ns
T _A	Operating free-air temperature	-55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†				MIN	TYP‡	MAX	UNIT
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.7 V, I _{OH} = -0.1 mA	2.4	3.3				V	
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.7 V, I _{OL} = 2 mA		0.15	0.3			V	
I _I	D	V _{CC} = MAX, V _I = 5.5 V					0.1	mA	
	CLR						0.3		
	PRE or CLK						0.2		
I _{IH}	D	V _{CC} = MAX, V _I = 2.4 V					10	μA	
	CLR						30		
	PRE or CLK						20		
I _{IL}	D or PRE	V _{CC} = MAX, V _I = 0.3 V					-0.18	μA	
	CLR or CLK						-0.36		
I _{OS}		V _{CC} = MAX	-3		-15			mA	
I _{CC}		V _{CC} = MAX, See Note 2		0.8	1.5			mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
f _{max}			R _L = 4 kΩ, C _L = 50 pF	2.5	3		MHz	
t _{PLH}	PRE or CLR	Q or \bar{Q}			50	75	ns	
t _{PHL}	PRE or CLR (CLK high)	\bar{Q} or Q			80	150	ns	
	PRE or CLR (CLK low)				80	150		
t _{PLH}	Clock	Q or \bar{Q}			15	65	100	ns
t _{PHL}					15	65	150	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

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3-301

TYPES SN54LS74A, SN74LS74A DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

		SN54LS74A			SN74LS74A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0		25	0		25	MHz
t _w	Pulse duration	CLK high		25	25			ns
		PRE or CLR low		25	25			
t _{su}	Setup time-before CLK †	High-level data		20	20			ns
		Low-level data		20	20			
t _h	Hold time-data after CLK †	5			5			ns
T _A	Operating free-air temperature	-55			125			0 70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS74A		SN74LS74A		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = MIN,	I _I = -18 mA	-1.5		-1.5		V
V _{OH}		V _{CC} = MIN,	V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4	2.7	3.4	V
V _{OL}		V _{CC} = MIN,	V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V
		V _{CC} = MIN,	V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA			0.35	0.5	
I _I	D or CLK	V _{CC} = MAX,	V _I = 7 V	0.1		0.1		mA
	CLR or PRE			0.2		0.2		
I _{IH}	D or CLK	V _{CC} = MAX,	V _I = 2.7 V	20		20		µA
	CLR or PRE			40		40		
I _{IL}	D or CLK	V _{CC} = MAX,	V _I = 0.4 V	-0.4		-0.4		mA
	CLR or PRE			-0.8		-0.8		
I _{OS} §		V _{CC} = MAX,	See Note 4	-20	-100	-20	-100	mA
I _{CC}		V _{CC} = MAX,	See Note 2	4	8	4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
f _{max}				25	33		MHz	
t _{PLH}	CLR, PRE or CLK	Q or \bar{Q}	R _L = 2 kΩ, C _L = 15 pF			13	25	ns
t _{PHL}						25	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S74, SN74S74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

		SN54S74			SN74S74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.8			0.8			V
I _{OH}	High-level output current	-1			-1			mA
I _{OL}	Low-level output current	20			20			mA
t _w	Pulse duration	CLK high		6	6		ns	
		CLK low		7.3	7.3			
		CLR or PRE low		7	7			
t _{su}	Setup time, before CLK †	High-level data		3	3		ns	
		Low-level data		3	3			
t _h	Input hold time - data after CLK †	2			2			ns
T _A	Operating free-air temperature	-55	125	0	70	°C		

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S74			SN74S74			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA,	-1.2			-1.2			V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4	V	
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA	0.5			0.5			V
I _I	V _{CC} = MAX, V _I = 5.5 V	1			1			mA
I _{IH}	D	50			50			mA
	CLR	150			150			
	PRE or CLK	100			100			
I _{IL}	D	-2			-2			mA
	CLR*	-6			-6			
	PRE*	-4			-4			
	CLK	-4			-4			
I _{OS} §	V _{CC} = MAX	-40	-100		-40	-100	mA	
I _{CC}	V _{CC} = MAX, See Note 2	15	25		15	25	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

* Clear is tested with preset high and preset is tested with clear high.

NOTE 2: All outputs open. I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				75	110		MHz
t _{PLH}	PRE or CLR	Q or \bar{Q}	R _L = 280 Ω, C _L = 15 pF	4	6	6	ns
t _{PHL}	PRE or CLR (CLK high)	\bar{Q} or Q		9	13.5		ns
	PRE or CLR (CLK low)			5	8		ns
t _{PLH}	CLK	Q or \bar{Q}		6	9	9	ns
t _{PHL}			6	9	9	ns	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3
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3-303