

SN74LS640, SN74LS641, SN74LS642, SN74LS645

Octal Bus Transceivers

These octal bus transceivers are designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. These circuits allow data transmission from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. Enable input (\bar{G}) can disable the device so that the buses are effectively isolated.

DEVICE	OUTPUT	LOGIC
LS640	3-State	Inverting
LS641	Open-Collector	True
LS642	Open-Collector	Inverting
LS645	3-State	True

FUNCTION TABLE

CONTROL INPUTS		OPERATION	
\bar{G}	DIR	LS640 LS642	LS641 LS645
L	L	\bar{B} data to A bus	B data to A bus
L	H	\bar{A} data to B bus	A data to B bus
H	X	Isolation	Isolation

H = HIGH Level, L = LOW Level, X = Irrelevant

GUARANTEED OPERATING RANGES (SN74LS640, SN74LS645)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			-3.0	mA
				-15	mA
I_{OL}	Output Current – Low			24	mA

GUARANTEED OPERATING RANGES (SN74LS641, SN74LS642)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
V_{OH}	Output Voltage – High			5.5	V
I_{OL}	Output Current – Low			24	mA

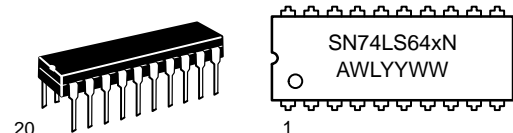


ON Semiconductor

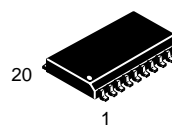
<http://onsemi.com>

LOW POWER SCHOTTKY

MARKING DIAGRAMS



PDIP-20
N SUFFIX
CASE 738



SOIC-20
DW SUFFIX
CASE 751D

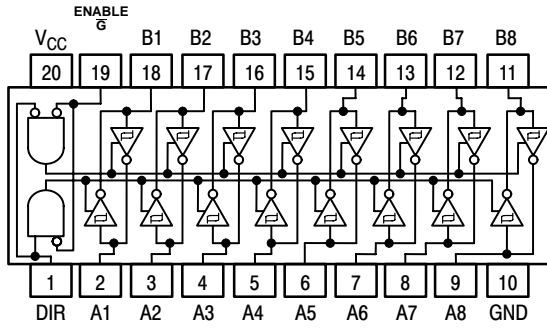
x = 0, 1, 2, or 5
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

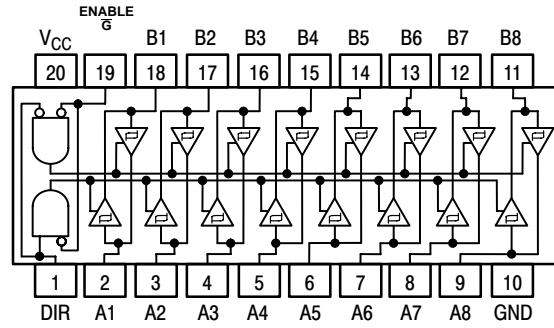
Device	Package	Shipping
SN74LS640N	PDIP-20	1440 Units/Box
SN74LS640DW	SOIC-20	2500/Tape & Reel
SN74LS641N	PDIP-20	1440 Units/Box
SN74LS641DW	SOIC-20	2500/Tape & Reel
SN74LS642N	PDIP-20	1440 Units/Box
SN74LS642DW	SOIC-20	2500/Tape & Reel
SN74LS645N	PDIP-20	1440 Units/Box

SN74LS640, SN74LS641, SN74LS642, SN74LS645

CONNECTION DIAGRAMS DIP (TOP VIEW)



SN74LS640
SN74LS642



SN74LS641
SN74LS645

SN74LS640, SN74LS641, SN74LS642, SN74LS645

SN74LS640 • SN74LS645

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.6	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.4	3.4		V	V _{CC} = MIN, I _{OH} = 3.0 mA
		2.0			V	V _{CC} = MIN, I _{OH} = MAX
V _{OL}	Output LOW Voltage		0.25	0.4	V	I _{OL} = 12 mA
			0.35	0.5	V	I _{OL} = 24 mA
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW			-400	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current	A or B, DIR or \overline{G}		20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		DIR or \overline{G}		0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
		A or B		0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Output Short Circuit Current (Note 1.)	-40		-225	mA	V _{CC} = MAX
I _{CC}	Power Supply Current					
	Total Output HIGH			70	mA	V _{CC} = MAX
	Total, Output LOW			90		
Total at HIGH Z			95			

1. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS640			LS645				
		Min	Typ	Max	Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay A to B		6.0 8.0	10 15		8.0 11	15 15	ns	C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay B to A		6.0 8.0	10 15		8.0 11	15 15		
t _{PZL} t _{PZH}	Output Enable Time \overline{G} , DIR to A		31 23	40 40		31 26	40 40		
t _{PZL} t _{PZH}	Output Enable Time \overline{G} , DIR to B		31 23	40 40		31 26	40 40		
t _{PLZ} t _{PHZ}	Output Disable Time \overline{G} , DIR to A		15 15	25 25		15 15	25 25		
t _{PLZ} t _{PHZ}	Output Disable Time \overline{G} , DIR to B		15 15	25 25		15 15	25 25		

SN74LS640, SN74LS641, SN74LS642, SN74LS645

SN74LS641 • SN74LS642

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.6	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
I _{OH}	Output HIGH Current			100	μA	V _{CC} = MIN, V _{OH} = MAX
V _{OL}	Output LOW Voltage		0.25	0.4	V	I _{OL} = 12 mA
			0.35	0.5	V	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				-0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{CC}	Power Supply Current Total, Output HIGH			70	mA	V _{CC} = MAX
	Total, Output LOW			90		
	Total at HIGH Z			95		

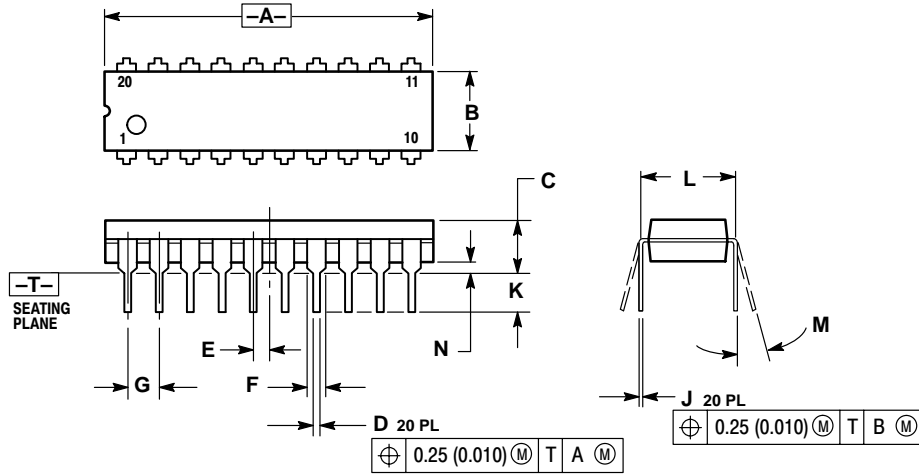
AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS641			LS642				
		Min	Typ	Max	Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, A to B		17 16	25 25		19 14	25 25	ns	C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, B to A		17 16	25 25		19 14	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, G̅, DIR to A		23 34	40 50		26 43	40 60	ns	
t _{PLH} t _{PHL}	Propagation Delay, G̅, DIR to B		25 37	40 50		28 39	40 60	ns	

SN74LS640, SN74LS641, SN74LS642, SN74LS645

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 738-03
ISSUE E



NOTES:

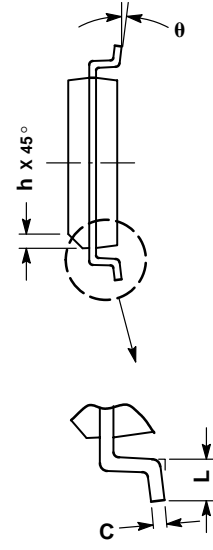
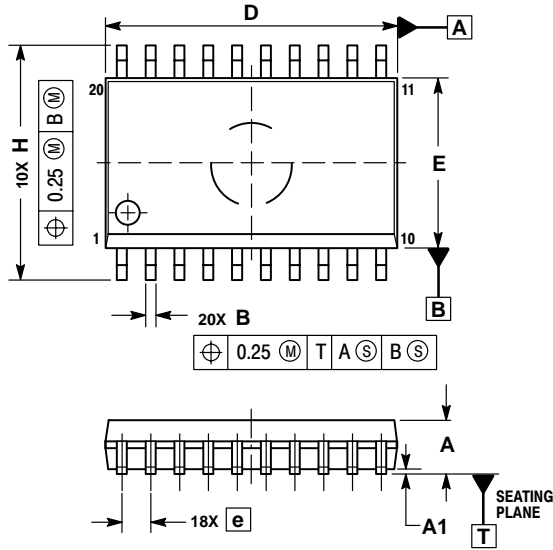
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0° to 15°		0° to 15°	
N	0.020	0.040	0.51	1.01

SN74LS640, SN74LS641, SN74LS642, SN74LS645

PACKAGE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751D-05 ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031

Phone: 81-3-5740-2745
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.