SN74LS640, SN74LS641, SN74LS642, SN74LS645

Octal Bus Transceivers

These octal bus transceivers are designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. These circuits allow data transmission from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. Enable input ($\overline{G}$) can disable the device so that the buses are effectively isolated.

DEVICE	OUTPUT	LOGIC
LS640	3-State	Inverting
LS641	Open-Collector	True
LS642	Open-Collector	Inverting
LS645	3-State	True

FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	LS640 LS642	LS641 LS645
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

H = HIGH Level, L = LOW Level, X = Irrelevant

GUARANTEED OPERATING RANGES (SN74LS640, SN74LS645)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–3.0	mA
				–15	mA
I_{OL}	Output Current – Low			24	mA

GUARANTEED OPERATING RANGES (SN74LS641, SN74LS642)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
V_{OH}	Output Voltage – High			5.5	V
I_{OL}	Output Current – Low			24	mA

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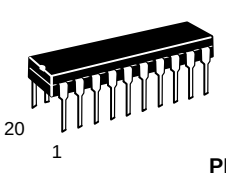
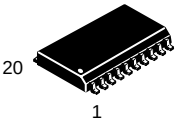
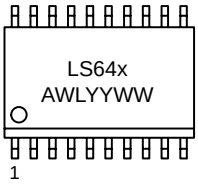
LOW POWER SCHOTTKY

MARKING DIAGRAMS



PDIP–20
N SUFFIX
CASE 738





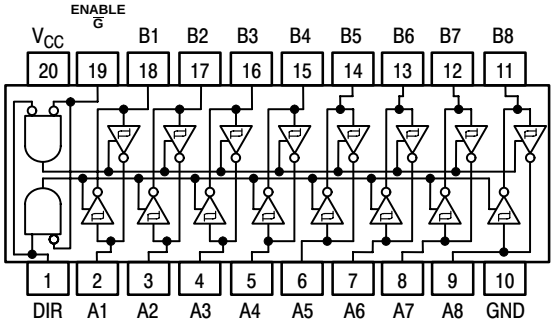
SOIC–20
DW SUFFIX
CASE 751D

x = 0, 1, 2, or 5
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

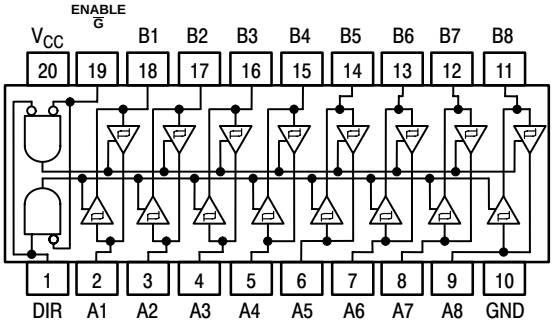
ORDERING INFORMATION

Device	Package	Shipping
SN74LS640N	PDIP–20	1440 Units/Box
SN74LS640DW	SOIC–20	2500/Tape & Reel
SN74LS641N	PDIP–20	1440 Units/Box
SN74LS641DW	SOIC–20	2500/Tape & Reel
SN74LS642N	PDIP–20	1440 Units/Box
SN74LS642DW	SOIC–20	2500/Tape & Reel
SN74LS645N	PDIP–20	1440 Units/Box

CONNECTION DIAGRAMS DIP (TOP VIEW)



SN74LS640
SN74LS642



SN74LS641
SN74LS645

SN74LS640 • SN74LS645

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.6	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage			–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage		2.4	3.4		V	V_{CC} = MIN, I_{OH} = 3.0 mA	
			2.0			V	V_{CC} = MIN, I_{OH} = MAX	
V_{OL}	Output LOW Voltage			0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
				0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				–400	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current	A or B, DIR or $\overline{G}$			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		DIR or $\overline{G}$			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		A or B			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current				–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 1.)		–40		–225	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total Output HIGH				70	mA	V_{CC} = MAX	
	Total, Output LOW				90			
	Total at HIGH Z				95			

1. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits LS640 Min	LS640 Typ	LS640 Max	LS645 Min	LS645 Typ	LS645 Max	Unit	Test Conditions
t_{PLH} t_{PHL}	Propagation Delay A to B		6.0 8.0	10 15		8.0 11	15 15	ns	C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay B to A		6.0 8.0	10 15		8.0 11	15 15	ns	
t_{PZL} t_{PZH}	Output Enable Time $\overline{G}$, DIR to A		31 23	40 40		31 26	40 40	ns	
t_{PZL} t_{PZH}	Output Enable Time $\overline{G}$, DIR to B		31 23	40 40		31 26	40 40	ns	
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{G}$, DIR to A		15 15	25 25		15 15	25 25	ns	C_L = 5.0 pF
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{G}$, DIR to B		15 15	25 25		15 15	25 25	ns	

SN74LS641 • SN74LS642

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

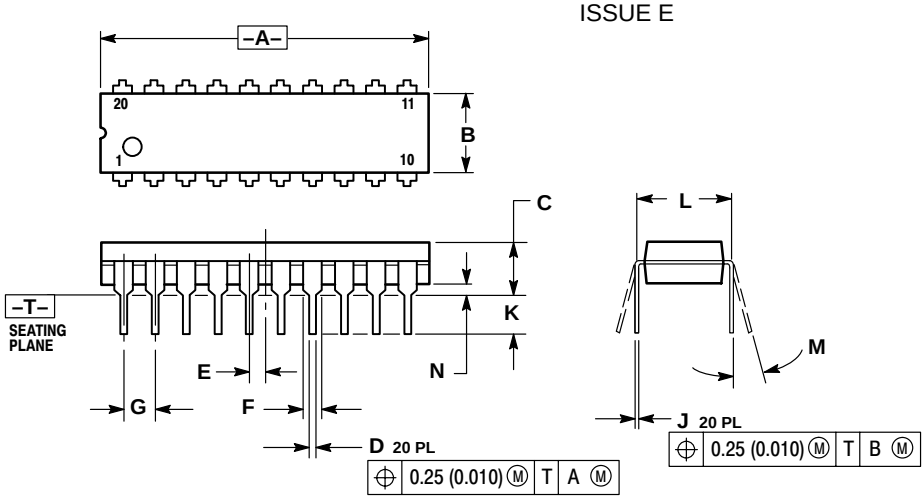
Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.6	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
I_{OH}	Output HIGH Current			100	μA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 24 mA	
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
				–0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current Total, Output HIGH			70	mA	V_{CC} = MAX	
	Total, Output LOW			90			
	Total at HIGH Z			95			

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS641			LS642				
		Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, A to B		17 16	25 25		19 14	25 25	ns	C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, B to A		17 16	25 25		19 14	25 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, DIR to A		23 34	40 50		26 43	40 60	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, DIR to B		25 37	40 50		28 39	40 60	ns	

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 738–03
ISSUE E

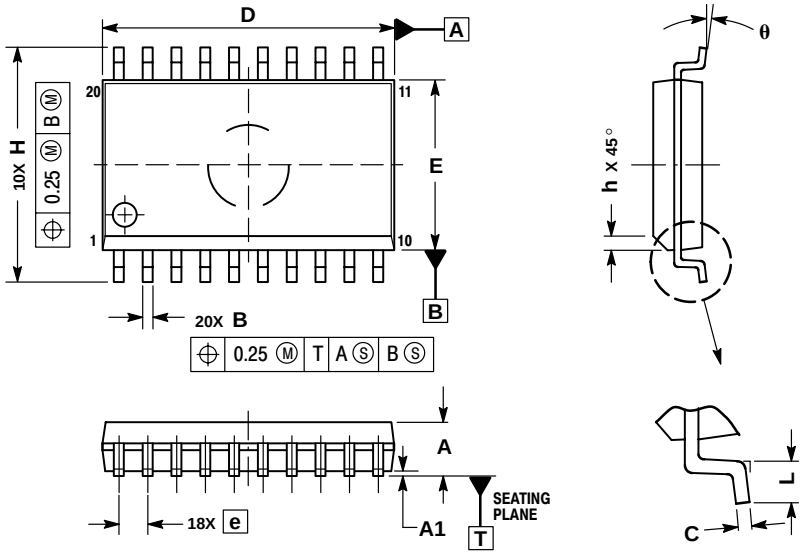


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

Notes

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