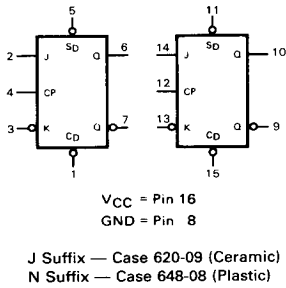


SN54/74LS109A

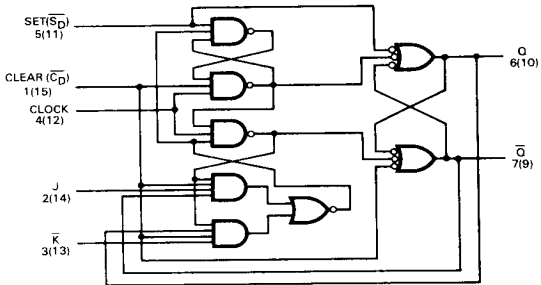
DESCRIPTION — The SN54LS/74LS109A consists of two high speed completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop by simply connecting the J and K pins together.

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP LOW POWER SCHOTTKY

LOGIC SYMBOL



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		74	2.7	3.5	V	
V_{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $I_{OL} = 8.0 \text{ mA}$ $V_{CC} = V_{CC \text{ MIN}}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74	0.35	0.5	V	
I_{IH}	Input HIGH Current J, \bar{K} , Clock Set, Clear			20 40	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
	J, \bar{K} , Clock Set, Clear			0.1 0.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current J, \bar{K} , Clock Set, Clear			-0.4 -0.8	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Output Short Circuit Current	-20		-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current			8.0	mA	$V_{CC} = \text{MAX}$

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\overline{S}_D	\overline{C}_D	J	\overline{K}	Q	\overline{Q}
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	\overline{q}
Toggle	H	H	h	l	\overline{q}	q
Load "0" (Reset)	H	H	l	l	L	H

*Both outputs will be HIGH while both \overline{S}_D and \overline{C}_D are LOW, but the output states are unpredictable if \overline{S}_D and \overline{C}_D go HIGH simultaneously.

H,h = HIGH Voltage Level
 L,l = LOW Voltage Level
 X = Don't Care

I, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f _{MAX}	Maximum Clock Frequency	25	33		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH}	Clock, Clear, Set to Output		13	25	ns	
t _{PHL}			25	40	ns	

AC SET UP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t _W	Clock High Clear, Set Pulse Width	25			ns	V _{CC} = 5.0 V
t _s	Data Setup Time — HIGH	35			ns	
	LOW	25			ns	
t _h	Hold Time	5.0			ns	

FAST AND LS TTL DATA