

# TYPES SN54H102, SN74H102 AND-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These monolithic J-K flip-flops are negative-edge-triggered. They feature gated J-K inputs and an asynchronous clear input. The AND gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

The SN54H102 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74H102 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	$H^{\dagger}$	$\bar{Q}_0^{\dagger}$
H	H	$\downarrow$	L	L	$Q_0$	$\bar{Q}_0$
H	H	$\downarrow$	H	L	H	L
H	H	$\downarrow$	L	H	L	H
H	H	$\downarrow$	H	H	TOGGLE	TOGGLE
H	H	H	X	X	$Q_0$	$\bar{Q}_0$

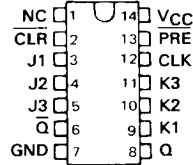
$\dagger$  This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## positive logic

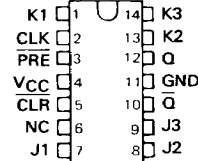
$$J = J1 \cdot J2 \cdot J3$$

$$K = K1 \cdot K2 \cdot K3$$

SN54H102 . . . J PACKAGE  
SN74H102 . . . J OR N PACKAGE  
(TOP VIEW)

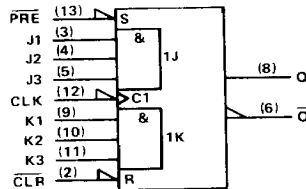


SN54H102 . . . W PACKAGE  
(TOP VIEW)



NC - No internal connection

## logic symbol



Pin numbers shown are for J and N packages.

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**PRODUCTION DATA**  
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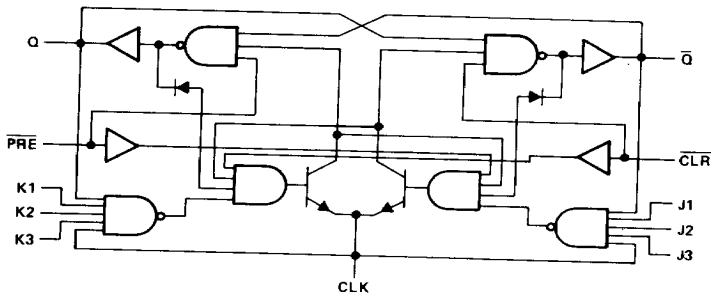
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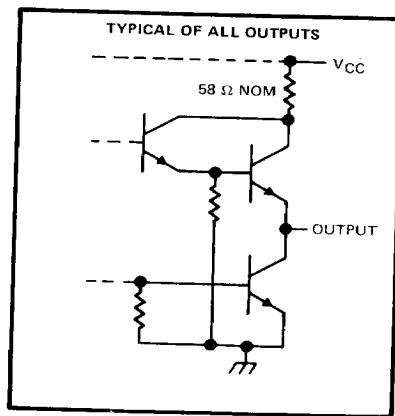
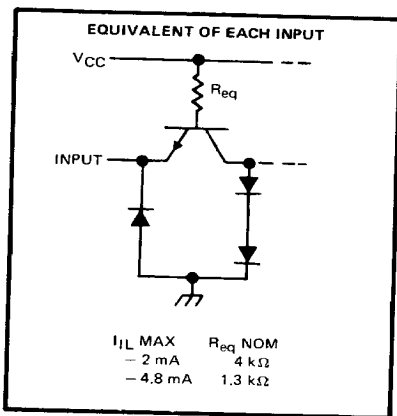
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**TYPES SN54H102, SN74H102  
AND-GATED J-K NEGATIVE-EDGE-TRIGGERED  
FLIP-FLOPS WITH PRESET AND CLEAR**

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54H'	- 55°C to 125°C
SN74H'	0°C to 70°C
Storage temperature range	- 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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# TYPES SN54H102, SN74H102 AND-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

## recommended operating conditions

		SN54H102			SN74H102			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage	0.8			0.8			V
I <sub>OH</sub>	High-level output current	-0.5			-0.5			mA
I <sub>OL</sub>	Low-level output current	20			20			mA
t <sub>w</sub>	Pulse duration	CLK high	10		10		ns	
		CLK low	15		15			
		CLR or PRE low	16		16			
t <sub>su</sub>	Setup time before CLK ↓	High-level data	10		10		ns	
		Low-level data	13		13			
t <sub>h</sub>	Hold time data after CLK ↓	0			0			ns
T <sub>A</sub>	Operating free-air temperature	-55	125		0	70		°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54H102			SN74H102			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -8 mA	-1.5			-1.5			V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -0.5 mA, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V	2.4	3.4		2.4	3.4	V	
V <sub>OL</sub>	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 20 mA, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V	0.2 0.4		0.2 0.4			V	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1			1			mA
I <sub>IH</sub>	Any J or K CLR PRE CLK V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V	50			50			μA
		100			100			
		100			100			
		0	-1	0	-1	0	-1	
I <sub>IL</sub>	Any J or K CLR PRE CLK V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-1 -2			-1 -2			mA
		-1 -2			-1 -2			
		-1 -2			-1 -2			
		-3 -4.8			-3 -4.8			
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-40	-100		-40	-100	mA	
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 2	20	38		20	38	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>				40	50		MHz
t <sub>PLH</sub>	PRE or CLR	Q or $\bar{Q}$	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 25 pF	8	12		ns
t <sub>PHL</sub>	PRE or CLR (CLK high)	$\bar{Q}$ or Q		15	20		ns
	PRE or CLR (CLK low)			23	35		ns
t <sub>PLH</sub>	CLK	Q or $\bar{Q}$		10	15		ns
t <sub>PHL</sub>				16	20		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

  
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