## description

These devices contain an 8-input positive-NAND gate and perform the following Boolean functions in positive logic:
$\left.\begin{array}{l}Y=\bar{A} \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H\end{array}\right) r$

SN54ALS30A, SN54AS30 . . . J PACKAGE
SN74ALS30A, SN74AS30 . . . D OR N PACKAGE SN74AS30 . . . DB PACKAGE
(TOP VIEW)


SN54ALS30A, SN54AS30 . . . FK PACKAGE (TOP VIEW)


NC - No internal connection

ORDERING INFORMATION

| $\mathrm{T}_{\mathbf{A}}$ | PACKAGE $\dagger$ |  | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
| :---: | :---: | :---: | :---: | :---: |
| $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | PDIP - N | Tube | SN74ALS30AN | SN74ALS30AN |
|  |  |  | SN74AS30N | SN74AS30N |
|  | SOIC - D | Tube | SN74ALS30AD | ALS30A |
|  |  | Tape and reel | SN74ALS30AD |  |
|  |  | Tube | SN74AS30D | AS30 |
|  |  | Tape and reel | SN74AS30D |  |
|  | SSOP - DB | Tape and reel | SN74AS30DBR | AS30 |
| $-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | CDIP - J | Tube | SNJ54ALS30AJ | SNJ54ALS30AJ |
|  |  |  | SNJ54AS30J | SNJ54AS30J |
|  | LCCC - FK | Tube | SNJ54ALS30AFK | SNJ54ALS30AFK |
|  |  |  | SNJ54AS30FK | SNJ54AS30FK |

$\dagger$ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE

| INPUTS | OUTPUT <br> $\mathbf{Y}-\mathbf{H}$ |
| :---: | :---: |
| All inputs H | L |
| One or more inputs L | H |

## logic symbol $\dagger$


$\dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the $\mathrm{D}, \mathrm{DB}, \mathrm{J}$, and N packages.

## logic diagram (positive logic)



Pin numbers shown are for the $\mathrm{D}, \mathrm{DB}, \mathrm{J}$, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted) $\ddagger$

Supply voltage range, $\mathrm{V}_{\mathrm{CC}}$ -0.5 V to 7 V

Package thermal impedance, $\theta_{\mathrm{JA}}$ (see Note 1): D package ........................................ 86 ${ }^{\circ} \mathrm{C} / \mathrm{W}$
DB package .......................................... $96^{\circ} \mathrm{C} / \mathrm{W}$
N package ............................................ $80^{\circ} \mathrm{C} / \mathrm{W}$

$\ddagger$ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions


$\dagger$ Applies to the 'AS30 and SN74ALS30A across the full operating temperature range, and SN54ALS30A over the temperature range of $-55^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.
$\ddagger$ Applies to the SN54ALS30A over the temperature range of $70^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS |  |  | MIN | TYP§ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IK }}$ | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$, | $\mathrm{I}=-18 \mathrm{~mA}$ | 'ALS30A |  |  | -1.5 | V |
|  |  |  | 'AS30 |  |  | -1.2 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ to 5.5 V | $\mathrm{IOH}=-0.4 \mathrm{~mA}$ | 'ALS30A | $\mathrm{V}_{\mathrm{CC}}-2$ |  |  | V |
|  |  | $\mathrm{IOH}=-2 \mathrm{~mA}$ | 'AS30 | $\mathrm{V}_{\mathrm{CC}}{ }^{-2}$ |  |  |  |
| VOL | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ | $\mathrm{I} \mathrm{OL}=4 \mathrm{~mA}$ | 'ALS30A |  | 0.25 | 0.4 | V |
|  |  | $\mathrm{I} \mathrm{OL}=8 \mathrm{~mA}$ | SN74ALS30A |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{I} \mathrm{OL}=20 \mathrm{~mA}$ | 'AS30 |  | 0.35 | 0.5 |  |
| 1 | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| 1 IH | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}$ | 'ALS30A |  |  | -0.1 | mA |
|  |  |  | 'AS30 |  |  | -0.5 |  |
| $10 \\|$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{O}}=2.25 \mathrm{~V}$ | SN54ALS30A | -20 |  | -112 | mA |
|  |  |  | SN74ALS30A | -30 |  | -112 |  |
|  |  |  | 'AS30 | -30 |  | -112 |  |
| ICCH | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $V_{1}=0$ | 'ALS30A |  | 0.22 | 0.36 | mA |
|  |  |  | 'AS30 |  | 0.9 | 1.5 |  |
| ICCL | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{I}}=4.5 \mathrm{~V}$ | 'ALS30A |  | 0.54 | 0.9 | mA |
|  |  |  | 'AS30 |  | 3 | 4.9 |  |

[^0]switching characteristics over recommended operating free-air temperature range (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) |  | MIN | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tPLH | A, B, C, D, E, F, G, or H | Y | SN54ALS30A | 3 | 15 | ns |
|  |  |  | SN74ALS30A | 3 | 10 |  |
|  |  |  | SN54AS30 | 1 | 5.5 |  |
|  |  |  | SN74AS30 | 1 | 5 |  |
| tPHL | A, B, C, D, E, F, G, or H | Y | SN54ALS30A | 3 | 15 | ns |
|  |  |  | SN74ALS30A | 3 | 12 |  |
|  |  |  | SN54AS30 | 1 | 5 |  |
|  |  |  | SN74AS30 | 1 | 4.5 |  |

## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


VOLTAGE WAVEFORMS PULSE DURATIONS


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS


VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES: A. $C_{L}$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3 -state outputs, switch S1 is open.
D. All input pulses have the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}}=2 \mathrm{~ns}$, duty cycle $=50 \%$.

E . The outputs are measured one at a time with one input transition per measurement.
Figure 1. Load Circuits and Voltage Waveforms

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[^0]:    § All typical values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    II The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

