

SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDAS220B – DECEMBER 1982 – REVISED DECEMBER 1994

- **Multiplexed I/O Ports Provide Improved Bit Density**
- **Four Modes of Operation:**
 - Hold (Store)
 - Shift Right
 - Shift Left
 - Load Data
- **Operate With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for n-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
 - Stacked or Push-Down Registers
 - Buffer Storage
 - Accumulator Registers
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

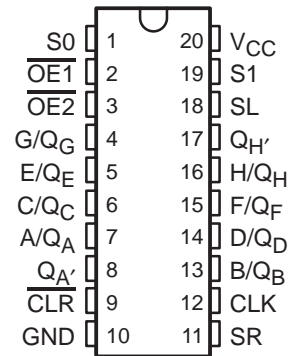
description

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S_0 , S_1) inputs and two output-enable ($\overline{OE1}$, $\overline{OE2}$) inputs can be used to choose the modes of operation listed in the function table.

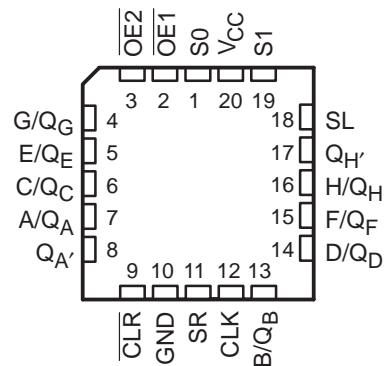
Synchronous parallel loading is accomplished by taking both S_0 and S_1 high. This places the 3-state outputs in the high-impedance state and permits data applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when the clear (\overline{CLR}) input is low. Taking either $\overline{OE1}$ or $\overline{OE2}$ high disables the outputs, but has no effect on clearing, shifting, or storing data.

The SN54ALS299 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS299 is characterized for operation from 0°C to 70°C .

SN54ALS299 . . . J PACKAGE
SN74ALS299 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS299 . . . FK PACKAGE
(TOP VIEW)



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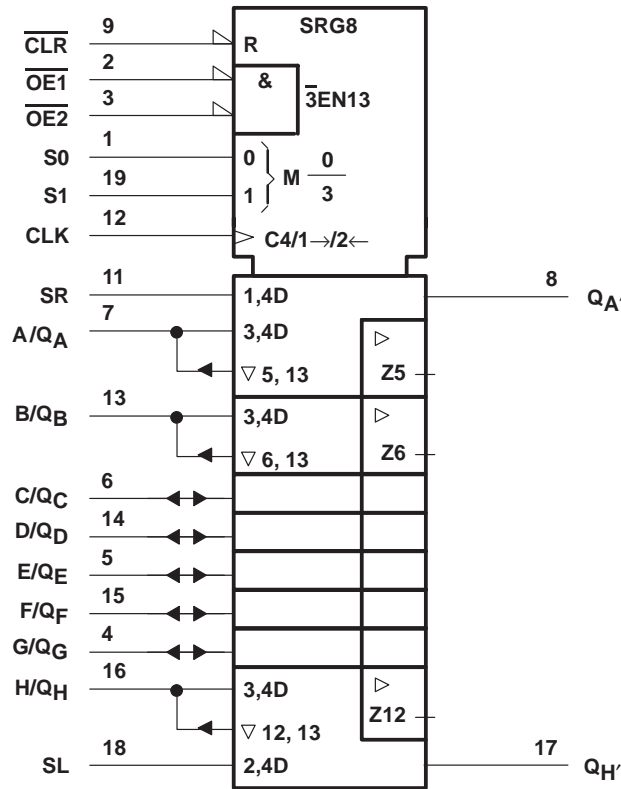
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS			
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'		
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	↑	X	H	H	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	H	QH	H	QH
	H	L	H	L	L	↑	X	L	L	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	L	QH	L	QH
Shift Left	H	H	L	L	L	↑	H	X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	H	QB _n	H	QB _n	H
	H	H	L	L	L	↑	L	X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	L	QB _n	L	QB _n	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbol‡

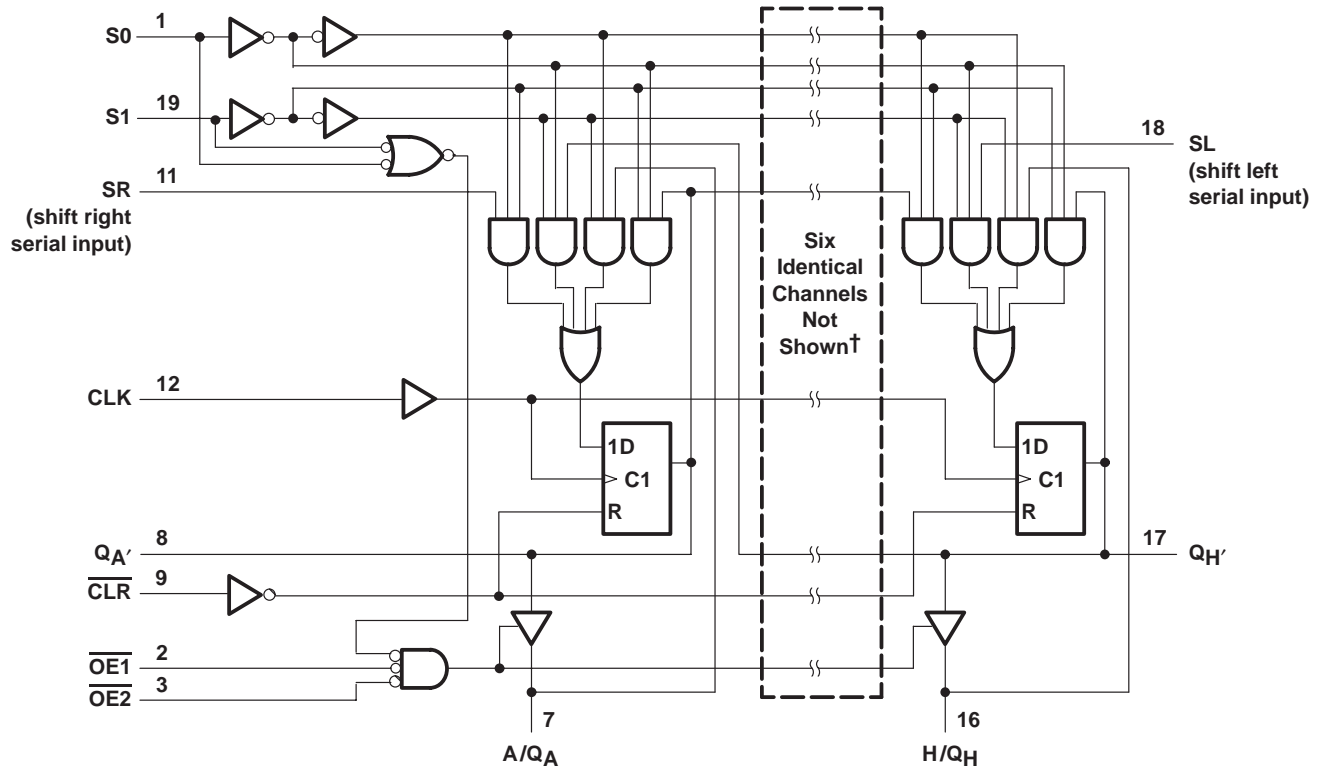


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDAS220B – DECEMBER 1982 – REVISED DECEMBER 1994

logic diagram (positive logic)



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T_A : SN54ALS299	-55°C to 125°C
SN74ALS299	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS299, SN74ALS299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

WITH 3-STATE OUTPUTS

SDAS220B – DECEMBER 1982 – REVISED DECEMBER 1994

recommended operating conditions

		SN54ALS299			SN74ALS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current	Q_A' or Q_H'		-0.4		-0.4		mA
		$Q_A - Q_H$		-1		-2.6		
I_{OL}	Low-level output current	Q_A' or Q_H'		4		8		mA
		$Q_A - Q_H$		12		24		
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS299			SN74ALS299			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$		-1.5			-1.5			V
V_{OH}	All outputs	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V
	$Q_A - Q_H$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$		2.4	3.3			V	
			$I_{OH} = -2.6\text{ mA}$				2.4	3.2		
V_{OL}	Q_A' or Q_H'	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$		0.25	0.4	0.25	0.4	V	
			$I_{OL} = 8\text{ mA}$				0.35	0.5		
	$Q_A - Q_H$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$		0.25	0.4	0.25	0.4		
			$I_{OL} = 24\text{ mA}$				0.35	0.5		
I_I	A - H	$V_{CC} = 5.5\text{ V}$	$V_I = 5.5\text{ V}$		0.1		0.1		mA	
	Any others		$V_I = 7\text{ V}$		0.1		0.1			
I_{IH}^\ddagger		$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$		20			20	μA	
I_{IL}^\ddagger	S0, S1, SR, SL	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$		-0.2			-0.2		mA
	Any others				-0.1			-0.1		
I_{OS}^\S	Q_A' or Q_H'	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$		-15	-70	-15	-70	mA	
	$Q_A - Q_H$				-20	-112	-30	-112		
I_{CC}		$V_{CC} = 5.5\text{ V}$	Outputs high		15	28	15	28	mA	
			Outputs low		22	38	22	38		
			Outputs disabled		23	40	23	40		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports ($Q_A - Q_H$), the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDAS220B – DECEMBER 1982 – REVISED DECEMBER 1994

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		SN54ALS299		SN74ALS299		UNIT	
		MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency (at 50% duty cycle)	0	17	0	30	MHz	
t_w	Pulse duration	CLK high or low		16.5		ns	
		CLR low		10			
t_{su}	Setup time before CLK \uparrow	S0 or S1		20		ns	
		Serial or parallel data	High		16		
			Low		6		
Inactive-state setup time before CLK \uparrow \dagger		CLR		15			
t_h	Hold time after CLK \uparrow	S0 or S1		0		ns	
		Serial or parallel data		0			

\dagger Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Figure 1)

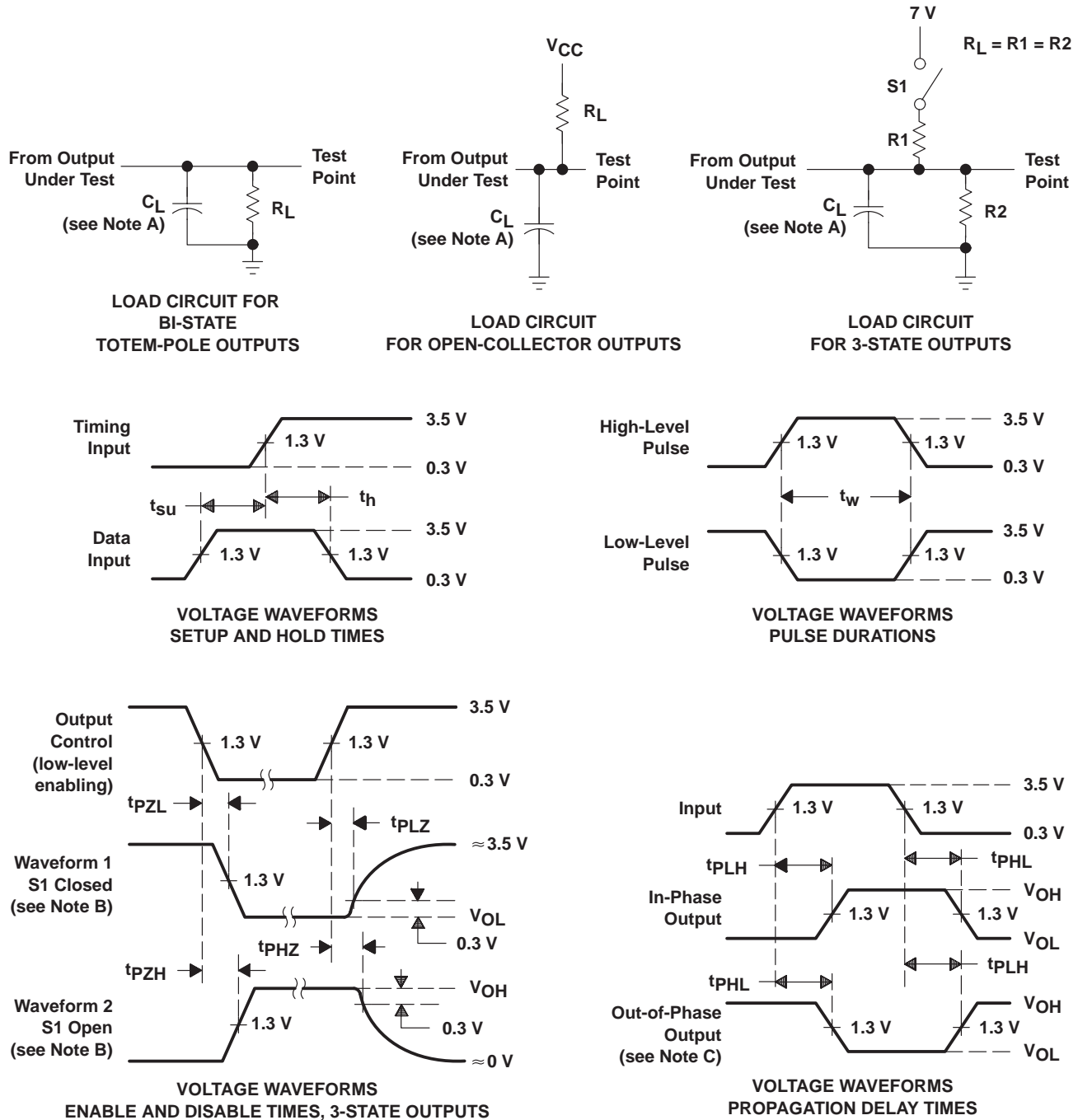
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}\ddagger$				UNIT
			SN54ALS299		SN74ALS299		
			MIN	MAX	MIN	MAX	
f_{max}			17		30		MHz
t_{PLH}	CLK	$Q_A - Q_H$	2	19	4	13	ns
t_{PHL}			4	25	7	19	
t_{PLH}	CLK	$Q_{A'} \text{ or } Q_{H'}$	2	21	5	15	ns
t_{PHL}			4	25	8	18	
t_{PHL}	CLR	$Q_A - Q_H$	6	29	6	22	ns
		$Q_{A'} \text{ or } Q_{H'}$	6	29	6	22	
t_{PZH}	$\overline{OE1}, \overline{OE2}$	$Q_A - Q_H$	5	22	6	16	ns
t_{PZL}			6	27	8	22	
t_{PZH}	S0, S1	$Q_A - Q_H$	5	27	7	17	ns
t_{PZL}			6	26	8	22	
t_{PHZ}	$\overline{OE1}, \overline{OE2}$	$Q_A - Q_H$	1	15	1	8	ns
t_{PLZ}			4	38	5	15	
t_{PHZ}	S0, S1	$Q_A - Q_H$	1	16	1	12	ns
t_{PLZ}			4	34	8	25	

\ddagger For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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SDAS220B – DECEMBER 1982 – REVISED DECEMBER 1994

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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