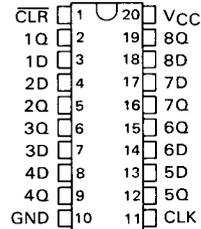


# SN54ALS273, SN74ALS273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

D2661, APRIL 1982—REVISED MAY 1986

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS273 . . . J PACKAGE  
SN74ALS273 . . . DW OR N PACKAGE  
(TOP VIEW)



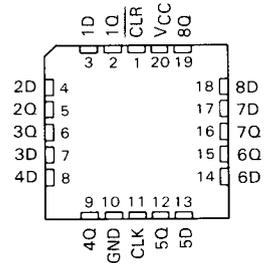
## description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54ALS273 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS273 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

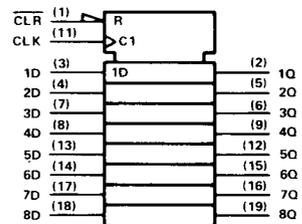
SN54ALS273 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

## logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.



# SN54ALS273, SN74ALS273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS273			SN74ALS273			UNIT
		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -0.4 mA	V <sub>CC</sub> - 2		V <sub>CC</sub> - 2				V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA	2.4	3.3					
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -2.6 mA			2.4	3.2			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA	0.25		0.4		0.25 0.4		V
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 24 mA					0.35 0.5		
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V			0.1		0.1		mA
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			20		20		μA
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V			-0.2		-0.2		mA
I <sub>O</sub> <sup>‡</sup>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-30		-112	-30		-112	mA
I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V			11	20	11 20		mA
I <sub>CCL</sub>	V <sub>CC</sub> = 5.5 V			19	29	19 29		

<sup>†</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>‡</sup>The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX				UNIT
			SN54ALS273		SN74ALS273		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			30		35	MHz	
t <sub>PHL</sub>	CLR	Any Q	4	24	4	18	ns
t <sub>PLH</sub>	CLK	Any Q	2	20	2	12	ns
t <sub>PHL</sub>			3	17	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



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