- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These devices contain a 13-input positive-NAND gate. They perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$$
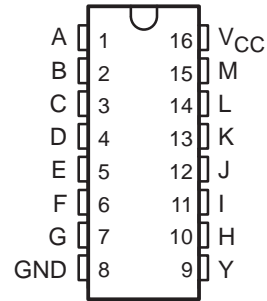$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$$

The SN54ALS133 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS133 is characterized for operation from 0°C to 70°C.
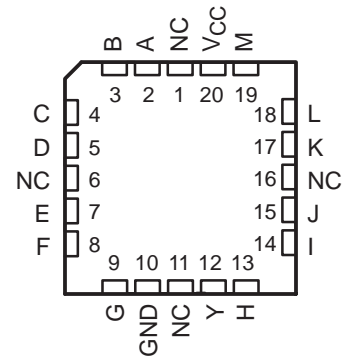
FUNCTION TABLE

INPUTS A – M	OUTPUT Y
All inputs H	L
One or more inputs L	H

SN54ALS133 . . . J PACKAGE
SN74ALS133 . . . D OR N PACKAGE
(TOP VIEW)

A	1		16	V_{CC}

A [1   16] V$_{CC}$
B [2   15] M
C [3   14] L
D [4   13] K
E [5   12] J
F [6   11] I
G [7   10] H
GND [8   9] Y

SN54ALS133 . . . FK PACKAGE
(TOP VIEW)

C [4   18] L
D [5   17] K
NC [6   16] NC
E [7   15] J
F [8   14] I

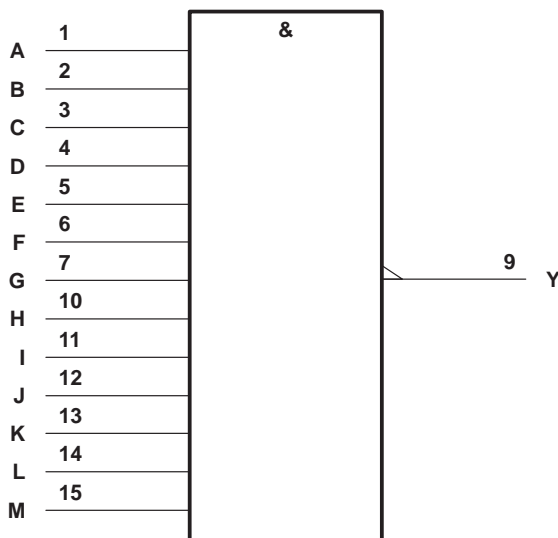Top pins (3 2 1 20 19): B A NC V$_{CC}$ M
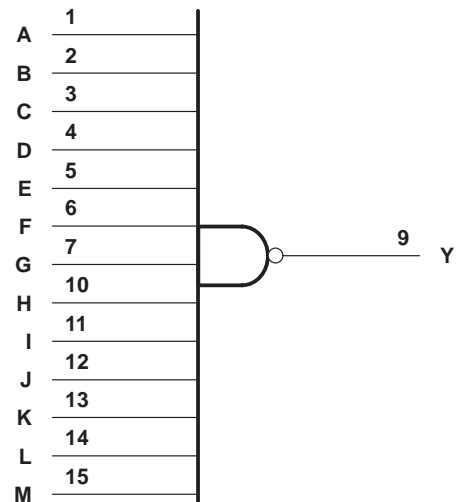Bottom pins (9 10 11 12 13): G GND NC Y H

NC – No internal connection

logic symbol†

logic diagram (positive logic)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . 7 V
Input voltage, V_I . . . . 7 V
Operating free-air temperature range, T_A: SN54ALS133 . . . . −55°C to 125°C
SN74ALS133 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS133			SN74ALS133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8‡			0.8	V
				0.7§				
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

‡ Applies over temperature range −55°C to 70°C
§ Applies over temperature range 70°C to 125°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS133			SN74ALS133			UNIT
			MIN	TYP¶	MAX	MIN	TYP¶	MAX	
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2			−1.5	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC}-2$			$V_{CC}-2$			V
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 4$ mA		0.25	0.5		0.25	0.4	V
		$I_{OL} = 8$ mA					0.35	0.5	
I_I	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	µA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			−0.1			−0.1	mA
I_O#	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	−20		−112	−30		−112	mA
I_{CCH}	$V_{CC} = 5.5$ V,	$V_I = 0$		0.24	0.34		0.24	0.34	mA
I_{CCL}	$V_{CC} = 5.5$ V,	$V_I = 4.5$ V		0.56	0.8		0.56	0.08	mA

¶ All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
# The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS
INSTRUMENTS

switching characteristics (see Figure 1)

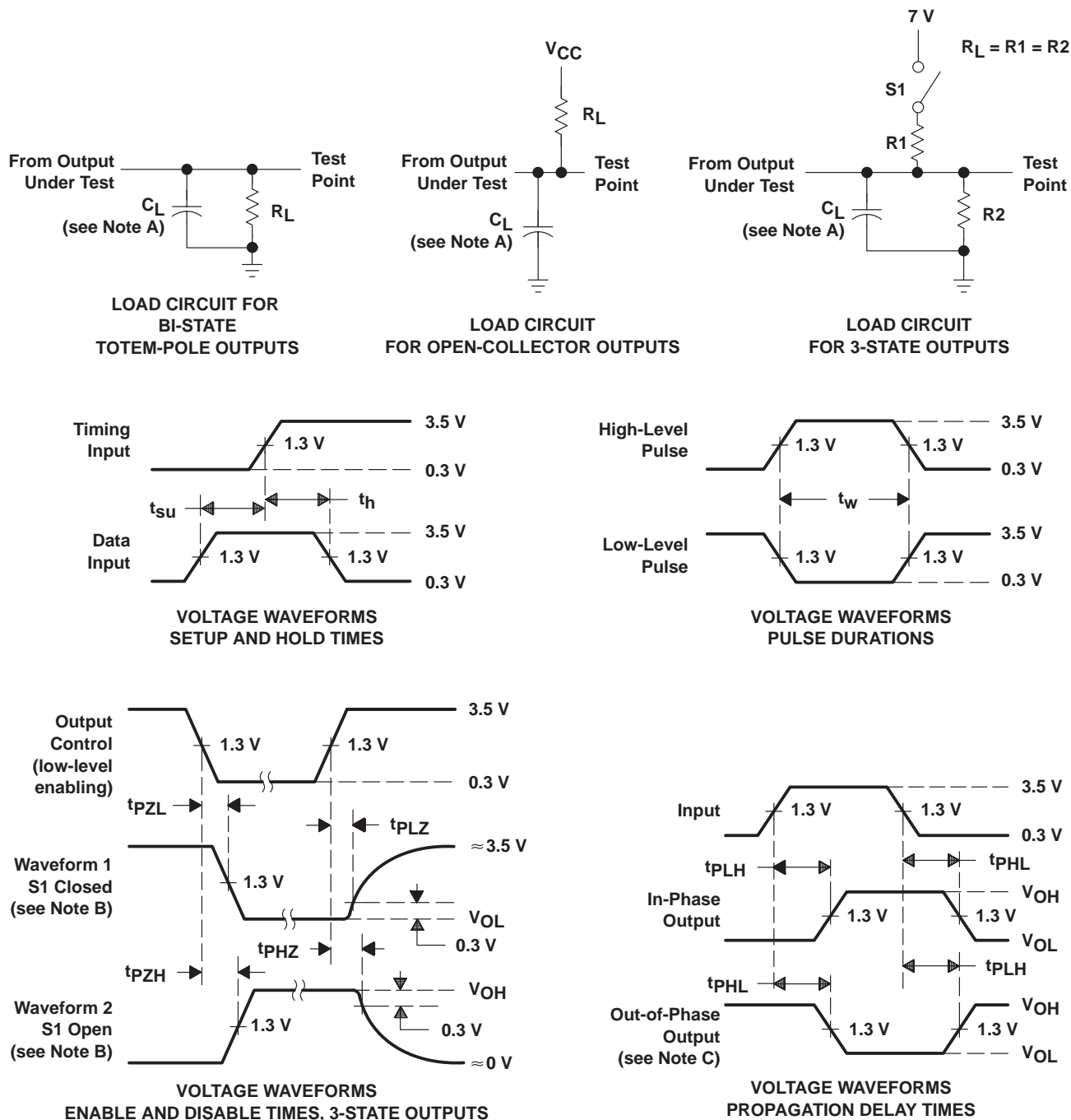| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX[†]				UNIT
			SN54ALS133		SN74ALS133		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	16	3	11	ns
t_{PHL}			1	47	5	25	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

**LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**

**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**

$R_L = R1 = R2$

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
   D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
   E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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