Am54S/74S194•Am54S/74S195

Four-Bit High-Speed Shift Registers

Distinctive Characteristics

- Parallel load or shift right with $J\overline{K}$ inputs on Am54S/74S195
- Shift left, right, parallel load or do nothing on Am54S/74S194
- Fully synchronous shifting and parallel loading
- Buffered common clock
- Buffered common active-LOW clear
- 100% reliability assurance testing in compliance with MIL-STD-883

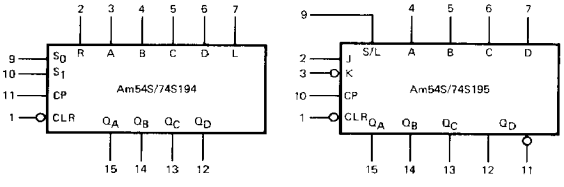
FUNCTIONAL DESCRIPTION

The Am54S/74S194 and Am54S/74S195 are 4-bit registers that exhibit fully synchronous operation in all operating modes. The Am54S/74S195 can either parallel load all four register bits via the parallel inputs (A, B, C, D) or shift each of the four register bits right one place. The shifting or parallel loading is under control of the shift/load input (S/L). When the shift/load input is LOW, data is loaded from the parallel data inputs; when the shift/load input is HIGH, data is loaded from the register bits on the left. The first bit, Q_A, is loaded via the J and $\overline{K}$ inputs in the shift mode.

The Am54S/74S194 operates in four modes under control of the two select inputs, S_0 and S_1. The four modes are parallel load (data comes from the parallel inputs), shift right (data comes from the flip-flop to the left, with the Q_A bit input from R), shift left (data comes from the flip-flop to the right, with the Q_D input from L), and hold or do nothing (each flip-flop receives data from its own output).

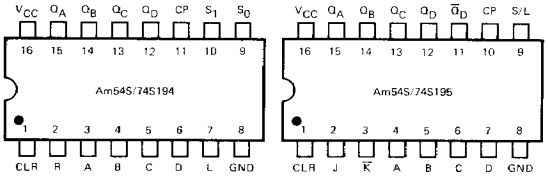
For both devices the outputs change state synchronously following a LOW-to-HIGH transition on the clock input, CP. Both devices have an active-LOW asynchronous clear (CLR) which forces all outputs to the LOW state ($\overline{Q}_D$ HIGH) independent of any other inputs. All control inputs are buffered to present only one Schottky TTL load to the system, and all outputs can drive 10 Schottky loads in the LOW state and 20 in the HIGH state. Because all the flip-flops are D-type they do not catch 0's or 1's, and the only requirements on any inputs is that they meet the short set-up and hold time intervals with respect to the clock LOW-to-HIGH transition.

LOGIC SYMBOLS



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
Top Views



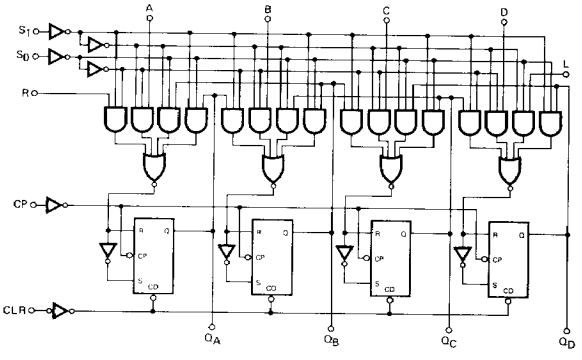
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

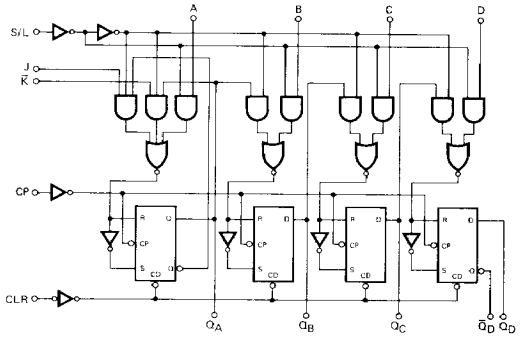
Package Type	Temperature Range	Am54S/74S194 Order Number	Am54S/74S195 Order Number
Molded DIP	0°C to +70°C	SN74S194N	SN74S195N
Hermetic DIP	0°C to +70°C	SN74S194J	SN74S195J
Dice	0°C to +70°C	SN74S194X	SN74S195X
Hermetic DIP	−55°C to +125°C	SN54S194J	SN54S195J
Hermetic Flat Pak	−55°C to +125°C	SN54S194W	SN54S195W
Dice	−55°C to +125°C	SN54S194X	SN54S195X

LOGIC DIAGRAMS

Am54S/74S194



Am54S/74S195



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S194, Am74S195 T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. 5.25 V
Am54S194, Am54S195 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1 mA, V_{IN} = V_{IH} or V_{IL}	Am74	2.7	3.4		Volts
			Am54	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18 mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	S194 (Note 5 & 7)		85	135	mA
			54S195 (Note 6)		70	99	
			74S195 (Note 6)		70	109	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open. Inputs A, B, C, D grounded. Inputs S_0, S_1, Clear, L, R, at 4.5 V. Measured after a momentary ground, then 4.5 V applied to clock.
6. Outputs open. S/L grounded. A, B, C, D, J, $\overline{K}$ at 4.5 V. Measured after applying a momentary ground then 4.5 V to the clear followed by ground then 4.5 V to clock.
7. For T_A = 125°C; I_{CC} MAX. = 110 mA for Am54S194W.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Output	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 280 Ω	4	8	12	ns
t_{PHL}	Clock to Output		4	11	16.5	ns
t_{PHL}	Clear to Output			12.5	18.5	ns
t_{pw}	Clock Pulse Width		7			ns
t_{pw}	Clear Pulse Width		12			ns
t_s	Mode Control Set-up Time		11			ns
t_s	Data Input Set-up Time		5			ns
t_s	Clear Recovery to Clock		9			ns
t_h	Data Hold Time		3			ns
t_R	Shift/Load Release Time Am54S/74S195				6	ns
$f_{MAX.}$	Maximum Clock Frequency		70	105		MHz

DEFINITION OF FUNCTIONAL TERMS

J, $\overline{K}$ The logic inputs used for controlling the Q_A flip-flop of the Am54S/74S195 register when S/L is HIGH.

CLR Clear. The asynchronous master reset input.

CP Clock pulse for the register. Enters data on the LOW-to-HIGH transition.

S/L Shift/Load. The input for selection of parallel or serial shifting for the AM54S/74S195 register. S/L LOW selects parallel entry.

S_0, S_1 The mode select inputs of the Am54S/74S194.

A, B, C, D The four parallel data inputs for the register.

R The serial input to the Q_A flip-flop of the Am54S/74S194 in the right shift mode.

L The serial input to the Q_D flip-flop of the Am54S/74S194 in the left shift mode.

Q_A, Q_B, Q_C, Q_D The four true outputs of the register.

$\overline{Q}_D$ The complement output of the Q_D flip-flop. (Am54S/74S195 only).

LOADING RULES (In Unit Loads)

Am54S/74S195 Input/Output	Am54S/74S194 Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
CLR	CLR	1	1	–	–
J	R	2	1	–	–
$\overline{K}$	A	3	1	–	–
A	B	4	1	–	–
B	C	5	1	–	–
C	D	6	1	–	–
D	L	7	1	–	–
GND	GND	8	–	–	–
Shift/Load	S_0	9	1	–	–
CP	S_1	10	1	–	–
$\overline{Q}_D$	–	11	–	20	10
–	CP		1	–	–
Q_D	Q_D	12	–	20	10
Q_C	Q_C	13	–	20	10
Q_B	Q_B	14	–	20	10
Q_A	Q_A	15	–	20	10
V_{CC}	V_{CC}	16	–	–	–

FUNCTION TABLE
Am54S/74S194

FUNCTION	Clear	Mode S_1	Mode S_0	Clock	Serial Left	Serial Right	Parallel A	Parallel B	Parallel C	Parallel D	OUTPUTS Q_A	Q_B	Q_C	Q_D
Clear	L	X	X	X	X	X	X	X	X	X	L	L	L	L
No Change	H	X	X	L	X	X	X	X	X	X	NC	NC	NC	NC
	H	X	X	H	X	X	X	X	X	X	NC	NC	NC	NC
Parallel Load	H	H	H	↑	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
Shift Right	H	L	H	↑	X	L	X	X	X	X	L	Q_A	Q_B	Q_C
	H	L	H	↑	X	H	X	X	X	X	H	Q_A	Q_B	Q_C
Shift Left	H	H	L	↑	L	X	X	X	X	X	Q_B	Q_C	Q_D	L
	H	H	L	↑	H	X	X	X	X	X	Q_B	Q_C	Q_D	H
Hold	H	L	L	X	X	X	X	X	X	X	NC	NC	NC	NC

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
D_i = May be a HIGH or a LOW and the respective output will assume the same state.

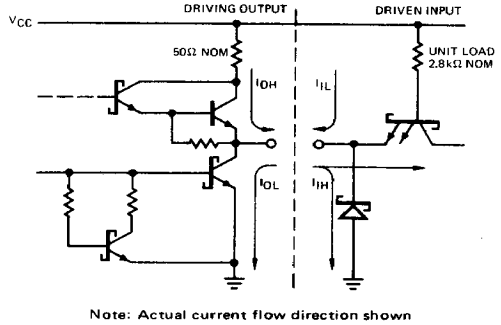
FUNCTION TABLE
Am54S/74S195

Clear	Shift/Load	Clock	Serial J	Serial $\overline{K}$	Parallel A	Parallel B	Parallel C	Parallel D	OUTPUTS Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	X	L	X	X	X	X	X	X	NC	NC	NC	NC	NC
H	X	H	X	X	X	X	X	X	NC	NC	NC	NC	NC
H	L	↑	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3	$\overline{D}_3$
H	H	↑	L	H	X	X	X	X	Q_A	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	L	L	X	X	X	X	L	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	H	H	X	X	X	X	H	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_A$	Q_A	Q_B	Q_C	$\overline{Q}_C$

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
D_i = May be a HIGH or a LOW and the respective output will assume the same state.

Notes: 1. If the J and $\overline{K}$ inputs are tied together, the common line becomes a D-Type input to the first bit in the shift mode.
2. Linear feedback shift counters can be made by connecting the Q_D and $\overline{Q}_D$ outputs to the $\overline{K}$ and J inputs, respectively.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

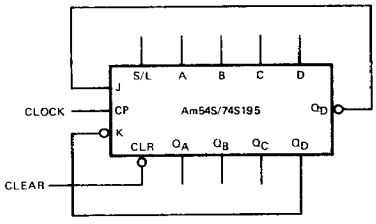


Note: Actual current flow direction shown

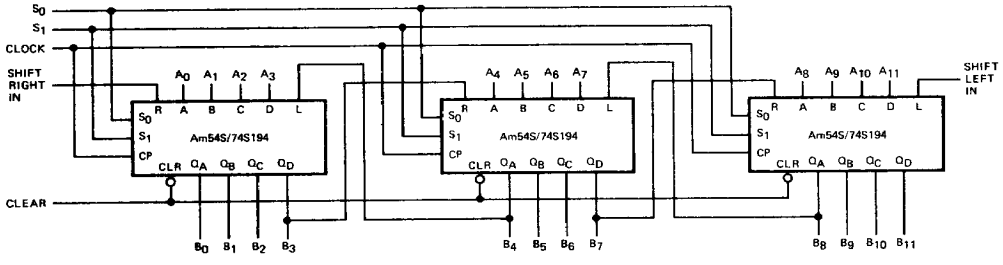
APPLICATIONS

HIGH-SPEED MOD 15 LINEAR FEEDBACK SHIFT REGISTER

Sequence is 0, 1, 2, 5, 10, 4, 9, 3, 6, 13, 11, 7, 14, 12, 8, 0 (15 is non-self correcting; use clear to initialize)

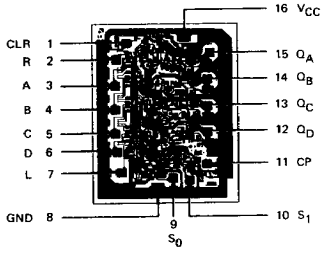


12-BIT SHIFT-LEFT, SHIFT-RIGHT, PARALLEL-LOAD REGISTER



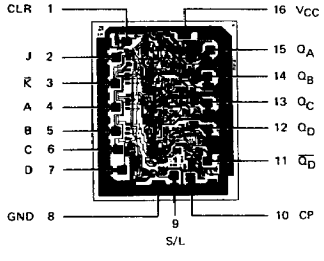
Metallization and Pad Layouts

Am54S/74S194



DIE SIZE 0.072" X 0.093"

Am54S/74S195



DIE SIZE 0.072" X 0.093"