

Signetics

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Status	Product Specification
FAST Products	

FAST 74F604

Latch

Dual Octal Latch (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F604	7.5ns	75mA

FEATURES

- High Impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Stores 16-bit-wide Data Inputs, multiplexed 8-bit outputs
- 3-state outputs
- Power supply current 75mA typical

DESCRIPTION

The 74F604 multiplexed latch is ideal for storing data from two input buses, A or B, and providing data from either the A or B latches to the output bus. Organized as 8-bit A and B latches, the latch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT A/B) input determines whether the A or B latch contents are multiplexed to the eight 3-state outputs. Data entered from the B inputs are selected when SELECT A/B is Low; data from the A inputs are selected when SELECT A/B is High. Data enters

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
28-Pin Plastic DIP	N74F604N
28-Pin Plastic SOL	N74F604D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

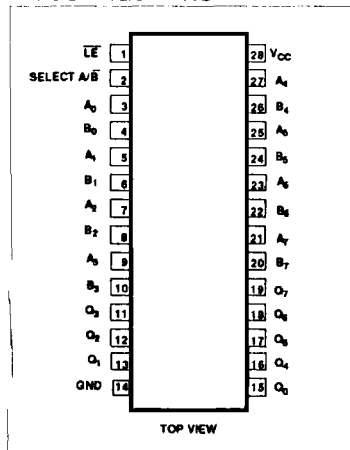
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A ₀ -A ₇ , B ₀ -B ₇	Data inputs	1.0/0.033	20µA/20µA
SELECT A/B	Select input	1.0/0.033	20µA/20µA
LE	Latch Enable Input (active Low)	1.0/0.033	20µA/20µA
Q ₀ -Q ₇	Data outputs	150/40	3mA/24mA

NOTE:

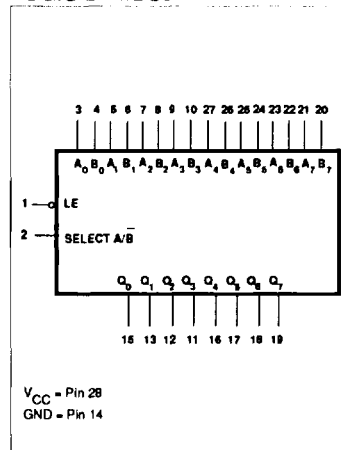
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

the latches when the Latch Enable (\overline{LE}) input is Low and is latched on the \overline{LE} rising edge. The outputs are enabled when \overline{LE} is High and disabled when \overline{LE} is Low.

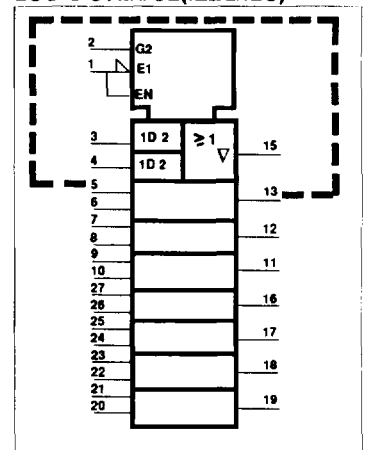
PIN CONFIGURATION



LOGIC SYMBOL



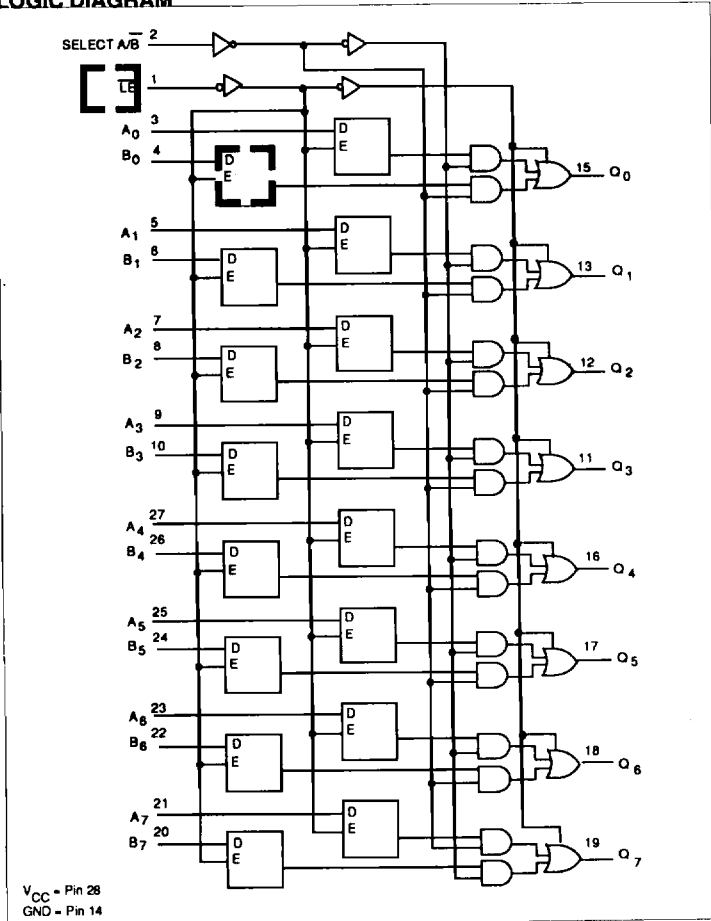
LOGIC SYMBOL (IEEE/IEC)



Latch

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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
A ₀ -A ₇	B ₀ -B ₇	SELECT A/B	LE	Q ₀ -Q ₇
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z
X	X	L	H	B latched data
X	X	H	H	A latched data

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance "off" state
- ↑ = Low-to-High transition

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _A = +25°C V _{CC} = 5V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = 5V ±10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay SELECT A/B to Q _n (B latch)	Waveform 1	5.0	7.0	9.0	4.5	10.0	ns
t _{PLH} t _{PHL}	Propagation delay SELECT A/B to Q _n (A latch)	Waveform 2	6.0	8.0	10.0	5.5	11.5	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	5.0	7.5	9.5	4.5	10.5	ns
t _{PHZ} t _{PLZ}	Output Disable time from High or Low level	Waveform 4 Waveform 5	5.0	7.0	9.5	4.5	11.0	ns

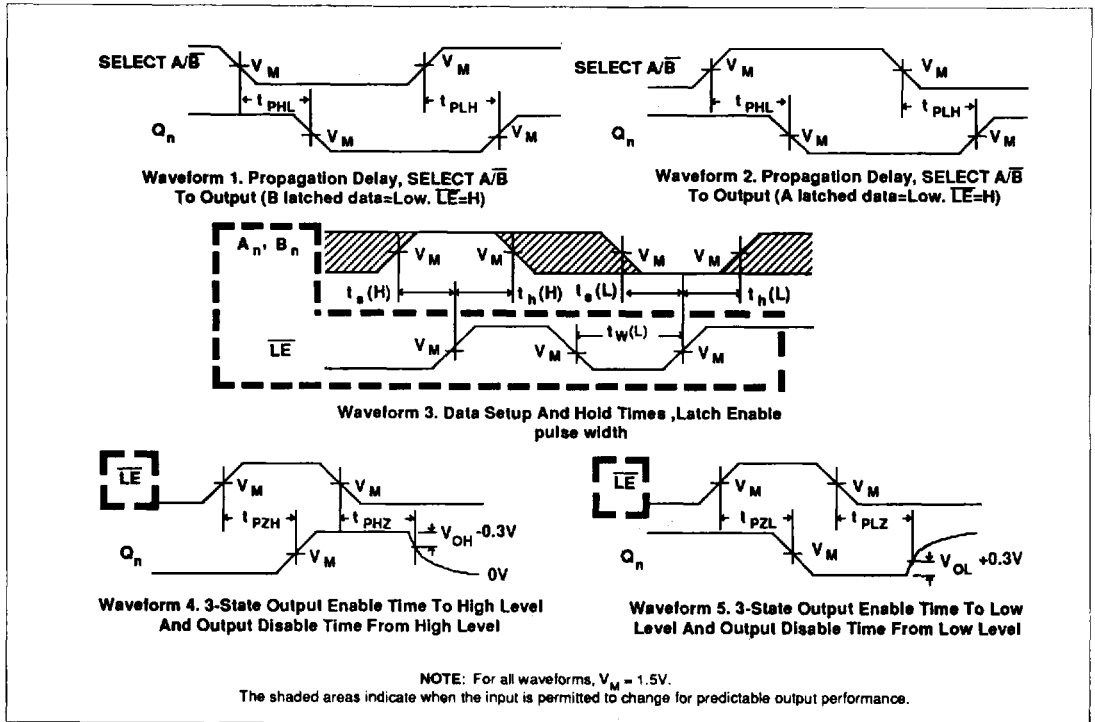
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _A = +25°C V _{CC} = 5V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = 5V ±10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Setup time, High or Low A _n , B _n to \overline{CE}	Waveform 3	1.0			2.0		ns
t _h (H) t _h (L)	Hold time, High or Low A _n , B _n to \overline{CE}	Waveform 3	0			0		ns
t _w (L)	\overline{CE} Pulse width, Low	Waveform 3	5.0			6.0		ns

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AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

