

FAST 74F412/432 Multi-Mode Buffered Latches

74F412 Multi-Mode Buffered Latch, Non-Inverting (3-State)
74F432 Multi-Mode Buffered Latch, Inverting (3-State)

FAST Products

FEATURES

- Status flip-flop for interrupt commands
- Asynchronous or latched receiver modes
- 'F412 Non-Inverting
'F432 Inverting
- 3-state outputs
- 300 mil wide Slim Dip package
- Functional equivalent to Intel 8212 except that 'F432 has inverting outputs

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F412	8.0ns	45mA
74F432	9.0ns	50mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
24-Pin Plastic Slim DIP (300mil)	N74F412N, N74F432N
24-Pin Plastic SOL	N74F412D, N74F432D

DESCRIPTION

The 'F412/'F432 have 8-bit latches with 3-state output buffers. Also included is a status flip-flop for providing device-busy or request-interrupt commands.

Separate mode (M) and Select (\bar{S}_0, S_1) inputs allow data to be stored with the outputs enabled or disabled. The devices can also be operated in a fully transparent mode.

Both 'F412 and 'F432 are functional equivalent to the Intel 8212 except that 'F432 has the inverting outputs.

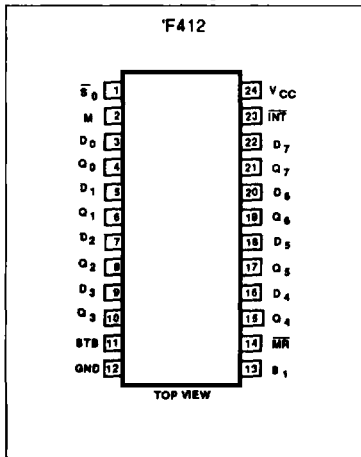
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/1.0	20 μ A/0.6mA
\bar{S}_0, S_1	Select inputs	1.0/1.0	20 μ A/0.6mA
STB	Strobe input	1.0/1.0	20 μ A/0.6mA
M	Mode Control input	1.0/1.0	20 μ A/0.6mA
\bar{MR}	Master Reset input	1.0/1.0	20 μ A/0.6mA
INT	Interrupt Output	50/33	1mA/20mA
$Q_0 - Q_7$	Data Latched Outputs	150/40	3mA/24mA

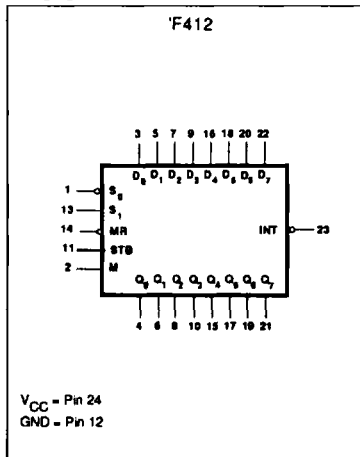
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

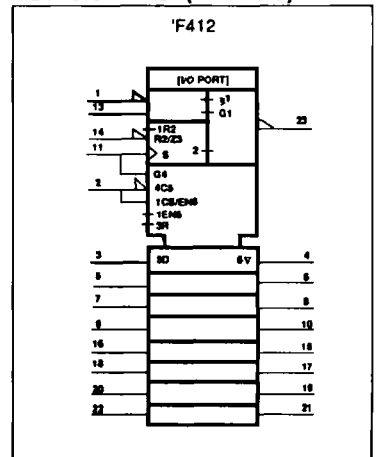
PIN CONFIGURATION



LOGIC SYMBOL



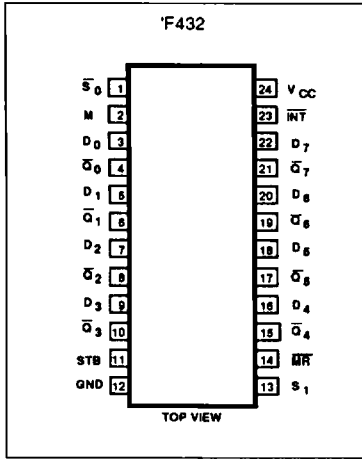
LOGIC SYMBOL (IEEE/IEC)



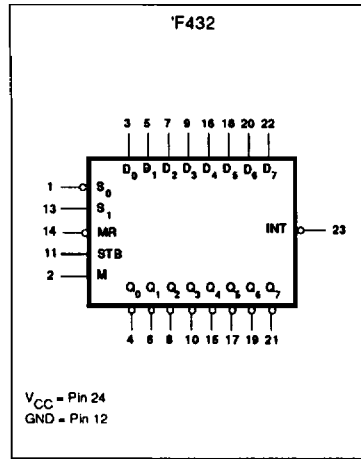
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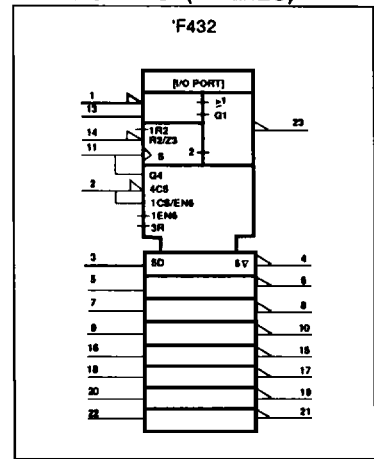
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



This high performance eight-bit parallel expandable buffer latch incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus organized input/output ports. The 3-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands. The eight data latches are fully transparent when the internal gate en-

able, G, input is High and the outputs are enabled. Latch transparency is selected by the mode control (M), select (S_0, S_1), and the strobe (STB) inputs and during transparency each data output (Q_n) follows its respective data input (D_n). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode, M=L, the eight data at the inputs

are enabled when the strobe is High regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken Low, the latches will store the most recently setup data.

In the output mode, M=H, the output buffers are enabled regardless of any other control input. During the output mode the contents of the register is under control of the select (S_0 and S_1) inputs.

FUNCTION TABLE for Data Latches

INPUTS					DATA IN	OUTPUTS		OPERATING MODE
MR	M	S_0	S_1	STB		'F412	'F432	
L	H	H	X	X	X	L	H	Clear
L	L	L	H	L	X	L	H	
X	L	X	L	X	X	Z	Z	De-select
X	L	H	X	X	X	Z	Z	
H	H	H	X	X	X	Q_0	\bar{Q}_0	Hold
H	L	L	H	L	X	Q_0	\bar{Q}_0	
H	H	L	H	X	L	L	H	Data Bus
H	H	L	H	X	H	H	L	
H	L	L	H	H	L	L	H	Data Bus
H	L	L	H	H	H	H	L	

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance "off" state

FUNCTION TABLE for Status Flip-Flop

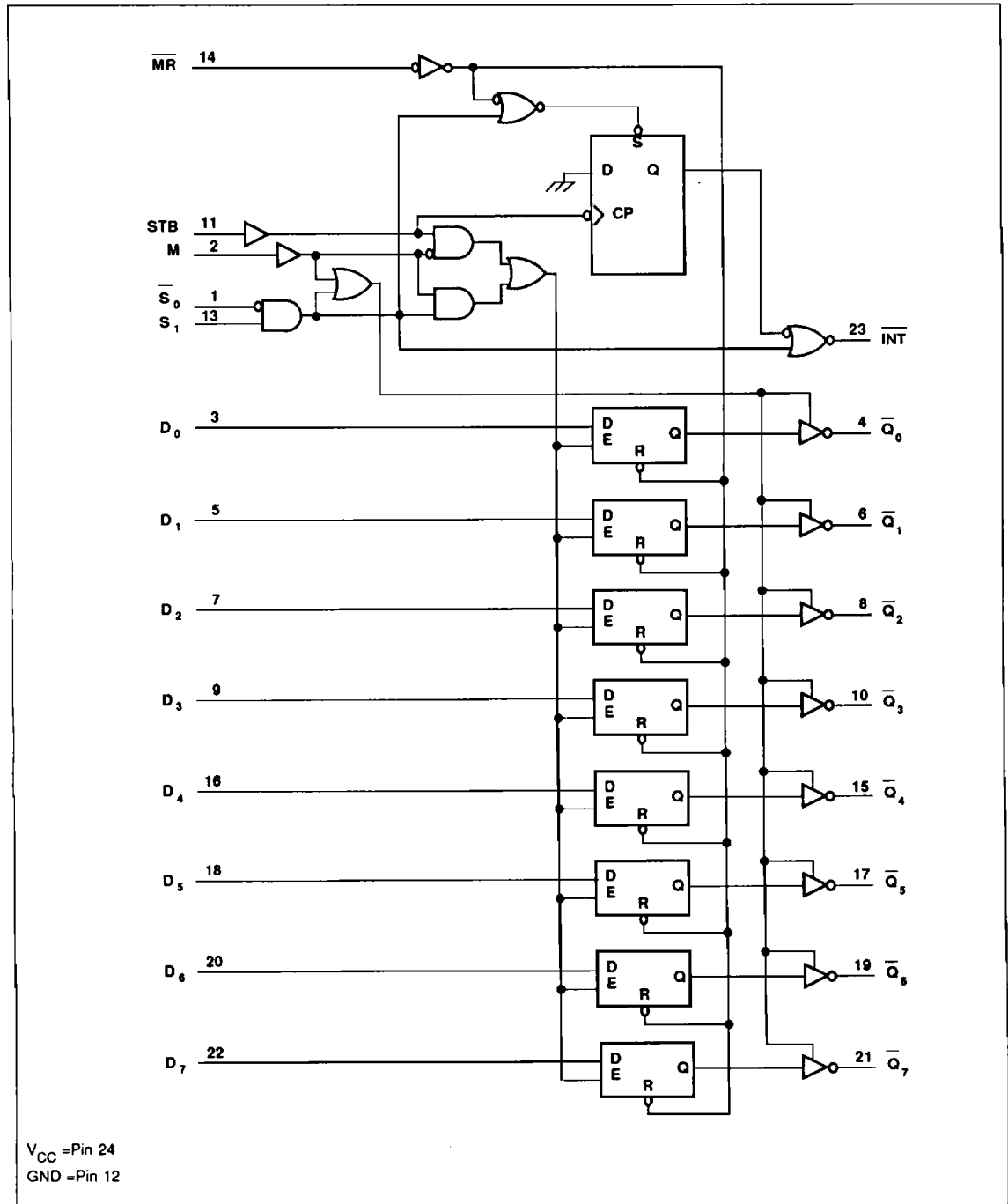
INPUTS				INT
MR	S_0	S_1	STB	
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	L	H	X	L

H = High voltage level
 L = Low voltage level
 ↓ = High-to-Low transition
 X = Don't care

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LOGIC DIAGRAM for 'F432



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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	\overline{INT}	40	mA
		Q_0-Q_7	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current	\overline{INT}		-1	mA
		Q_0-Q_7		-3	mA
I_{OL}	Low-level output current	\overline{INT}		20	mA
		Q_0-Q_7		24	mA
T_A	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT			
					Min	Typ ²	Max				
V_{OH}	High-level output voltage		$V_{CC} = \text{MIN}$ $V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}$	$I_{OH} = -1\text{mA}$	$\pm 10\% V_{CC}$	2.5			V		
					$\pm 5\% V_{CC}$	2.7	3.4		V		
						$I_{OH} = -3\text{mA}$	$\pm 10\% V_{CC}$	2.4			V
							$\pm 5\% V_{CC}$	2.7	3.3		V
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}$ $V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$	$\pm 10\% V_{CC}$		0.30	0.50	V		
					$\pm 5\% V_{CC}$		0.35	0.50	V		
V_{IK}	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.73	-1.2	V			
I_I	Input current at maximum input voltage		$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$				100	μA			
I_{IH}	High-level input current		$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20	μA			
I_{IL}	Low-level input current		$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$				-0.6	mA			
I_{OZH}	Off-state output current, High-level voltage applied		$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$				50	μA			
I_{OZL}	Off-state output current, Low-level voltage applied		$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$				-50	μA			
I_{OS}	Short-circuit output current ³		$V_{CC} = \text{MAX}$			-60	-150	mA			
I_{CC}	Supply current (total)	'F412	I_{CCH}	$V_{CC} = \text{MAX}$		35	50	mA			
			I_{CCL}		45	60	mA				
			I_{CCZ}		45	60	mA				
		'F432	I_{CCH}		40	55	mA				
			I_{CCL}		50	70	mA				
			I_{CCZ}		50	65	mA				

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS for 74F412

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	3.5 2.0	6.0 3.5	8.5 6.5	3.0 2.0	9.5 7.5	ns	
t_{PLH} t_{PHL}	Propagation delay \bar{S}_0, S_1 or STB to Q_n	Waveform 1, 2	7.5 7.0	13.0 9.0	17.0 14.0	7.0 6.5	18.5 15.0	ns	
t_{PLH} t_{PHL}	Propagation delay \bar{S}_0 or S_1 to INT	Waveform 1, 2	3.0 3.0	6.0 6.5	9.5 10.5	3.0 3.0	10.5 11.5	ns	
t_{PHL}	Propagation delay \overline{MR} to Q_n	Waveform 1	6.0	8.0	12.0	5.5	13.0	ns	
t_{PHL}	Propagation delay STB to INT	Waveform 2	6.5	10.0	13.0	5.5	15.0	ns	
t_{PZH} t_{PZL}	Output Enable time to High or Low level \bar{S}_0 to Q_n	Waveform 5 Waveform 6	7.0 7.0	9.0 10.0	12.5 13.5	6.0 6.0	14.0 15.0	ns	
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level \bar{S}_0 to Q_n	Waveform 5 Waveform 6	4.5 6.5	7.5 12.0	10.5 15.0	4.0 6.0	12.0 16.5	ns	
t_{PZH} t_{PZL}	Output Enable time to High or Low level S_1 to Q_n	Waveform 5 Waveform 6	6.0 6.0	10.0 9.0	13.0 12.0	5.0 5.5	14.0 13.0	ns	
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level S_1 to Q_n	Waveform 5 Waveform 6	4.0 6.5	6.0 10.0	9.5 13.5	3.5 6.0	10.5 15.0	ns	
t_{PZH} t_{PZL}	Output Enable time to High or Low level M to Q_n	Waveform 5 Waveform 6	5.0 5.0	8.5 8.5	11.0 11.0	4.5 4.5	12.0 12.0	ns	
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level M to Q_n	Waveform 5 Waveform 6	4.0 6.0	6.5 9.5	9.0 12.5	3.5 5.5	10.0 14.0	ns	

AC SETUP REQUIREMENTS for 74F412

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			
			Min	Typ	Max	Min	Max		
$t_{s(H)}$ $t_{s(L)}$	Setup time, High or Low D_n to $\bar{S}_0, S_1, \text{STB}$ or M	Waveform 3	0 0			1.0 1.0		ns	
$t_{h(H)}$ $t_{h(L)}$	Hold time, High or Low D_n to $\bar{S}_0, S_1, \text{STB}$ or M	Waveform 3	8.0 8.0			9.0 9.0		ns	
$t_{w(H)}$ $t_{w(L)}$	$\bar{S}_0, S_1, \text{STB}$ or M Pulse width, High or Low	Waveform 3	8.0 8.0			9.0 9.0		ns	
$t_{w(L)}$	\overline{MR} Pulse width, Low	Waveform 4	8.0			9.0		ns	
t_{REC}	Recovery time, \overline{MR} to $\bar{S}_0, S_1, M, \text{STB}$	Waveform 4	0			0		ns	

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AC ELECTRICAL CHARACTERISTICS for 74F432

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	4.5 2.5	7.5 4.5	10.5 7.0	4.0 2.5	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay \bar{S}_0 , S_1 or STB to Q_n	Waveform 1, 2	8.5 6.0	14.0 9.5	17.0 13.0	8.0 5.5	19.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay \bar{S}_0 or S_1 to $\overline{\text{INT}}$	Waveform 1, 2	3.0 3.5	6.0 6.5	9.5 10.5	2.5 3.0	10.5 10.5	ns
t_{PHL}	Propagation delay $\overline{\text{MR}}$ to Q_n	Waveform 1	8.0	12.0	16.0	7.5	17.0	ns
t_{PHL}	Propagation delay STB to $\overline{\text{INT}}$	Waveform 2	7.0	10.0	13.5	6.5	14.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level \bar{S}_0 or S_1 to Q_n	Waveform 5 Waveform 6	6.0 6.0	9.0 11.0	12.5 14.0	5.5 5.5	14.0 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level \bar{S}_0 or S_1 to Q_n	Waveform 5 Waveform 6	4.0 6.0	7.5 11.5	11.5 15.0	3.5 5.5	12.5 16.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level M to Q_n	Waveform 5 Waveform 6	5.0 6.0	7.5 8.0	11.0 11.5	4.5 5.5	12.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level M to Q_n	Waveform 5 Waveform 6	3.5 6.0	6.0 10.0	9.5 13.0	3.0 5.5	10.5 13.5	ns

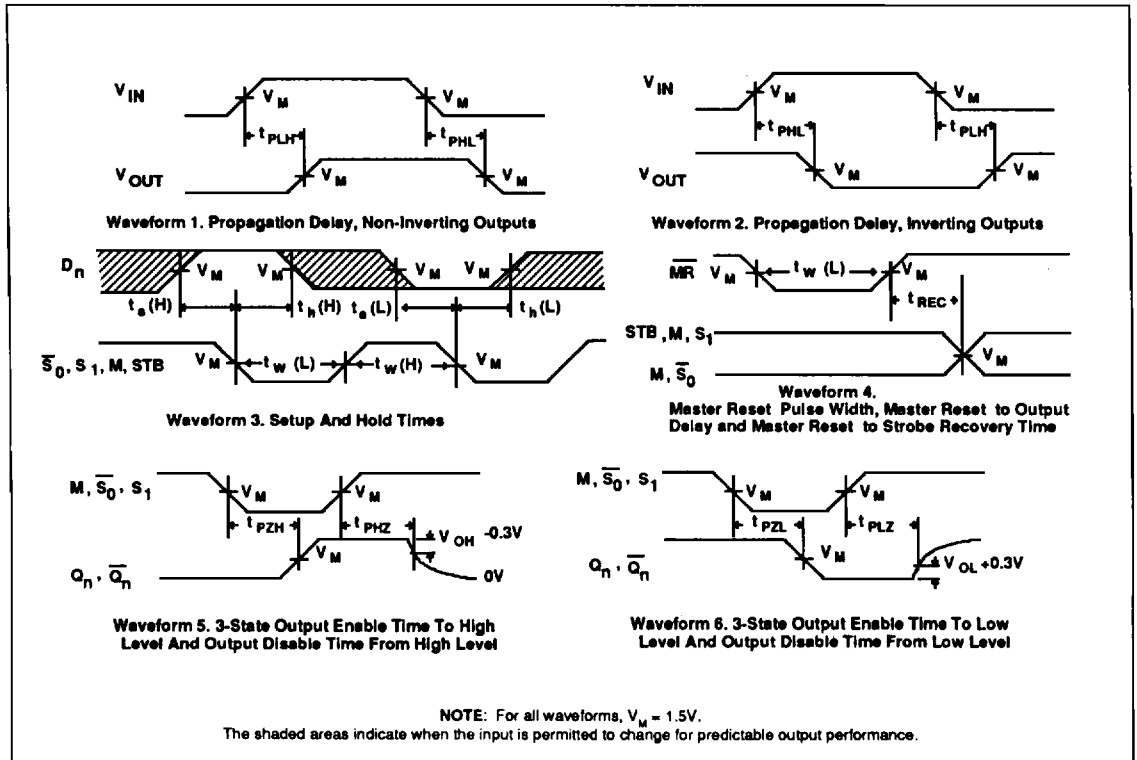
AC SETUP REQUIREMENTS for 74F432

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to \bar{S}_0 , S_1 , STB or M	Waveform 3	0 0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to \bar{S}_0 , S_1 , STB or M	Waveform 3	9.0 8.0			9.5 8.5		ns
$t_w(H)$ $t_w(L)$	\bar{S}_0 , S_1 , STB or M Pulse width, High or Low	Waveform 3	8.0 8.0			9.0 9.0		ns
$t_w(L)$	$\overline{\text{MR}}$ Pulse width, Low	Waveform 4	8.0			9.0		ns
t_{REC}	Recovery time, $\overline{\text{MR}}$ to \bar{S}_0 , S_1 , M, STB	Waveform 4	0			0		ns

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AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

