# Octal D flip–flop | 74F273/273A

## FEATURES

- High impedance inputs for reduced loading (20μA in Low and High states)
- Ideal buffer for MOS microprocessor or memory
- Eight edge–triggered D–type flip–flops
- Buffered common clock
- Buffered asynchronous Master Reset
- 74F273A has improved DC, AC, and $f_{MAX}$
- 74F273A has improved noise margin
- See 74F377 for clock enable version
- See 74F373 for transparent latch version
- See 74F374 for 3–State version

## DESCRIPTION

The 74F273 has eight edge–triggered D–type flip–flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip–flops simultaneously.

The register is fully edge–triggered. The state of each D input, one setup time before the Low–to–High clock transition, is transferred to the corresponding flip–flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common to all elements.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F273 | 125MHz | 66mA |
| 74F273A | 170MHz | 25mA |

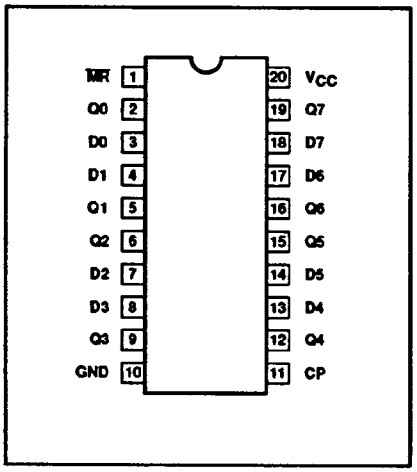
## ORDERING INFORMATION

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V±10%; $T_{amb}$ = 0°C to +70°C |
|---|---|
| 20–pin plastic DIP | 74F273N, 74F273AN |
| 20–pin plastic SOL | 74F273D, 74F273AD |

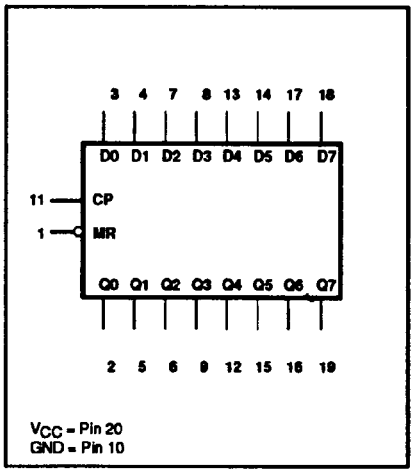
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| D0 – D7 | Data inputs | 1.0/0.033 | 20μA/20μA |
| $\overline{MR}$ | Master Reset input (active–Low) | 1.0/0.033 | 20μA/20μA |
| CP | Clock pulse input (active rising edge) | 1.0/0.033 | 20μA/20μA |
| Q0 – Q7 | Data outputs | 50/33 | 1.0mA/20mA |

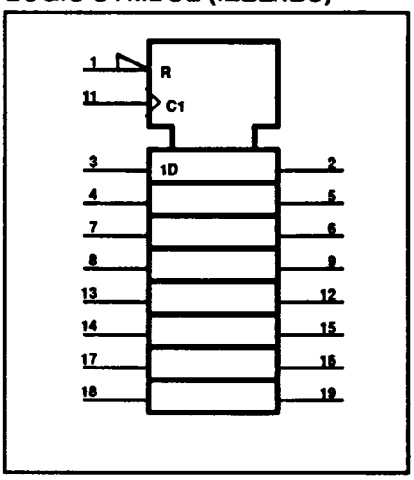
## PIN CONFIGURATION




## LOGIC SYMBOL




## LOGIC SYMBOL (IEEE/IEC)



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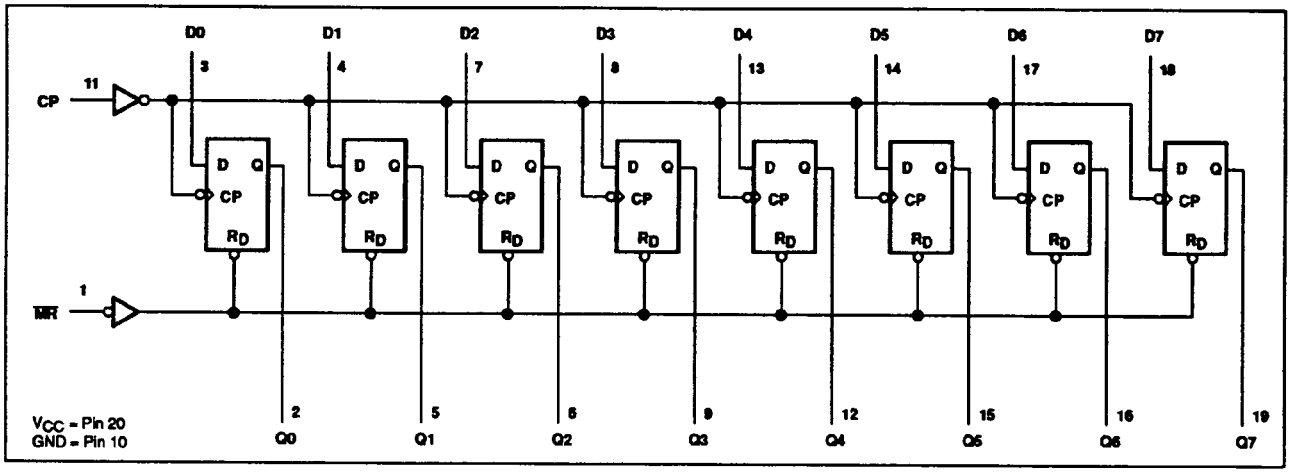
## LOGIC DIAGRAM




## FUNCTION TABLE

| INPUTS | | | OUTPUTS | OPERATING MODE |
|---|---|---|---|---|
| $\overline{MR}$ | CP | Dn | Q0 – Q7 | |
| L | X | X | L | Reset (clear) |
| H | ↑ | h | H | Load "1" |
| H | ↑ | l | L | Load "0" |

H = High voltage level
h = High voltage level one set–up time prior to the Low–to–High clock transition
L = Low voltage level
l = Low voltage level one set–up time prior to the Low–to–High clock transition
X = Don't care
↑ = Low–to–High clock transition

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | –0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | –0.5 to +7.0 | V |
| $I_{IN}$ | Input current | –30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in High output state | –0.5 to $V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in Low output state | 40 | mA |
| $T_{amb}$ | Operating free air temperature range | 0 to +70 | °C |
| $T_{stg}$ | Storage temperature range | –65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High–level input voltage | 2.0 | | | V |
| $V_{IL}$ | Low–level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High–level output current | | | –1 | mA |
| $I_{OL}$ | Low–level output current | | | 20 | mA |
| $T_{amb}$ | Operating free air temperature range | 0 | | +70 | °C |

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | | | TEST CONDITIONS[1] | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP[2] | MAX | |
| $V_{OH}$ | High-level output voltage | | MR & CP inputs | $V_{CC}$ = MIN, $V_{IL}$ = 0.0V[3], $V_{IH}$ = 4.5V[3], $I_{OH}$ = MAX | ±10%$V_{CC}$ | 2.5 | | | V |
| | | | | | ±5%$V_{CC}$ | 2.7 | 3.4 | | V |
| | | | other inputs | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN, $I_{OH}$ = MAX | ±10%$V_{CC}$ | 2.5 | | | V |
| | | | | | ±5%$V_{CC}$ | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN, $I_{OH}$ = MAX | ±10%$V_{CC}$ | | 0.30 | 0.50 | V |
| | | | | | ±5%$V_{CC}$ | | 0.30 | 0.50 | V |
| $V_{IK}$ | Input clamp voltage | | | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ | | | –0.73 | -1.2 | V |
| $I_I$ | Input current at maximum input voltage | | | $V_{CC}$ = 0.0V, $V_I$ = 7.0V | | | | 100 | µA |
| $I_{IH}$ | High–level input current | | | $V_{CC}$ = MAX, $V_I$ = 2.7V | | | | 20 | µA |
| $I_{IL}$ | Low–level input current | | | $V_{CC}$ = MAX, $V_I$ = 0.5V | | | | –20 | µA |
| $I_{OS}$ | Short–circuit output current[4] | | | $V_{CC}$ = MAX | | -60 | | -150 | mA |
| $I_{CC}$ | Supply current (total) | 74F273 | $I_{CCH}$ | $V_{CC}$ = MAX | | | 65 | 85 | mA |
| | | | $I_{CCL}$ | | | | 68 | 88 | mA |
| | | 74F273A | $I_{CCH}$ | $V_{CC}$ = MAX | | | 24 | 38 | mA |
| | | | $I_{CCL}$ | | | | 27 | 43 | mA |

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC}$ = 5V, $T_{amb}$ = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing $I_{OS}$, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

## AC CHARACTERISTICS FOR 'F273

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50pF, $R_L$ = 500Ω | | | $T_{amb}$ = –40°C to +85°C, $V_{CC}$ = +5.0V ±10%, $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum clock frequency | 1 | 115 | 125 | | 100 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to Qn | 1 | 4.0<br>4.0 | 7.5<br>7.5 | 9.5<br>9.5 | 4.0<br>4.0 | 10.5<br>10.5 | ns |
| $t_{PHL}$ | Propagation delay<br>$\overline{MR}$ to Qn | 2 | 4.0 | 5.5 | 8.5 | 3.5 | 9.0 | ns |

## AC SETUP REQUIREMENTS FOR 'F273

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50pF, $R_L$ = 500Ω | | | $T_{amb}$ = –40°C to +85°C, $V_{CC}$ = +5.0V ±10%, $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | Min | Typ | Max | Min | Max | |
| $t_s(H)$<br>$t_s(L)$ | Setup time, High or Low<br>Dn to CP | 3 | 3.0<br>3.0 | | | 3.0<br>3.0 | | |
| $t_h(H)$<br>$t_h(L)$ | Hold time, High or Low<br>Dn to CP | 3 | 0.0<br>0.0 | | | 0.0<br>0.0 | | ns |
| $t_w(H)$<br>$t_w(L)$ | Clock pulse width<br>High or Low | 1 | 4.0<br>5.0 | | | 4.0<br>5.5 | | ns |
| $t_w(L)$ | Master Reset pulse width, Low | 2 | 3.5 | | | 4.5 | | ns |
| $t_{REC}$ | Recovery time<br>$\overline{MR}$ to CP | 2 | 8.5 | | | 9.0 | | ns |

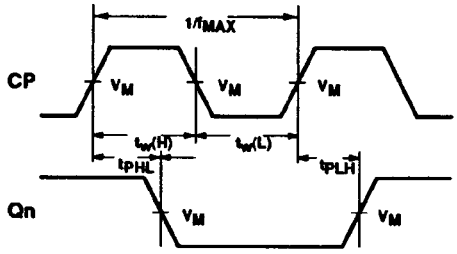
## AC CHARACTERISTICS FOR 'F273A

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50pF, $R_L$ = 500Ω | | | $T_{amb}$ = –40°C to +85°C, $V_{CC}$ = +5.0V ±10%, $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum clock frequency | 1 | 150 | 170 | | 125 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to Qn | 1 | 3.5<br>5.0 | 5.0<br>7.0 | 8.0<br>9.5 | 3.0<br>4.5 | 9.0<br>10.0 | ns |
| $t_{PHL}$ | Propagation delay<br>$\overline{MR}$ to Qn | 2 | 5.0 | 7.0 | 9.0 | 5.0 | 9.5 | ns |

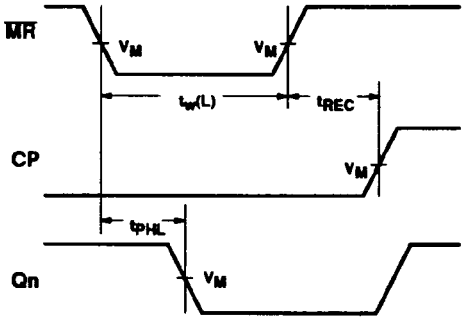
## AC SETUP REQUIREMENTS FOR 'F273A

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50pF, $R_L$ = 500Ω | | | $T_{amb}$ = –40°C to +85°C, $V_{CC}$ = +5.0V ±10%, $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | Min | Typ | Max | Min | Max | |
| $t_s(H)$<br>$t_s(L)$ | Setup time, High or Low<br>Dn to CP | 3 | 3.0<br>2.0 | | | 2.5<br>2.5 | | |
| $t_h(H)$<br>$t_h(L)$ | Hold time, High or Low<br>Dn to CP | 3 | 0.5<br>0.0 | | | 2.5<br>1.0 | | ns |
| $t_w(H)$<br>$t_w(L)$ | Clock pulse width<br>High or Low | 1 | 4.5<br>3.5 | | | 5.0<br>4.0 | | ns |
| $t_w(L)$ | Master Reset pulse width, Low | 2 | 3.0 | | | 3.5 | | ns |
| $t_{REC}$ | Recovery time<br>$\overline{MR}$ to CP | 2 | 4.0 | | | 5.0 | | ns |

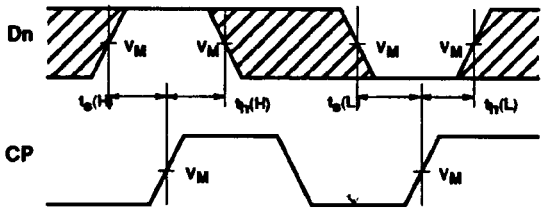
## AC WAVEFORMS




**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**



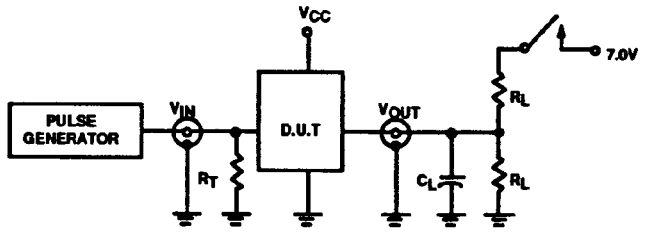

**Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**



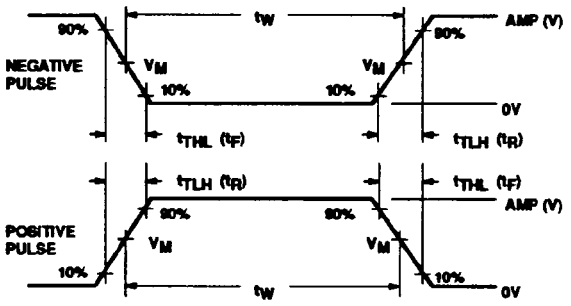

**Waveform 3. Data Setup and Hold Times**

**NOTE:** For all waveforms, $V_M$ = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUIT AND WAVEFORMS




**Test Circuit for Totem Outputs**




$V_M$ = 1.5V
**Input Pulse Definition**

### DEFINITIONS

$R_L$ = Load resistor; see AC CHARACTERISTICS for value.

$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|---|---|---|---|---|---|
| | Amplitude | Rep. Rate | $t_W$ | $t_R$ | $t_F$ |
| 74F | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |