

HD74LS93

4-bit Binary Counter

REJ03D0423-0200 Rev.2.00 Feb.18.2005

The HD74LS93 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-state binary counter for divide-by-eight. To use this maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are described in the appropriate function table.

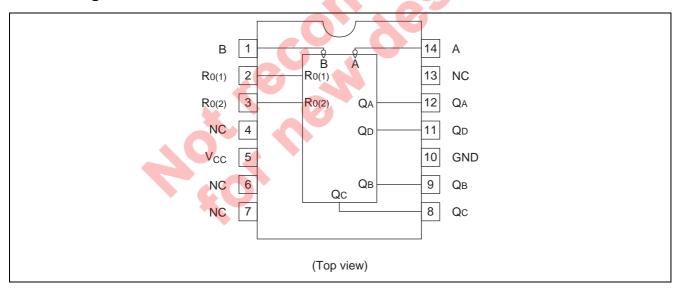
Features

• Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|--------------|--------------------|---------------------------------|-------------------------|--------------------------------|
| HD74LS93P | DILP-14 pin | PRDP0014AB-B (DP-14AV) | Р | _ |
| HD74LS93FPEL | SOP-14 pin (JEITA) | PRSP0014DF-B (FP-14DAV) | FP | EL (2,000 pcs/reel) |

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Function Table

• Reset / Count Function Table

| Reset | inputs | Outputs | | | | | |
|-------------------|-------------------|------------------|----------------|---|---|--|--|
| R ₀₍₁₎ | R ₀₍₂₎ | \mathbf{Q}_{D} | Q _A | | | | |
| Н | Н | L | L | L | L | | |
| L | Х | Count | | | | | |
| Х | L | Count | | | | | |

Note: H; high level, L; low level, X; irrelevant

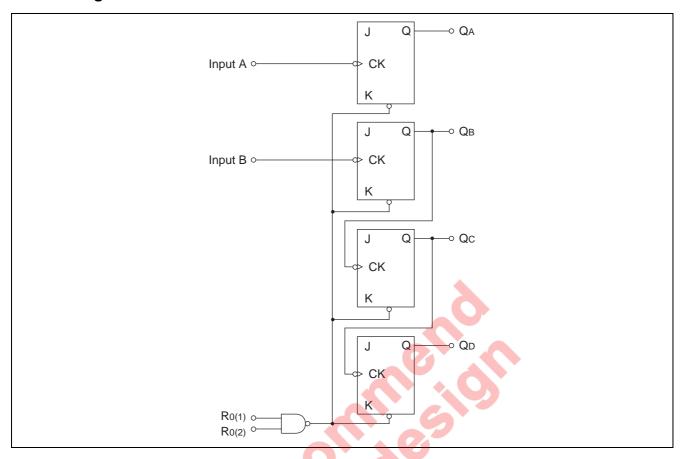
• BCD Count Sequence (Notes 1)

| Count | | Out | puts | |
|-------|------------------|----------------|----------------|-------|
| | \mathbf{Q}_{D} | Q _C | Q _B | Q_A |
| 0 | L | L | L | L |
| 1 | L | L | L | Н |
| 2 | L | L | Н | L |
| 3 | L | L | H | Н |
| 4 | L | Н | L | Н |
| 5 | L | Н | L | Н |
| 6 | L | Н | H | L |
| 7 | L | Н | Н | Н |
| 8 | Н | L | L | L |
| 9 | Н | Ц | L | Н |
| 10 | Н | L | Н | L |
| 11 | Н | L | ✓ H | Н |
| 12 | Н | Н | L | L |
| 13 | Н | Н | L | Н |
| 14 | H | H | Н | L |
| 15 | Н | Н | Н | Н |

Notes: 1. Output QA is connected to input B for BCD count.

2. H; high level, L; low level

Block Diagram



Absolute Maximum Ratings

| Item | 4 | Symbol | Ratings | Unit |
|---------------------|-------------|-----------------|-------------|------|
| Supply voltage | | V_{CC} | 7 | V |
| lanut valta aa | R Inputs | V _{IN} | 7 | V |
| Input voltage | A, B Inputs | V _{IN} | 5.5 | V |
| Power dissipation | | P _T | 400 | mW |
| Storage temperature | | Tstg | -65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

| Item | | Symbol | Min | Тур | Max | Unit |
|---------------------|-----------------------|-----------------|------|------|------|------|
| Supply voltage | | V _{CC} | 4.75 | 5.00 | 5.25 | V |
| Output ourront | | I _{OH} | _ | _ | -400 | μΑ |
| Output current | Output current | | _ | _ | 8 | mA |
| Operating temperatu | Operating temperature | | -20 | 25 | 75 | °C |
| Count fraguency | A input | | 0 | _ | 32 | MHz |
| Count frequency | B input | f_{count} | 0 | _ | 16 | |
| | A input | t _w | 15 | _ | _ | |
| Pulse width | B input | | 30 | _ | _ | ns |
| | Reset input | | 15 | _ | _ | |
| Setup time | | t _{su} | 25 | _ | _ | ns |

Electrical Characteristics

 $(Ta = -20 \text{ to } +75 \text{ }^{\circ}\text{C})$

| | Item | Symbol | min. | typ.* | max. | Unit | Condition | | |
|----------------------|-------------|---------------------|------|-------|------|------|---|--|--|
| Input val | tago | V _{IH} | 2.0 | _ | _ | V | | | |
| Input voltage | | V_{IL} | _ | _ | 0.8 | V | | | |
| | | V _{OH} | 2.7 | _ | _ | V | $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V},$ $I_{OH} = -400 \mu\text{A}$ | | |
| Output v | oitage | \/ | _ | _ | 0.4 | V | $I_{OL} = 4 \text{ mA**}$ | $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$ | |
| | | V _{OL} | _ | _ | 0.5 | V | I _{OL} = 8 mA** | $V_{IL} = 0.8 V$ | |
| | Any reset | | _ | _ | -0.4 | | • | | |
| | A input | I₁∟ | _ | _ | -2.4 | mA | $V_{CC} = 5.25 \text{ V}, V_{I} = 0.4 \text{ V}$ | $V_1 = 0.4 \text{ V}$ | |
| | B input | | _ | _ | -1.6 | | | | |
| la a t | Any reset | | _ | _ | 20 | | | | |
| Input | A input | I _{IH} | _ | _ | 40 | μΑ | $V_{CC} = 5.25 \text{ V}, V_{I} = 2.7 \text{ V}$ | | |
| Current | B input | | _ | _ | 40 | | | | |
| | Any reset | | _ | _ | 0.1 | | V _I = 7 V | | |
| | A input | I ₁ | _ | _ | 0.2 | mA | V _I = 5.5 V | $V_{CC} = 5.25 \text{ V}$ | |
| | B input | | _ | _ | 0.2 | | V _I = 5.5 V | | |
| Short-cir current | cuit output | Ios | -20 | _ | -100 | mA | mA V _{CC} = 5.25 V | | |
| Supply o | urrent | I _{CC} *** | _ | 9 | 15 | mA | V _{CC} = 5.25 V | | |
| Input cla | mp voltage | V _{IK} | _ | _ | -1.5 | V | $V_{CC} = 4.75 \text{ V}, I_1$ | _N = −18 mA | |

Switching Characteristics

 $(V_{CC} = 5 \text{ V}, \text{ Ta} = 25^{\circ}\text{C})$

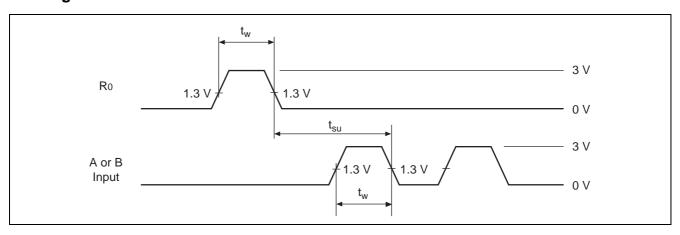
| Item | Symbol | Inputs | Outputs | min. | typ. | max. | Unit | Condition |
|-------------------------|------------------|----------|----------------|------|------|------|---------|--|
| Maximum count frequency | f _{max} | A | Q_A | 32 | 42 | _ | MHz | |
| waximum count frequency | | В | Q _B | 16 | | | IVII IZ | |
| | t _{PLH} | А | Q_A | | 10 | 16 | | |
| | t _{PHL} | | QΑ | _ | 12 | 18 | | $C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega$ |
| | t _{PLH} | А | Q_D | 1 | 46 | 70 | ns | |
| | t _{PHL} | | | 1 | 46 | 70 | | |
| | t _{PLH} | В | Q _B | 1 | 10 | 16 | | |
| Propagation delay time | t _{PHL} | | | 1 | 14 | 21 | | |
| | t _{PLH} | В | Q _C | 1 | 21 | 32 | | |
| | t _{PHL} | ם | Q U | | 23 | 35 | | |
| | t _{PLH} | В | Q _D | 1 | 34 | 51 | | |
| | t _{PHL} | ט | | | 34 | 51 | | |
| | t _{PHL} | Set-to-0 | Q_A to Q_D | | 26 | 40 | | |

Note: Refer to Test Circuit and Waveform of the Common Item "TTL Common Matter (Document No.: REJ27D0005-0100)".

Notes: ${}^*V_{CC} = 5 \text{ V}$, Ta = 25°C ** Q_A output is tested at specified I_{OL} plus the limit value of IIL for the B input. This permits driving the B input while maintaining full fan-out capability.

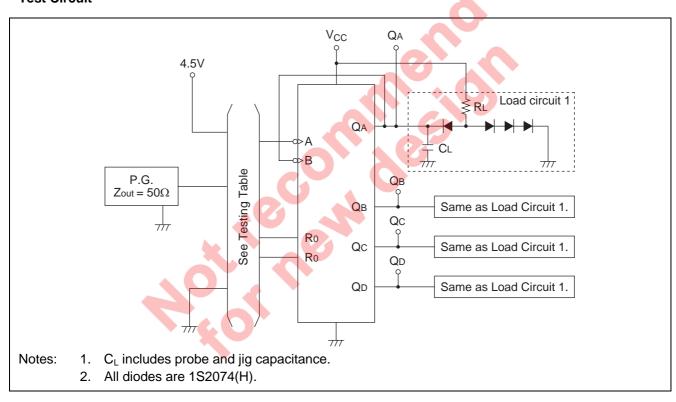
^{***} I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

Timing Definition



Testing Method

Test Circuit



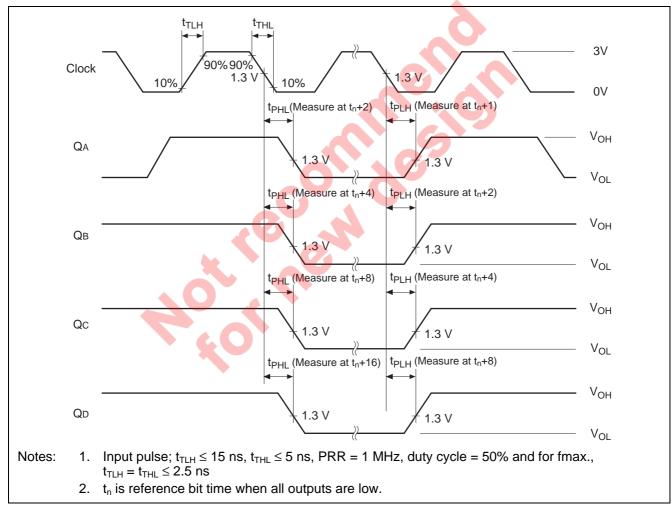
Testing Table

| Item | From input | | Inputs | | Outputs | | | |
|------------------|--------------------------|-------|-------------------|----------------|----------------|----------------|-----|----------------|
| пеш | to output | Α | В | R ₀ | Q _A | Q _B | Qc | Q _D |
| f | $A \to Q$ | IN | to Q _A | GND | Out | Out | Out | Out |
| f _{max} | $B\toQ$ | 4.5 V | IN | GND | _ | Out | Out | Out |
| | $A\toQ_A$ | IN | to Q _A | GND | Out | _ | _ | _ |
| | $A\toQ_D$ | IN | to Q _A | GND | _ | _ | _ | Out |
| t_{PLH} | $B\toQ_B$ | 4.5 V | IN | GND | _ | Out | _ | _ |
| t_{PHL} | $B\toQ_C$ | 4.5 V | IN | GND | _ | _ | Out | _ |
| | $B\toQ_D$ | 4.5 V | IN | GND | _ | _ | _ | Out |
| | $R_0^{**} \rightarrow Q$ | IN* | to Q _A | IN | Out | Out | Out | Out |

^{*} For initialized.

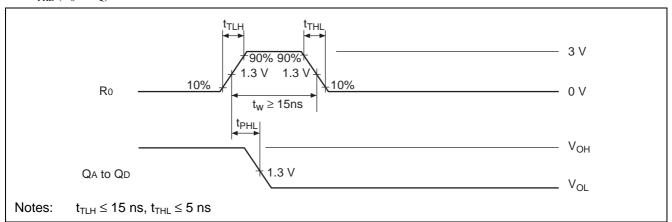
Waveform

1. f_{max} , t_{PLH} , t_{PHL} (Clock \rightarrow Q)



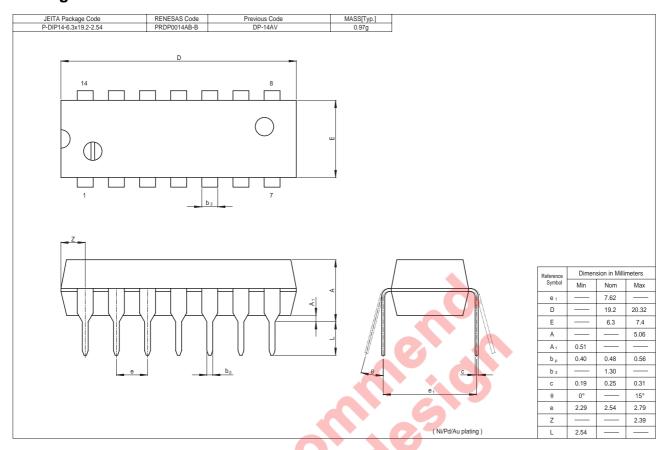
^{**} Measured with each input and unused inputs at 4.5 V.

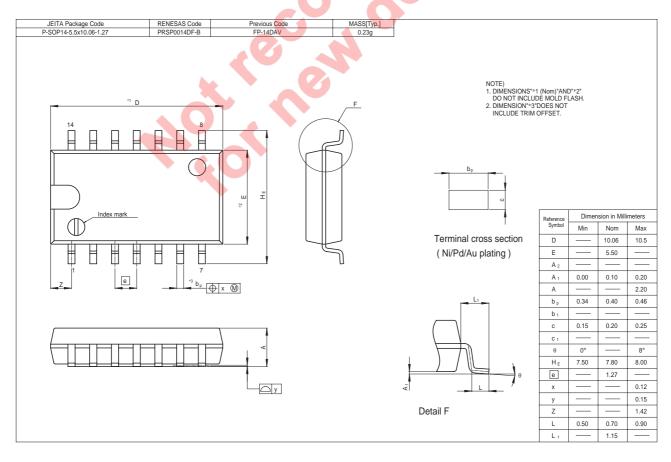
2. $t_{PHL} (R_0 \rightarrow Q)$





Package Dimensions





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