

HD74HC174

Hex D-type Flip-Flops (with Clear)

REJ03D0584-0300

Rev.3.00

Jan 31, 2006

Description

This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the clock input. The clear input when low, sets all outputs to a low state.




Features

- High Speed Operation: t_{pd} (Clock to Q) = 15 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC174P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC174FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HC174TELL	TSSOP-16 pin	PTSP0016JB-A (TTP-16DAV)	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

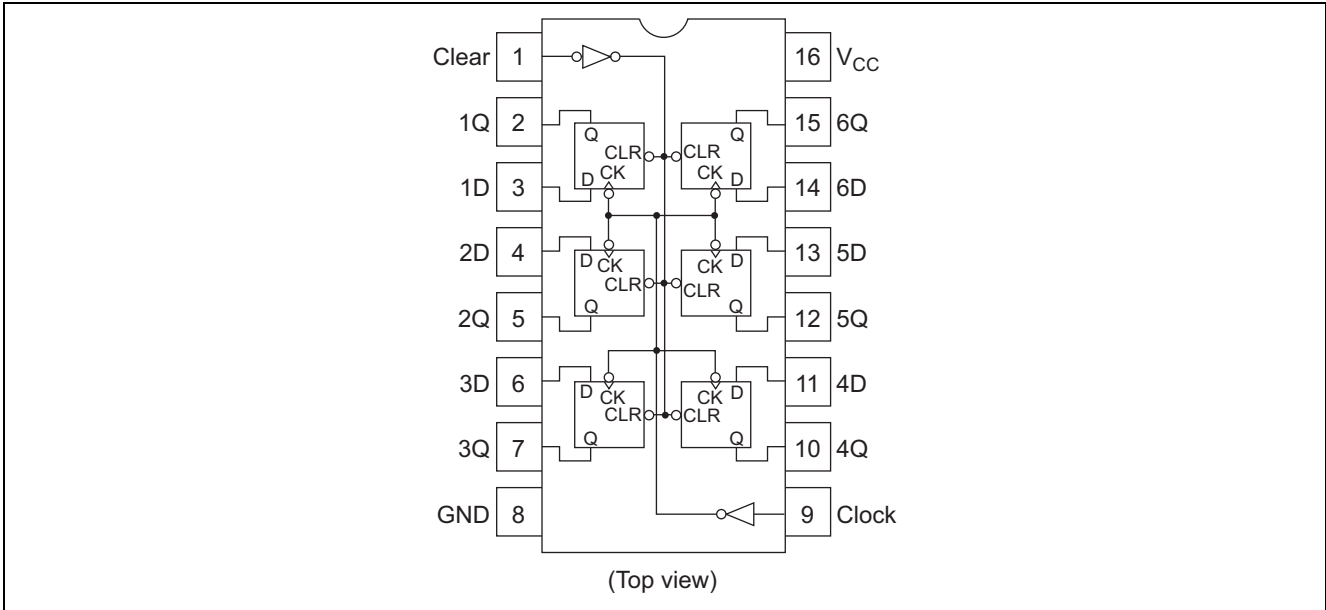
Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	no change
H		X	no change

H: High level

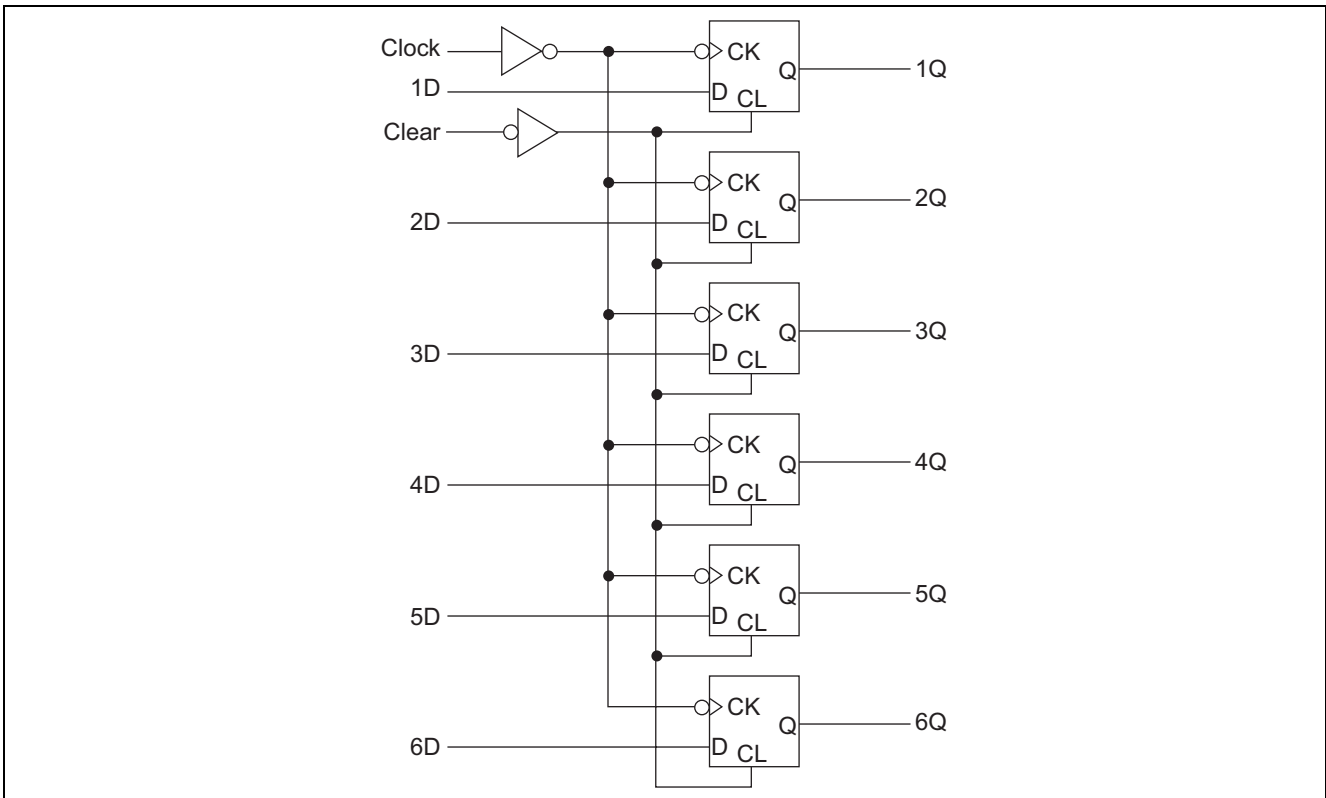
L: Low level

X: Irrelevant

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{in}, V_{out}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 25	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0$ V
		0 to 500		$V_{CC} = 4.5$ V
		0 to 400		$V_{CC} = 6.0$ V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

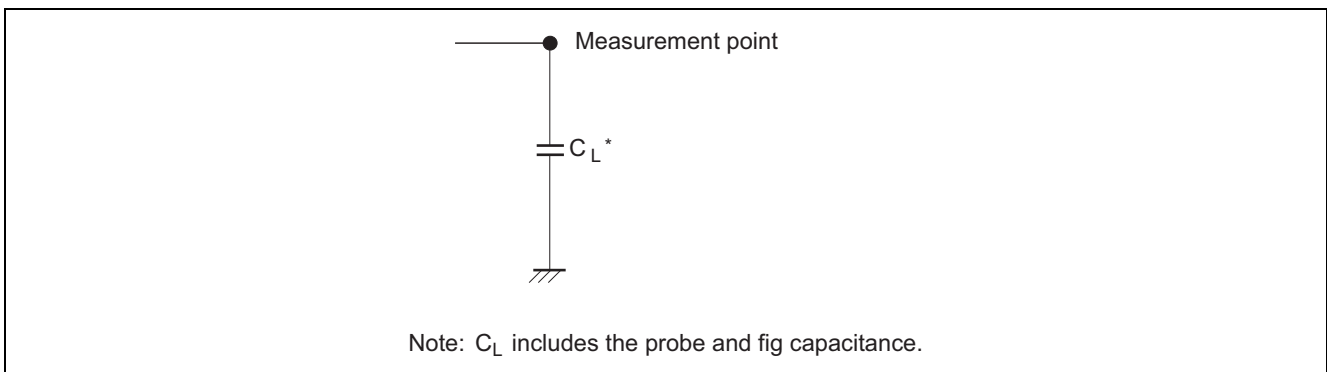
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -4 \text{ mA}$
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -5.2 \text{ mA}$
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
		6.0	5.68	—	—	5.63	—			
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OL} = 4 \text{ mA}$
6.0	—	—	0.26	—	0.33	$I_{OL} = 5.2 \text{ mA}$				
Input current	I_{in}	6.0	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC}$ or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	μA	$V_{in} = V_{CC}$ or GND, $I_{out} = 0 \mu\text{A}$	

Switching Characteristics

($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

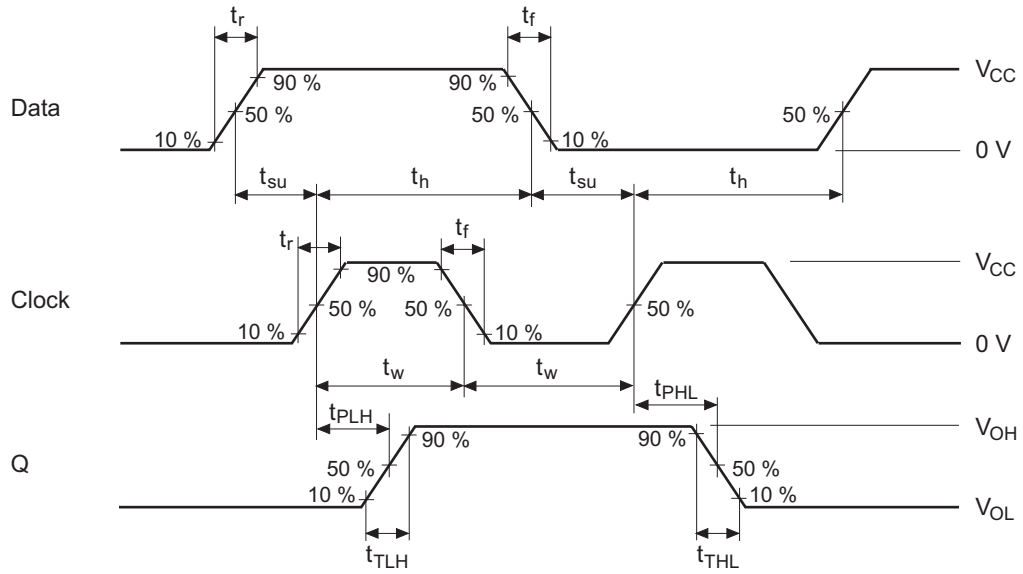
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	6	—	5	MHz	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	t_{PLH}, t_{PHL}	2.0	—	—	160	—	200	ns	Clock to Q
		4.5	—	15	32	—	40		
		6.0	—	—	27	—	34		
		2.0	—	—	160	—	200	ns	Clear to Q
		4.5	—	17	32	—	40		
		6.0	—	—	27	—	34		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Data to Clock
		4.5	20	3	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	Clock to Data
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t_{rem}	2.0	25	—	—	31	—	ns	Clear to Clock
		4.5	5	-1	—	6	—		
		6.0	4	—	—	5	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Clock, Clear
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH}, t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

Test Circuit

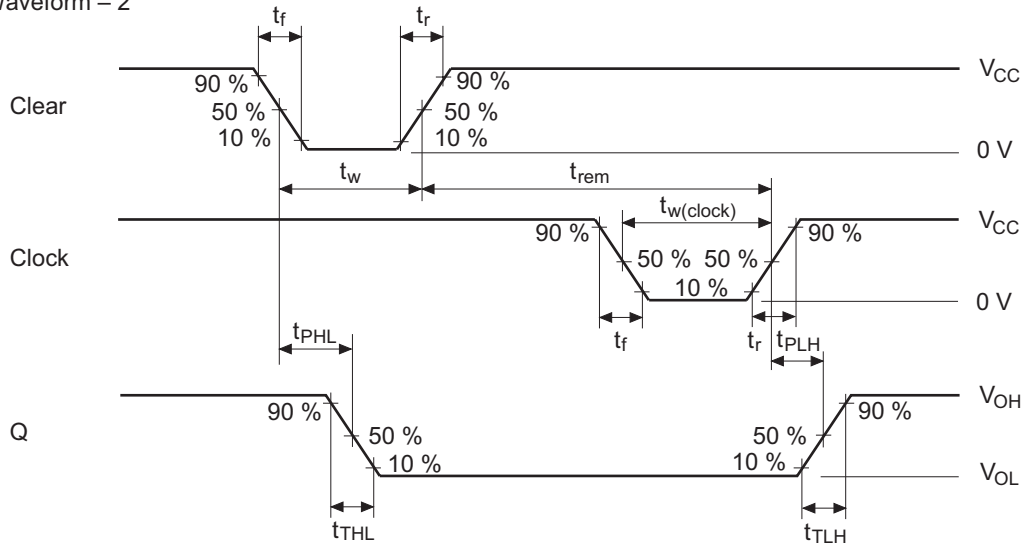


Waveforms

• Waveform – 1

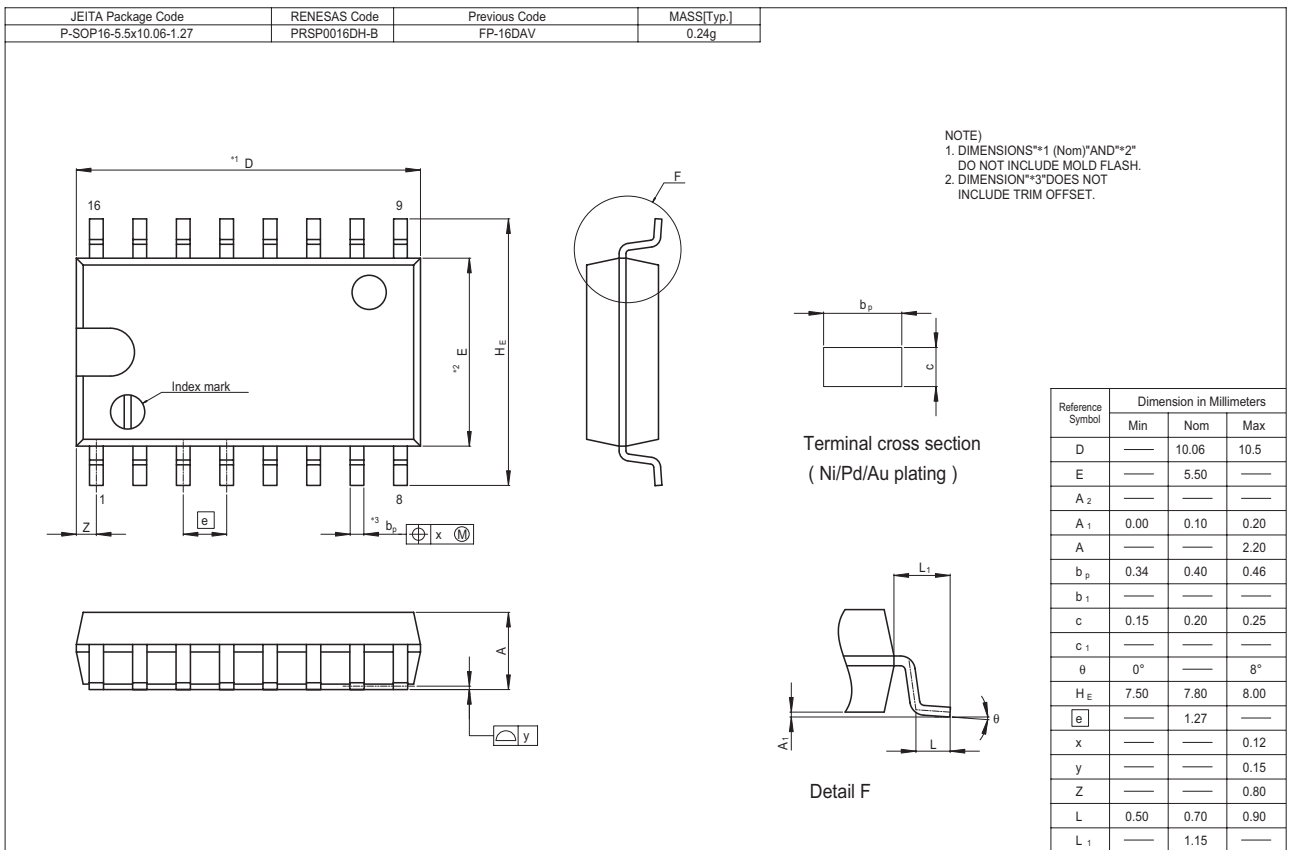
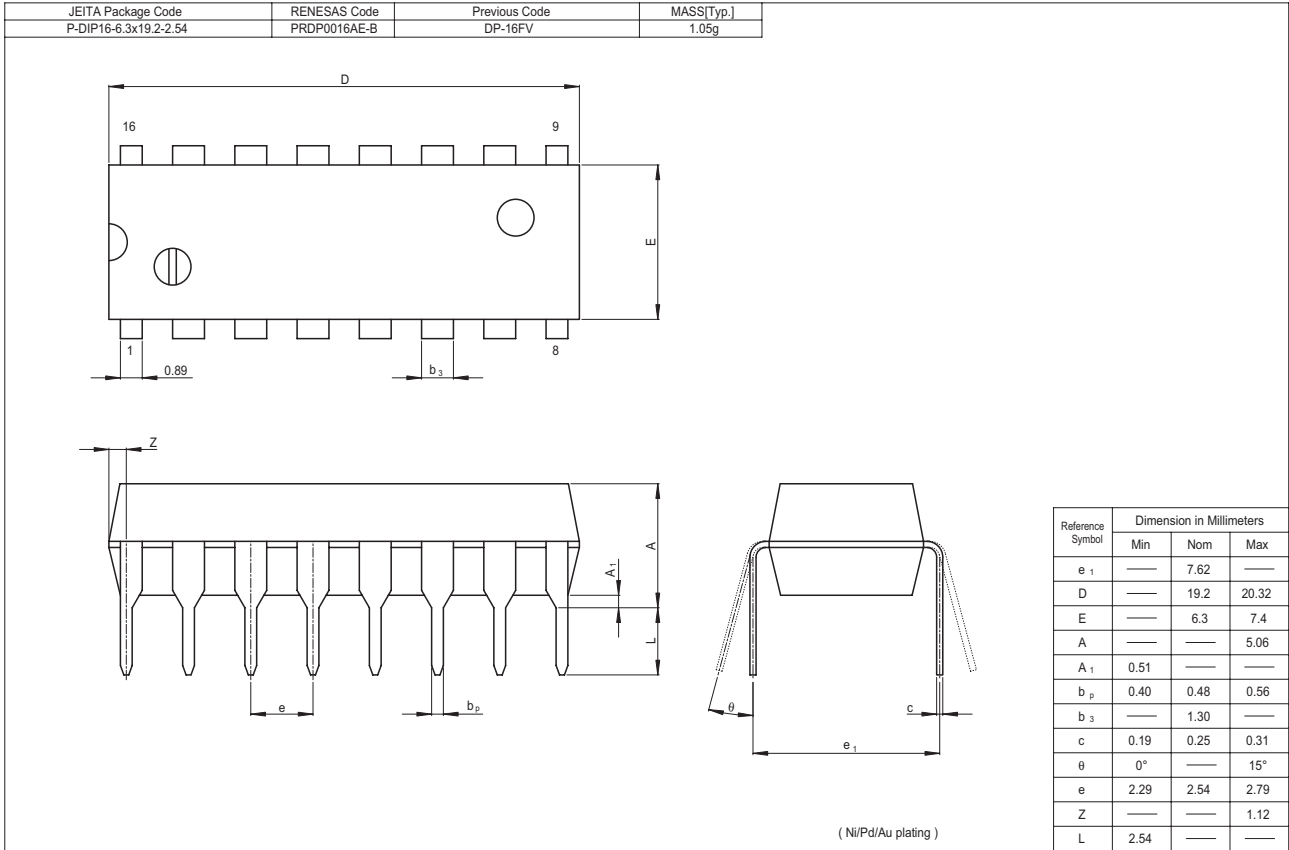


• Waveform – 2



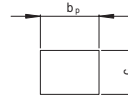
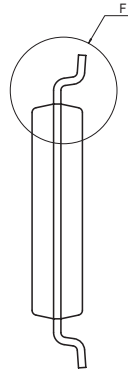
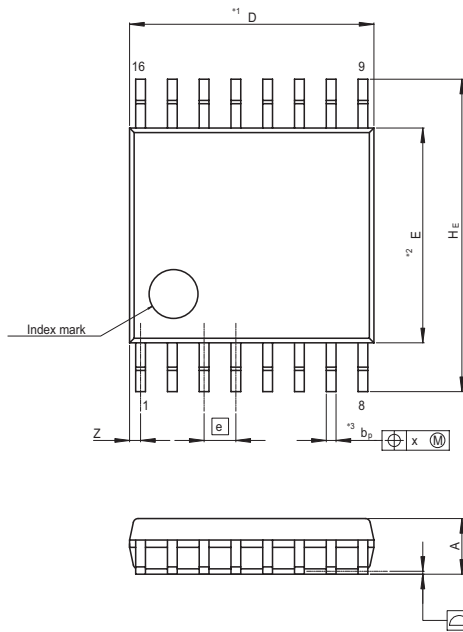
Note : Clock Input : PRR \leq 1 MHz, $Z_o = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns
 Data Input : PRR \leq 500 kHz

Package Dimensions

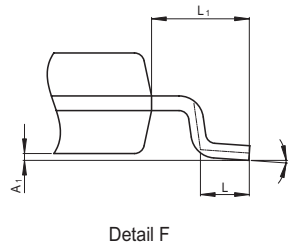


HD74HC174

JEITA Package Code P-TSSOP16-4.4x5-0.65	RENESAS Code PTSP0016JB-A	Previous Code TTP-16DAV	MASS[Typ.] 0.05g
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Terminal cross section
(Ni/Pd/Au plating)



NOTE)
1. DIMENSIONS*1 (Nom)*AND*2*
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION*3*DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.0	5.3
E	—	4.40	—
A ₂	—	—	—
A ₁	0.03	0.07	0.10
A	—	—	1.10
b _p	0.15	0.20	0.25
b ₁	—	—	—
c	0.10	0.15	0.20
c ₁	—	—	—
θ	0°	—	8°
H _E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L ₁	—	1.0	—

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