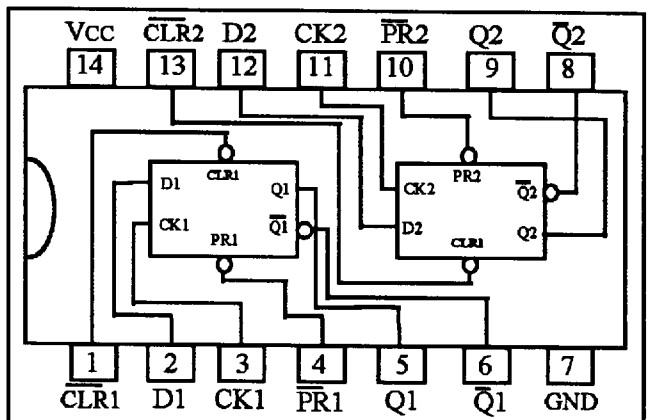
Description

The GD74F74 is a dual D-type positive edge triggered flip-flop with Direct Clear($\overline{CLR}$) and Set inputs ($\overline{PR}$) and complementary outputs(Q,$\overline{Q}$). Clock triggering occurs at a voltage level of the clock pluse and is not directly related to the transition time of the positive-going pluse. After the Clock Pluse input threshold voltage has been passed, the Data input is locked out and Data will not be transfered to the outputs until the next rising edge of the Clock Pluse input.

Pin Configuration



Dn : Data Inputs
CK : Clock Pluse Inputs
$\overline{PR}$: Direct Set Inputs
$\overline{CLR}$: Direct Clear Inputs

Function Table

Inputs				Outputs	
$\overline{PR}$	$\overline{CLR}$	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Qo	$\overline{Qo}$

↑ : Low-to-High Clock Transition
X : Immaterial
Qo : Previous Q($\overline{Q}$) before Low-to-High Clock Transition

Absolute Maximum Ratings

Storage Temperature	-65 ℃ ~ 150 ℃
Ambient Temperature Under Bias	-55 ℃ ~ 125 ℃
Junction Temperature Under Bias	-0.5 ℃ ~ 175 ℃
Vcc Voltage	-0.5 V ~ 7.0 V
Input Voltage	-0.5 V ~ 7.0 V
Input Current	-30 mA ~ 5.0 mA
Output Voltage	-0.5 V ~ Vcc

Note : Absolute Maximum ratings are values beyond which the device maybe damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Free Air Ambient Temperature..... : 0 ℃ ~ 70 ℃
Supply Voltage ..... : 4.5 V ~ 5.5 V

DC Electrical Characteristics over recommended operating free-air temperature range

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Vcc	CONDITION	TEST CIRCUIT
V_{IH}	Input High Voltage	2.0			V		- - - - - - - - -	
V_{IL}	Input Low Voltage			0.8	V		- - - - - - - - -	
V_{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I_{IN} = -18mA	See FIG. 18
V_{OH}	Output High Voltage	2.5 2.7			V	4.5 4.75	I_{OH} = - 1mA I_{OH} = - 1mA	See FIG. 19
V_{OL}	Output Low Voltage			0.5	V	Min	I_{OL} = 20 mA	
I_I	Input High Current Breakdown Test			7.0	μA	Max	V_{IN} = 7.0 V	See FIG. 20
I_{IH}	Input High Current			5.0	μA	Max	V_{IN} = 2.7 V	
I_{IL}	Input Low Current D,CK $\overline{PR}$,$\overline{CLR}$			-0.6 -1.8	mA mA	Max	V_{IN} = 0.5 V	
I_{ILK}	Input Leakage Circuit Current			1.9	μA	0.0	V_{IN} = 4.75 V All other pins grounded	See FIG. 21
I_{OLK}	Output Leakage Circuit Current			3.75	μA	0.0	V_{OUT} = 150mV All other pins grounded	See FIG. 22
I_{OS}	Output Short Circuit Current	-60		-150	mA	Max	V_{OUT} = 0 V	See FIG. 24
I_{CC}	Supply Current		10.5	16.0	mA	Max		See FIG. 25

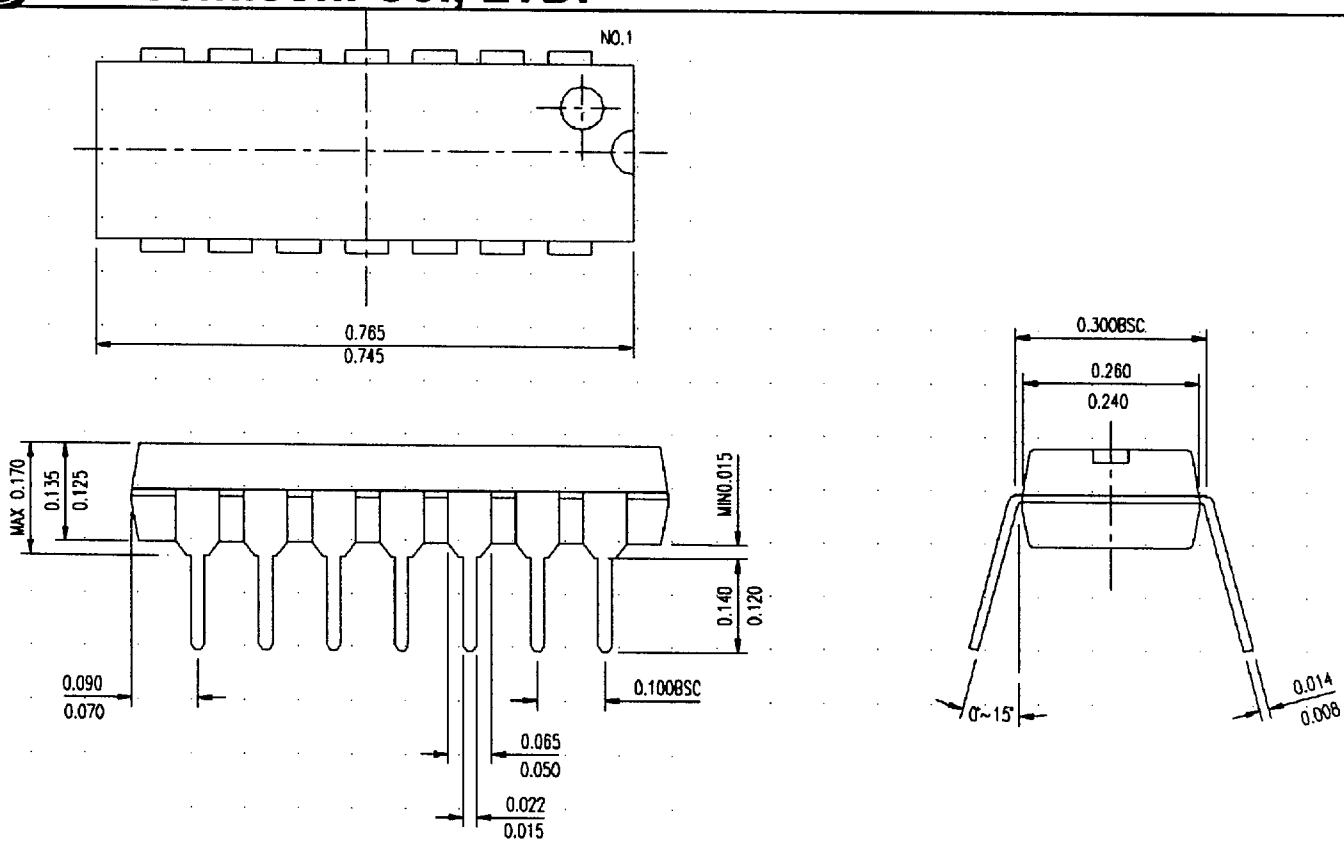
* For Ios, Not more than one output should be shorted at a time , and duration should not exceed one second

AC Characteristics

SYMBOL	PARAMETER	TEST CONDITION						UNIT
		T_A = 25 ℃ Vcc = 5.0 V C_L = 50 pF			T_A = 0 ~ 70 ℃ Vcc = 5 V ± 10 % C_L = 50pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay CK to Q or $\overline{Q}$	3.8 4.4	5.3 6.2	6.8 8.0	3.8 4.4	-- --	7.8 9.2	ns ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLR}$ or $\overline{PR}$ to Q or $\overline{Q}$	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	-- --	7.1 10.5	ns ns
f_{MAX}	Maximum clock frequency	100	125	--	100	--	--	MHz

RECOMMENDED OPERATING CONDITIONS

SYMBOL	ITEM	VALUE	UNIT
tS(H) tS(L)	Setup Time, High or Low Before CK ↑	2.0 (Ta = 25 ℃, Vcc = 5V) 3.0 (Ta = 25 ℃, Vcc = 5V)	ns
tH(H) tH(L)	Hold Time, High or Low After CK ↑	1.0 (Ta = 25 ℃, Vcc = 5V) 1.0 (Ta = 25 ℃, Vcc = 5V)	ns
tW(H) tW(L)	Pulse Width, CK High CK Low	4.0 (Ta = 25 ℃, Vcc = 5V) 5.0 (Ta = 25 ℃, Vcc = 5V)	ns
tREC	Recovery Time $\overline{CLR}$ or $\overline{PR}$ to CK	2.0 (Ta = 25 ℃, Vcc = 5V)	ns


NO.1
0.765
0.745
MAX 0.170
0.135
0.125
MIN0.015
0.140
0.120
0.090
0.070
0.100BSC
0.065
0.050
0.022
0.015
0.300BSC
0.260
0.240
0~15°
0.014
0.008