Am71/81LS95 • Am71/81LS96
Am71/81LS97 • Am71/81LS98

Three-State Octal Buffers

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus line directly
- Typical propagation delay
  Am71/81LS95, Am71/81LS97 13ns
  Am71/81LS96, Am71/81LS98 10ns
- Typical power dissipation
  Am71/81LS95, Am71/81LS97 80mW
  Am71/81LS96, Am71/81LS98 65mW
- PNP inputs reduce DC loading on bus lines
- Am71/81LS96 and Am71/81LS98 are inverting; Am71/81LS95 and Am71/81LS97 are non-inverting
- 20-pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

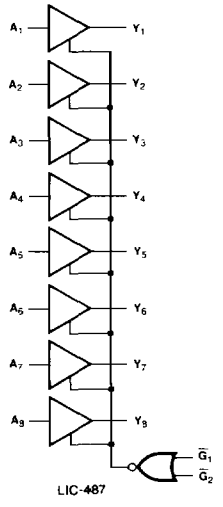
GENERAL DESCRIPTION

The Am71/81LS95, Am71/81LS96, Am71/81LS97 and Am71/81LS98 are octal buffers fabricated using Advanced Low-Power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

The Am71/81LS95 and Am71/81LS97 present true data at the outputs, while the Am71/81LS96 and Am71/81LS98 are inverting. The Am71/81LS95 and Am71/81LS96 have a common enable for all eight buffers with access through a 2-input NOR gate. The Am71/81LS97 and Am71/81LS98 octal buffers have four buffers enabled from one common line, and the other four buffers enabled from another common line. In all cases the outputs are placed in the three-state condition by applying a high logic level to the enable pins. All parts feature low current PNP inputs.

LOGIC DIAGRAMS

Am71/81LS95



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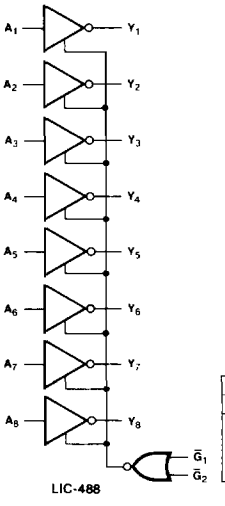
Am71/81LS96



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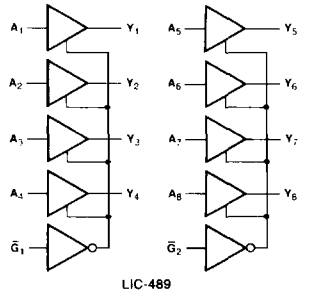
Am71/81LS97



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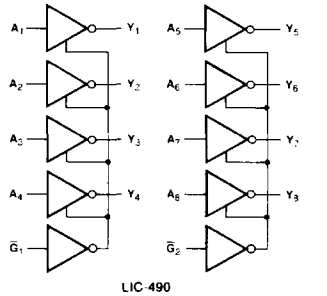
Am71/81LS98



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'LS95

INPUTS			OUTPUT
$\overline{G}_1$	$\overline{G}_2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

'LS96

INPUTS			OUTPUT
$\overline{G}_1$	$\overline{G}_2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

'LS97

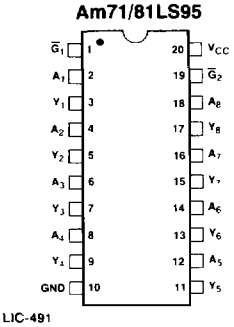
INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

'LS98

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

CONNECTION DIAGRAMS – Top Views

Am71/81LS95



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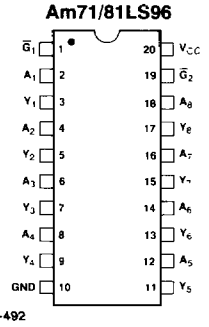
Am71/81LS96



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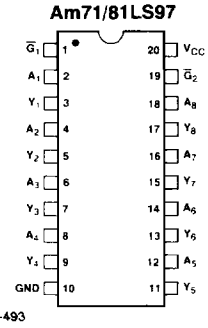
Am71/81LS97



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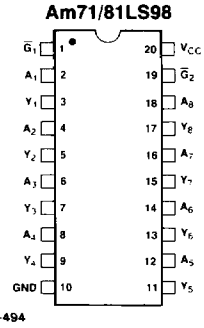
Am71/81LS98



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MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Am71/81LS95
Am71/81LS96
Am71/81LS97
Am71/81LS98

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{IH}	High Level Input Voltage				2			Volts
V_{IL}	Low Level Input Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., I_I = −18mA					−1.5	Volts
I_{OH}	High Level Output Current	MIL					−1.0	mA
		COM'L					−2.6	
V_{OH}	High Level Output Voltage	V_{CC} = Min., V_{IH} = 2.0V, V_{IL} = 0.8V	COM'L	I_{OH} = −5.0mA	2.4			Volts
				I_{OH} = −2.6mA	2.7			
			MIL, I_{OH} = −1.0mA		2.5			
I_{OL}	Low Level Output Current	COM'L					16	mA
		MIL					8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min., V_{IH} = 2.0V, V_{IL} = 0.8V	COM'L, I_{OL} = 16mA				0.5	V
			MIL, I_{OL} = 8.0mA				0.4	
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max., V_{IH} =2.0V, V_{IL} = 0.8V	V_O = 0.4V				−20	μA
			V_O = 2.4V				20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max., V_I = 7.0V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max., V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current, A Input	V_{CC} = Max.	Both $\overline{G}$ Inputs at 2.0V	V_I = 0.5V			−50	μA
	Low Level Input Current, $\overline{G}$ Input		Both $\overline{G}$ Inputs at 0.4V	V_I = 0.4V			−0.36	mA
				V_I = 0.4V			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max. (Note 2)			−30	−60	−130	mA
I_{CC}	Supply Current	V_{CC} = Max.	Am71/81LS95, Am71/81LS97			16	26	mA
			Am71/81LS96, Am71/81LS98			13	21	

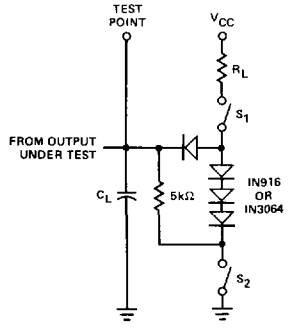
Notes: 1. All typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Not more than output should be shorted at a time, and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C

Parameters	Description	Test Conditions	Am71/81LS95 Am71/81LS97 Min.	Typ.	Max.	Am71/81LS96 Am71/81LS98 Min.	Typ.	Max.	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15pF, R_L = 2kΩ		11	16		6	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			15	22		13	17	ns
t_{ZH}	Output Enable Time to High Level			16	25		17	27	ns
t_{ZL}	Output Enable Time to Low Level			13	20		16	25	ns
t_{HZ}	Output Disable Time from HIGH Level	C_L = 5pF, R_L = 2kΩ		13	20		13	20	ns
t_{LZ}	Output Disable Time from Low Level			19	27		18	27	

SWITCHING CHARACTERISTICS TEST CONDITIONS

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



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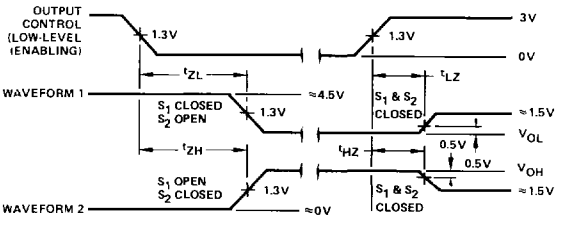
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



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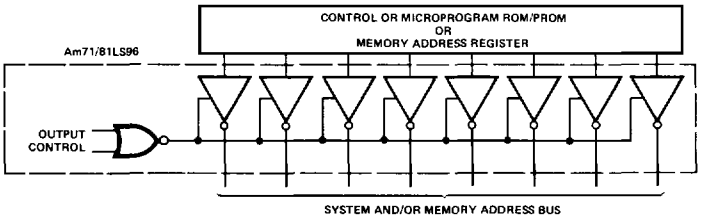
Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR ≤ 1MHz, $Z_{OUT} \approx 50\Omega$, $t_r \leq 15$ns, $t_f \leq 6$ns.
5. When measuring t_{PLH} and t_{PHL}, switches S_1 and S_2 are closed.

APPLICATIONS

Am71/81LS96 USED AS SYSTEM AND/OR MEMORY BUS DRIVER



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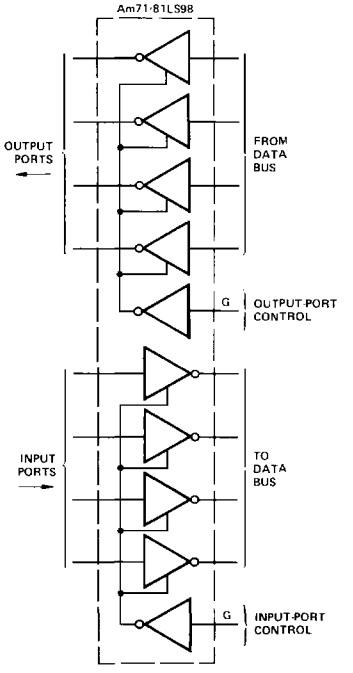
INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



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ORDERING INFORMATION

Package Type	Temperature Range	Order Number			
		Am71/81LS95	Am71/81LS96	Am71/81LS97	Am71/81LS98
Molded DIP	0°C to +70°C	DM81LS95N	DM81LS96N	DM81LS97N	DM81LS98N
Hermetic DIP	0°C to +70°C	DM81LS95J	DM81LS96J	DM81LS97J	DM81LS98J
Hermetic DIP	−55°C to +125°C	DM71LS95J	DM71LS96J	DM71LS97J	DM71LS98J
Dice	0°C to +70°C	AM81LS95X	AM81LS96X	AM81LS97X	AM81LS98X

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