FAIRCHILD SEMICONDUCTOR™

April 1988
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74F257A
Quad 2-Input Multiplexer with 3-STATE Outputs

General Description

The 74F257A is a quad 2-input multiplexer with 3-STATE outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

Features

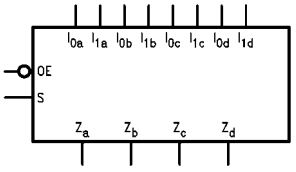
- Multiplexer expansion by tying outputs together
- Non-inverting 3-STATE outputs
- Input clamp diodes limit high-speed termination effects

Ordering Code:

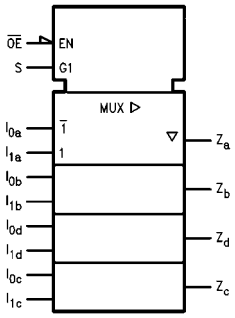
Order Number	Package Number	Package Description
74F257ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F257ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F257APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

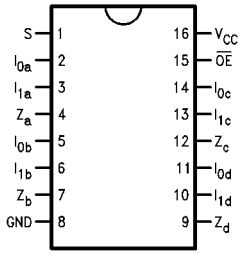
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
S	Common Data Select Input	1.0/1.0	20 µA/–0.6 mA
$\overline{OE}$	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
I_{0a}–I_{0d}	Data Inputs from Source 0	1.0/1.0	20 µA/–0.6 mA
I_{1a}–I_{1d}	Data Inputs from Source 1	1.0/1.0	20 µA/–0.6 mA
Z_a–Z_d	3-STATE Multiplexer Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)

Truth Table

Output Enable	Select Input	Data Inputs		Output
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

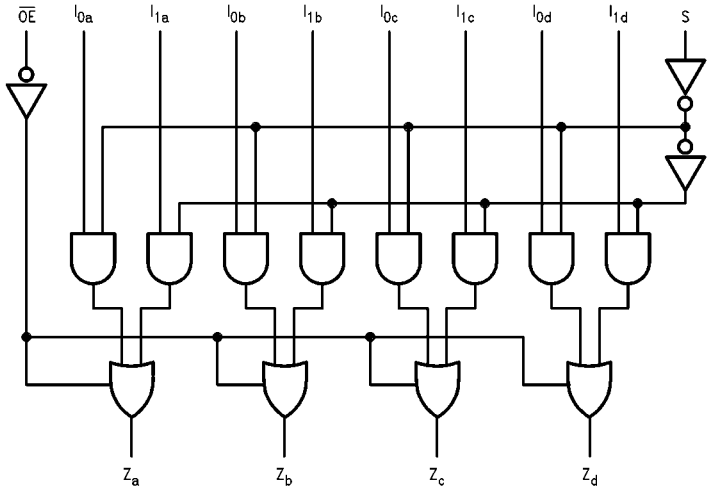
Functional Description

The 74F257A is a quad 2-input multiplexer with 3-STATE outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equation for the outputs is shown below:

$$Z_n = \overline{OE} \bullet (I_n \bullet S + I_{on} \bullet \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-STATE devices whose outputs are tied together are designed so there is no overlap.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

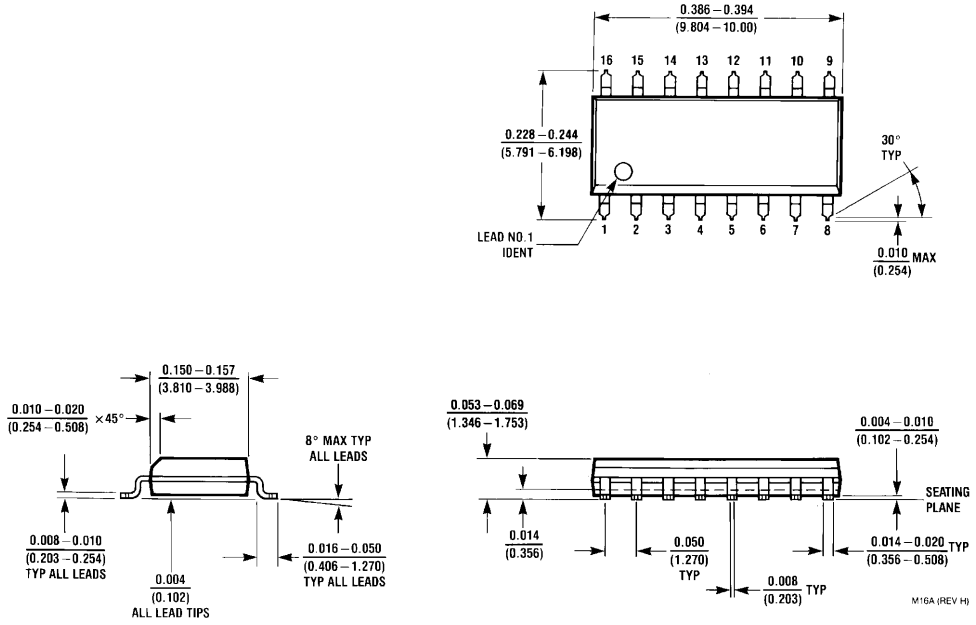
DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		10% V_{CC}	2.4					I_{OH} = −3 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 24 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	µA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	µA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			9.0	15	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			14.5	22	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			15	23	mA	Max	V_O = HIGH Z

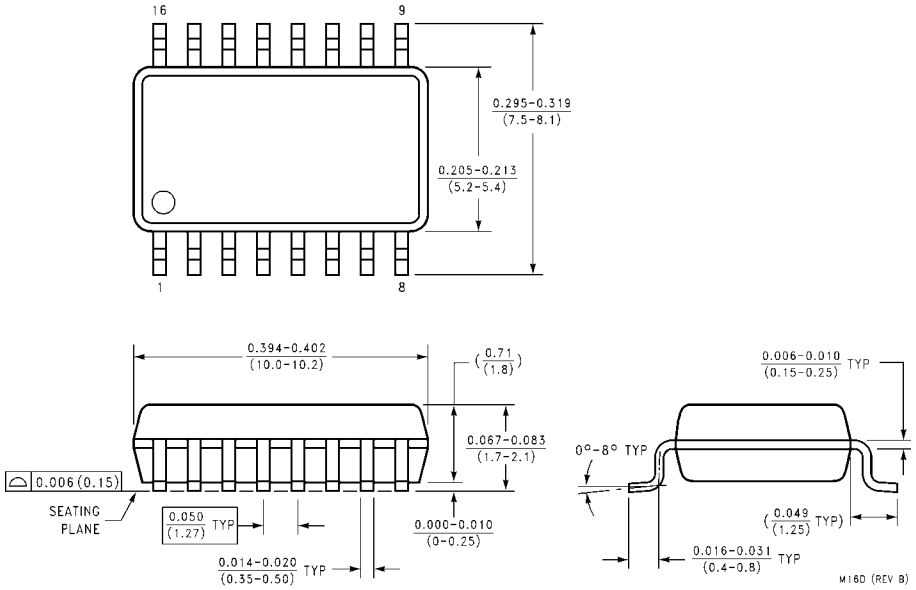
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = 5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	2.5	4.5	5.5	2.0	7.0	2.0	6.0	ns
t_{PHL}	I_n to Z_n	2.0	4.2	5.5	1.5	7.0	2.0	6.0	
t_{PLH}	Propagation Delay	4.0	5.0	9.5	3.5	11.5	3.5	10.5	ns
t_{PHL}	S to Z_n	2.5	6.5	7.0	2.5	9.0	2.5	8.0	
t_{PZH}	Output Enable Time	2.0	5.9	6.0	2.0	8.0	2.0	7.0	ns
t_{PZL}		2.5	5.5	7.0	2.5	9.0	2.5	8.0	
t_{PHZ}	Output Disable Time	2.0	4.3	6.0	2.0	7.0	2.0	7.0	
t_{PLZ}		2.0	4.5	6.0	2.0	8.5	2.0	7.0	

Physical Dimensions inches (millimeters) unless otherwise noted

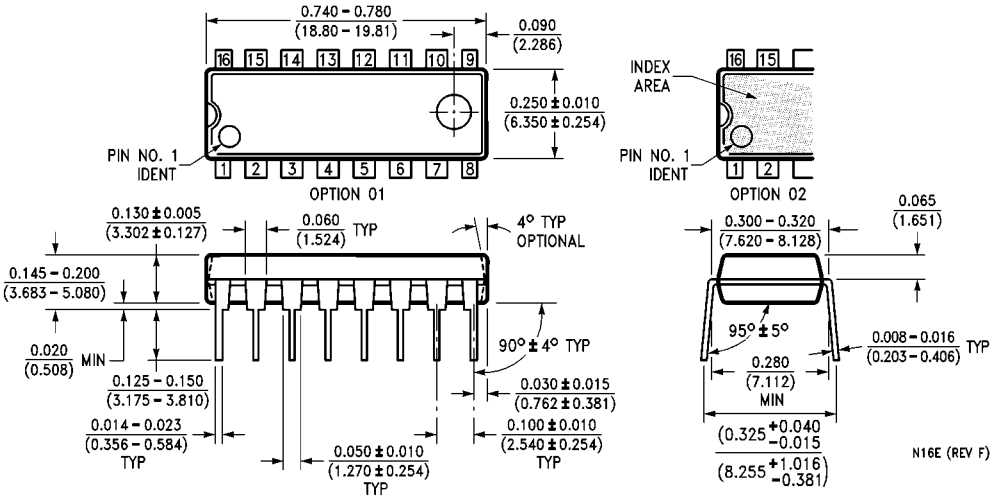


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E