

## 74F240 • 74F241 • 74F244

### Octal Buffers/Line Drivers with 3-STATE Outputs

#### General Description

The 74F240, 74F241 and 74F244 are octal buffers and line drivers designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC and board density.

#### Features

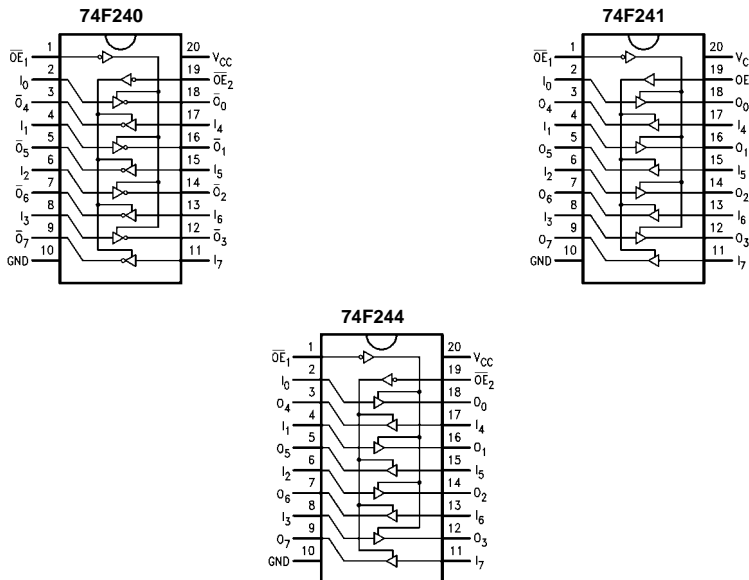
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 64 mA (48 mA mil)
- 12 mA source current
- Input clamp diodes limit high-speed termination effects

#### Ordering Code:

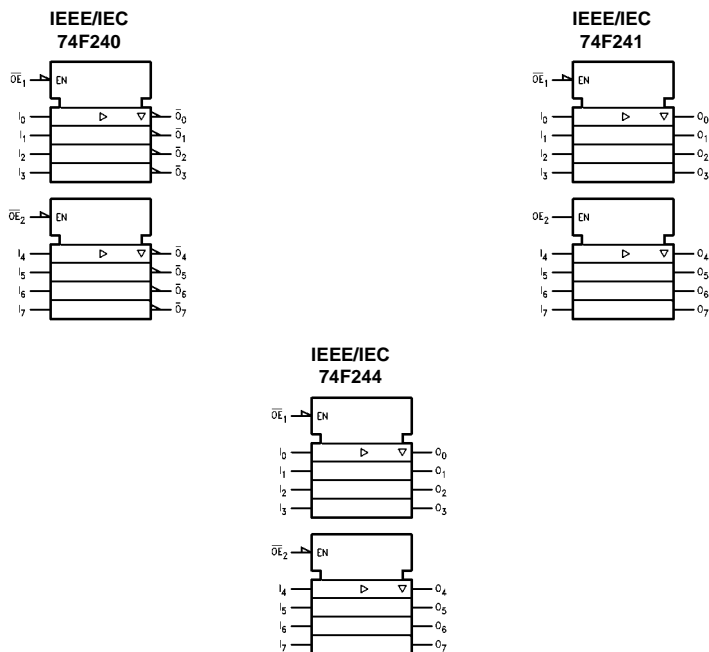
Order Code	Package Number	Package Description
74F240SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F240PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F241SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F241SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F241PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F244SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F244MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74F244PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagrams



### Logic Symbols



### Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Input (Active LOW)	1.0/1.667	20 $\mu$ A/-1 mA
$OE_2$	3-STATE Output Enable Input (Active HIGH)	1.0/1.667	20 $\mu$ A/-1 mA
$I_0-I_7$	Inputs (74F240)	1.0/1.667 (Note 1)	20 $\mu$ A/-1 mA
$I_0-I_7$	Inputs (74F241, 74F244)	1.0/2.667 (Note 1)	20 $\mu$ A/-1.6 mA
$\overline{O}_0-\overline{O}_7, O_0-O_7$	Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)

Note 1: Worst-case 74F240 enabled; 74F241, 74F244 disabled

### Truth Tables

74F240

$\overline{OE}_1$	$D_{1n}$	$O_{1n}$	$\overline{OE}_2$	$D_{2n}$	$O_{2n}$
H	X	Z	H	X	Z
L	H	L	L	H	L
L	L	H	L	L	H

74F244

$\overline{OE}_1$	$D_{1n}$	$O_{1n}$	$\overline{OE}_2$	$D_{2n}$	$O_{2n}$
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

74F241

$\overline{OE}_1$	$D_{1n}$	$O_{1n}$	$OE_2$	$D_{2n}$	$O_{2n}$
H	X	Z	L	X	Z
L	H	H	H	H	H
L	L	L	H	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

**Absolute Maximum Ratings**(Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

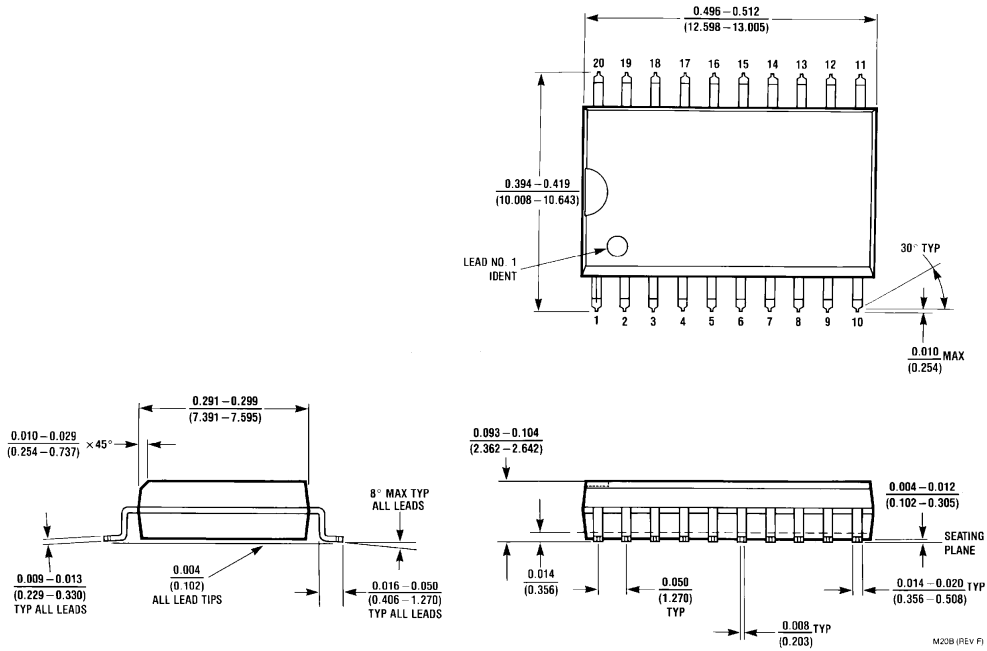
**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.4		V	Min	I <sub>OH</sub> = -3 mA
		10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = -15 mA
		5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage			0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>ID</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-1.0 -1.6	mA	Max	V <sub>IN</sub> = 0.5V ( $\overline{OE}_1, \overline{OE}_2, OE_2, D_n$ 74F240)) V <sub>IN</sub> = 0.5V (D <sub>n</sub> (74F241, 74F244))
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current (74F240)		19	29	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (74F240)		50	75	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current (74F240)		42	63	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current (74F241, 74F244)		40	60	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (74F241, 74F244)		60	90	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current (74F241, 74F244)		60	90	mA	Max	V <sub>O</sub> = HIGH Z

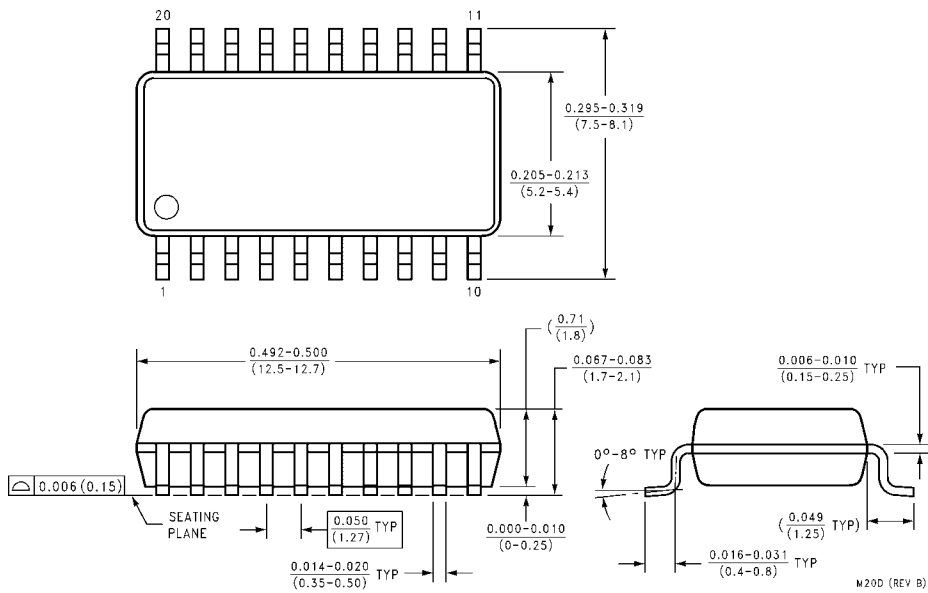
## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = 5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	3.0	5.1	7.0	3.0	9.0	3.0	8.0	ns
t <sub>PHL</sub>	Data to Output (74F240)	2.0	3.5	4.7	2.0	6.0	2.0	5.7	
t <sub>pZH</sub>	Output Enable Time (74F240)	2.0	3.5	4.7	2.0	6.5	2.0	5.7	ns
t <sub>pZL</sub>		4.0	6.9	9.0	4.0	10.5	4.0	10.0	
t <sub>PHZ</sub>	Output Disable Time (74F240)	2.0	4.0	5.3	2.0	6.5	2.0	6.3	ns
t <sub>PLZ</sub>		2.0	6.0	8.0	2.0	12.5	2.0	9.5	
t <sub>PLH</sub>	Propagation Delay	2.5	4.0	5.2	2.0	6.5	2.5	6.2	ns
t <sub>PHL</sub>	Data to Output (74F241, 74F244)	2.5	4.0	5.2	2.0	7.0	2.5	6.5	
t <sub>pZH</sub>	Output Enable Time (74F241, 74F244)	2.0	4.3	5.7	2.0	7.0	2.0	6.7	ns
t <sub>pZL</sub>		2.0	5.4	7.0	2.0	8.5	2.0	8.0	
t <sub>PHZ</sub>	Output Disable Time (74F241, 74F244)	2.0	4.5	6.0	2.0	7.0	2.0	7.0	ns
t <sub>PLZ</sub>		2.0	4.5	6.0	2.0	7.5	2.0	7.0	

**Physical Dimensions** inches (millimeters) unless otherwise noted

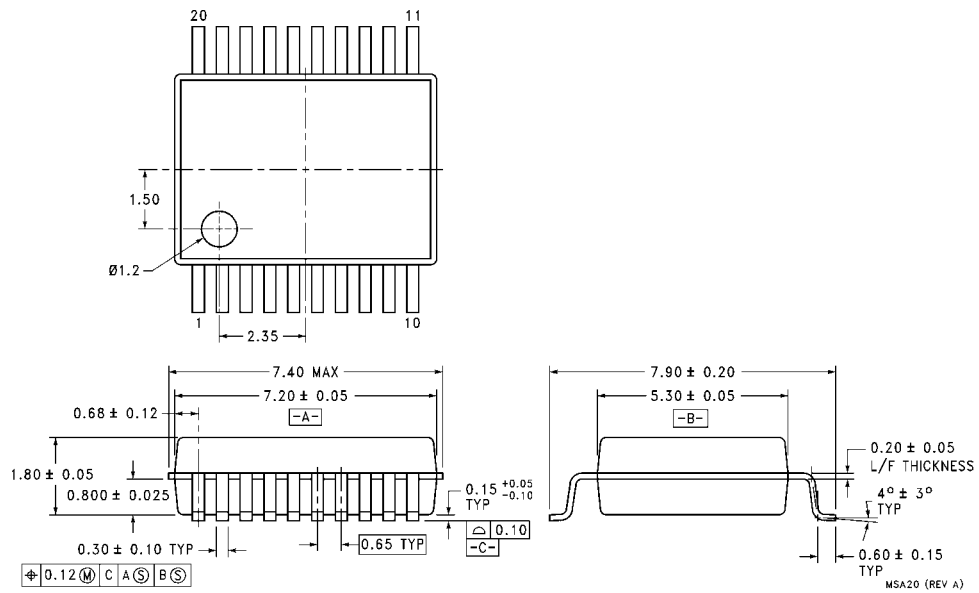


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B**



**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D**

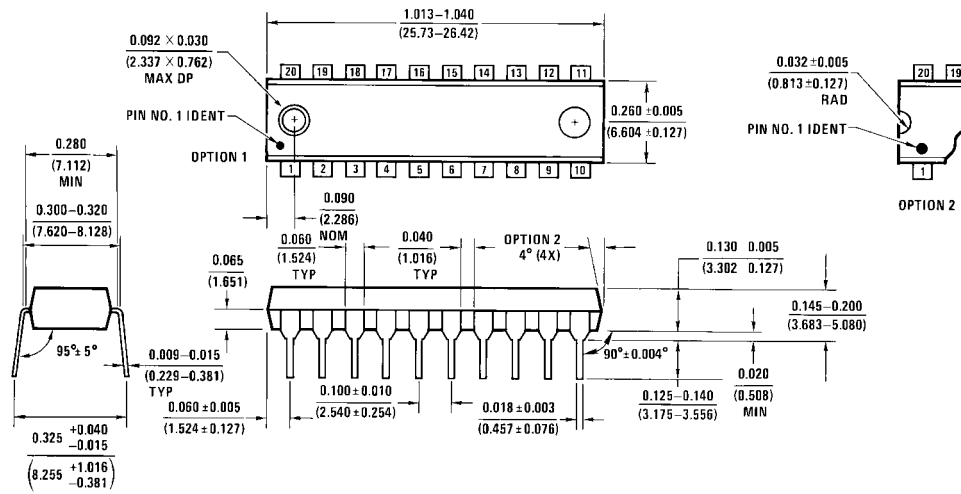
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA20**

MSA20 (REV A)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N20A**

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