

74F182 Carry Lookahead Generator

General Description

The 74F182 is a high-speed carry lookahead generator. It is generally used with the 74F181 or 74F381 4-bit arithmetic logic units to provide high-speed lookahead over word lengths of more than four bits.

Features

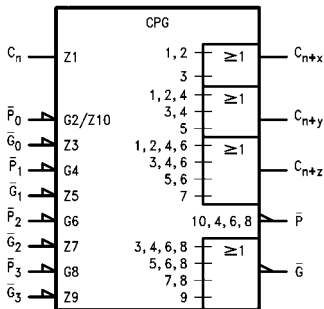
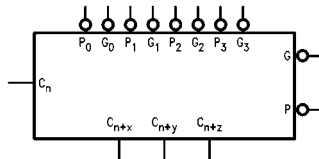
- Provides lookahead carries across a group of four ALUs
- Multi-level lookahead high-speed arithmetic operation over long word lengths

Ordering Code:

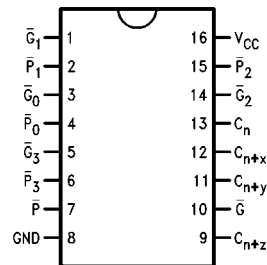
Order Number	Package Number	Package Description
74F182SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F182PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
C _n	Carry Input	1.0/2.0	20 μA/-1.2 mA
$\overline{G}_0, \overline{G}_2$	Carry Generate Inputs (Active LOW)	1.0/14.0	20 μA/-8.4 mA
\overline{G}_1	Carry Generate Input (Active LOW)	1.0/16.0	20 μA/-9.6 mA
\overline{G}_3	Carry Generate Input (Active LOW)	1.0/8.0	20 μA/-4.8 mA
$\overline{P}_0, \overline{P}_1$	Carry Propagate Inputs (Active LOW)	1.0/8.0	20 μA/-4.8 mA
\overline{P}_2	Carry Propagate Input (Active LOW)	1.0/6.0	20 μA/-3.6 mA
\overline{P}_3	Carry Propagate Input (Active LOW)	1.0/4.0	20 μA/-2.4 mA
C _{n+x} - C _{n+z}	Carry Outputs	50/33.3	-1 mA/20 mA
\overline{G}	Carry Generate Output (Active LOW)	50/33.3	-1 mA/20 mA
\overline{P}	Carry Propagate Output (Active LOW)	50/33.3	-1 mA/20 mA

Functional Description

The 74F182 carry lookahead generator accepts up to four pairs of Active LOW Carry Propagate (\overline{P}_0 - \overline{P}_3) and Carry Generate (\overline{G}_0 - \overline{G}_3) signals and an Active HIGH Carry input (C_n) and provides anticipated Active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 74F182 also has Active LOW Carry Propagate (\overline{P}) and Carry Generate (\overline{G}) outputs which may be used for further levels of lookahead. The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

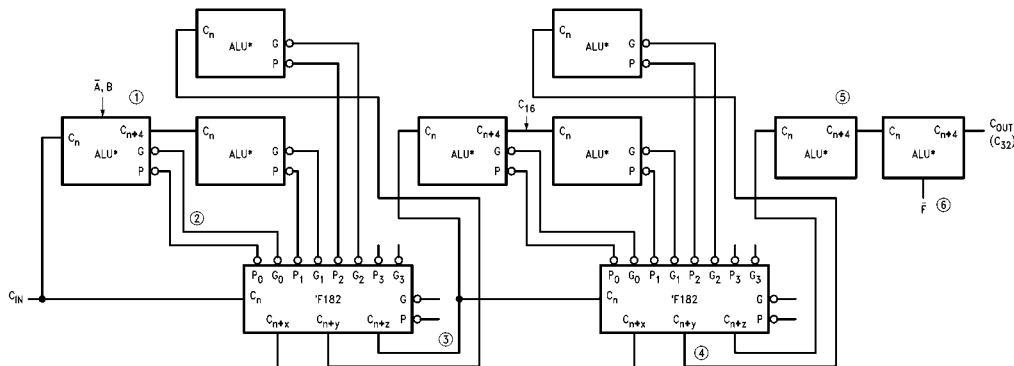
$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

$$G = \overline{G}_3 + \overline{P}_3 \overline{G}_2 + \overline{P}_3 \overline{P}_2 \overline{G}_1 + \overline{P}_3 \overline{P}_2 \overline{P}_1 \overline{G}_0$$

$$P = \overline{P}_2 \overline{P}_2 \overline{P}_1 \overline{P}_0$$

Also, the 74F182 can be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections (Figure 1) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last 74F182 or 74F381.



*ALUs may be either 74F181 or 74F381

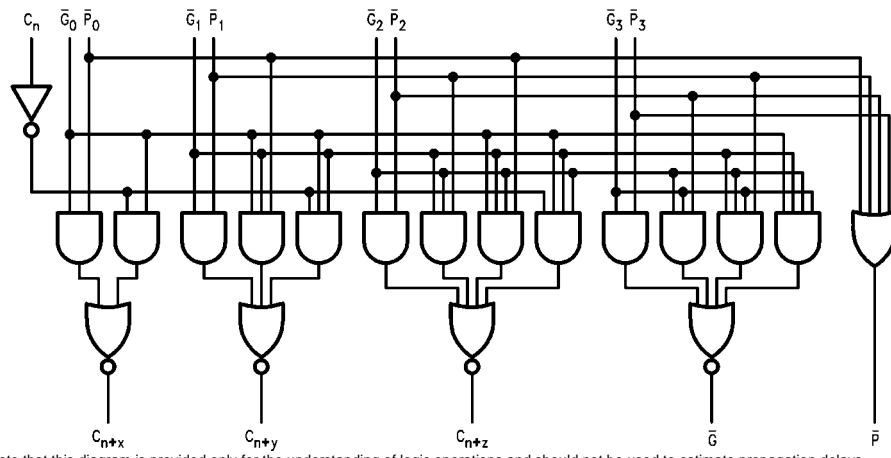
FIGURE 1. 32-Bit ALU with Rippled Carry between 16-Bit Lookahead ALUs

Truth Table

Inputs									Outputs				
C _n	\overline{G}_0	\overline{P}_0	\overline{G}_1	\overline{P}_1	\overline{G}_2	\overline{P}_2	\overline{G}_3	\overline{P}_3	C _{n+x}	C _{n+y}	C _{n+z}	\overline{G}	\overline{P}
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
X			X	X	X	X	H	H				H	
X			X	X	H	H	H	X				H	
X			H	H	H	X	H	X				H	
H			H	X	H	X	H	X				H	
X			X	X	X	X	L	X				L	
X			X	X	L	X	X	L				L	
X			L	X	X	L	X	L				L	
L			X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

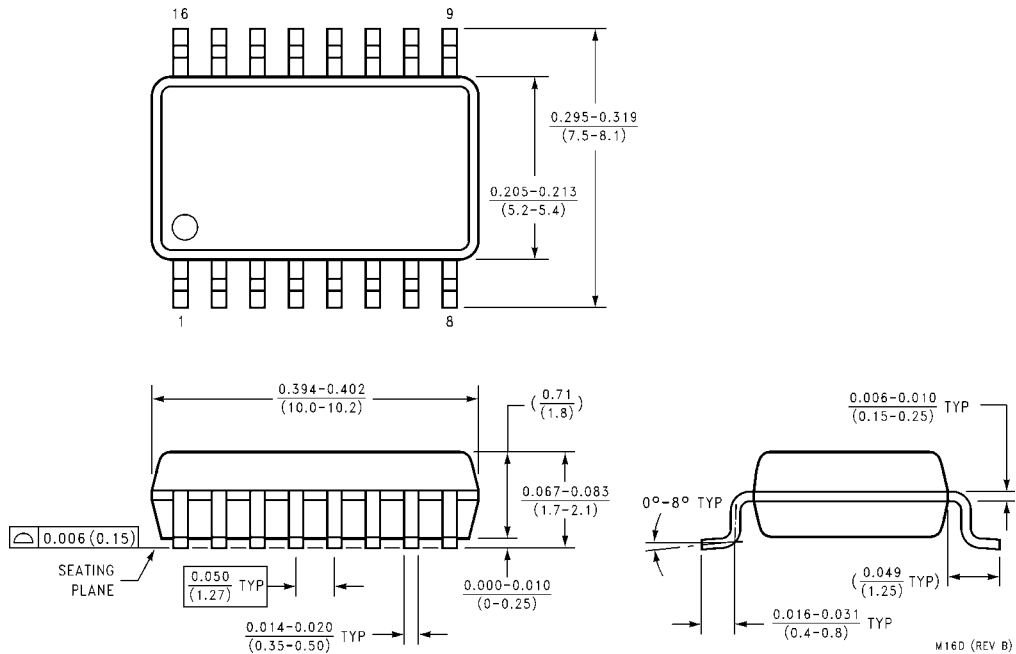
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA
		5% V _{CC}	2.7				I _{OH} = -1 mA
V _{OL}	Output LOW Voltage			0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEx}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-1.2	mA	Max	V _{IN} = 0.5V (C _n)
				-2.4			V _{IN} = 0.5V (\bar{P}_3)
				-3.6			V _{IN} = 0.5V (\bar{P}_2)
				-4.8			V _{IN} = 0.5V ($\bar{G}_3, \bar{P}_0, \bar{P}_1$)
				-8.4			V _{IN} = 0.5V (\bar{G}_0, \bar{G}_2)
				-9.6		V _{IN} = 0.5V (\bar{G}_1)	
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		18.4	28.0	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		23.5	36.0	mA	Max	V _O = LOW

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0	6.6	8.5	3.0	12.0	3.0	9.5	ns
t_{PHL}	C_n to C_{n+x} , C_{n+y} , C_{n+z}	3.0	6.8	9.0	3.0	11.0	3.0	10.0	
t_{PLH}	Propagation Delay	2.5	6.2	8.0	2.5	11.0	2.5	9.0	ns
t_{PHL}	\bar{P}_0 , \bar{P}_1 , or \bar{P}_2 to C_{n+x} , C_{n+y} , or C_{n+z}	1.5	3.7	5.0	1.0	7.0	1.5	6.0	
t_{PLH}	Propagation Delay	2.5	6.5	8.5	2.5	11.0	2.5	9.5	ns
t_{PHL}	\bar{G}_0 , \bar{G}_1 , or \bar{G}_2 to C_{n+x} , C_{n+y} , or C_{n+z}	1.5	3.9	5.2	1.0	7.0	1.5	6.0	
t_{PLH}	Propagation Delay	3.0	7.9	10.0	3.0	12.0	3.0	11.0	ns
t_{PHL}	\bar{P}_1 , \bar{P}_2 , or \bar{P}_3 to \bar{G}	3.0	6.0	8.0	2.5	10.0	3.0	9.0	
t_{PLH}	Propagation Delay	3.0	8.3	10.5	3.0	12.0	3.0	11.5	ns
t_{PHL}	\bar{G}_n to \bar{G}	3.0	5.7	7.5	2.5	10.0	3.0	8.5	
t_{PLH}	Propagation Delay	3.0	5.7	7.5	2.5	10.0	3.0	8.5	ns
t_{PHL}	\bar{P}_n to \bar{P}	2.5	4.1	5.5	2.5	8.0	2.5	6.5	

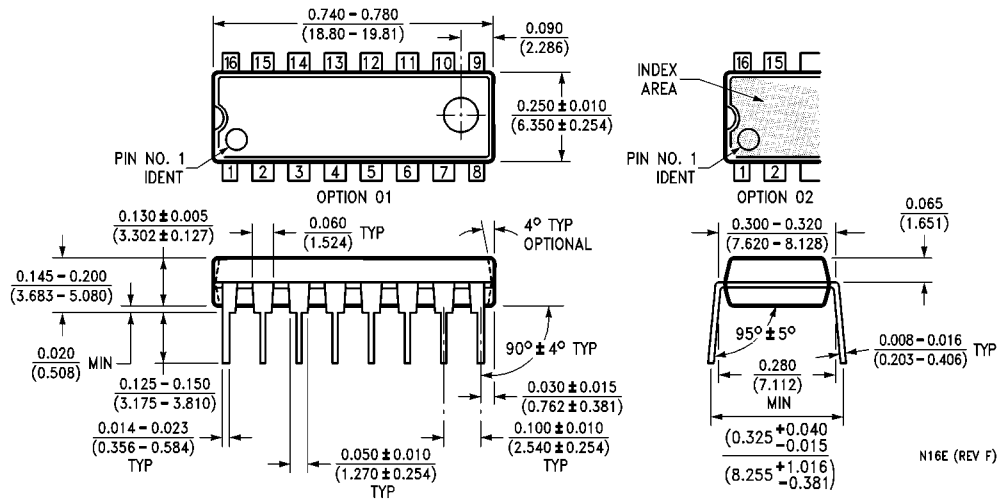
Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

M16D (REV B)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com