

November 1988 Revised November 1999

#### 74AC11

## **Triple 3-Input AND Gate**

#### **General Description**

The AC11 contains three 3-input AND gates.

#### **Features**

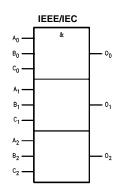
- I<sub>CC</sub> reduced by 50%
- Outputs source/sink 24 mA

## **Ordering Code:**

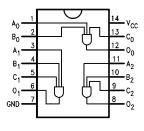
Order Number	Package Number	Package Description				
74AC11SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow				
74AC11MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide				
74AC11PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide				

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### **Logic Symbol**



#### **Connection Diagram**



#### **Pin Descriptions**

Pin Names	Description			
$A_n, B_n, C_n$	Inputs			
$O_n$	Outputs			

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#### **Absolute Maximum Ratings**(Note 1)

-0.5V to +7.0V Supply Voltage (V<sub>CC</sub>)

DC Input Diode Current  $(I_{IK})$ 

 $V_{I} = -0.5V$ -20 mA  $V_I = V_{CC} + 0.5V$ +20 mA DC Input Voltage (V<sub>I</sub>) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Diode Current (I<sub>OK</sub>)

 $V_O = -0.5V$ -20 mA  $V_O = V_{CC} + 0.5V$ +20 mA DC Output Voltage (V<sub>O</sub>) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Source

or Sink Current (I<sub>O</sub>)  $\pm$  50 mA

DC  $V_{CC}$  or Ground Current

per Output Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm$  50 mA -65°C to +150°C

Storage Temperature (T<sub>STG</sub>) Junction Temperature (T<sub>J</sub>)

PDIP 140°C

#### **Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ ) 2.0V to 6.0V 0V to  $V_{CC}$ Input Voltage (V<sub>I</sub>) 0V to  $V_{\mbox{\footnotesize CC}}$ Output Voltage (V<sub>O</sub>) Operating Temperature (T<sub>A</sub>) -40°C to +85°C Minimum Input Edge Rate  $(\Delta V/\Delta t)$ 125 mV/ns

 $V_{\mbox{\scriptsize IN}}$  from 30% to 70% of  $V_{\mbox{\scriptsize CC}}$ V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

#### **DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = +25°C		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions
Symbol		(V)	Typ Guaranteed Limits		Units	Conditions	
V <sub>IH</sub>	Minimum HIGH Level	3.0	1.5	2.1	2.1		V <sub>OUT</sub> = 0.1V
	Input Voltage	4.5	2.25	3.15	3.15	V	or V <sub>CC</sub> - 0.1V
		5.5	2.75	3.85	3.85		
V <sub>IL</sub>	Maximum LOW Level	3.0	1.5	0.9	0.9		V <sub>OUT</sub> = 0.1V
	Input Voltage	4.5	2.25	1.35	1.35	V	or V <sub>CC</sub> – 0.1V
		5.5	2.75	1.65	1.65		
V <sub>OH</sub>	Minimum HIGH Level	3.0	2.99	2.9	2.9		
	Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or $V_{IH}$
		3.0		2.56	2.46		$I_{OH} = -12 \text{ mA}$
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$
		5.5		4.86	4.76		I <sub>OH</sub> = -24 mA (Note 2)
V <sub>OL</sub>	Maximum LOW Level	3.0	0.002	0.1	0.1		
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or $V_{IH}$
		3.0		0.36	0.44		I <sub>OL</sub> = 12 mA
		4.5		0.36	0.44	V	I <sub>OL</sub> = 24 mA
		5.5		0.36	0.44		I <sub>OL</sub> = 24 mA (Note 2)
I <sub>IN</sub>	Maximum Input	5.5		± 0.1	± 1.0	μА	$V_I = V_{CC}$
(Note 4)	Leakage Current	5.5		± 0.1	± 1.0	μА	GND
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current (Note 3)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent	5.5		2.0	20.0	μА	$V_{IN} = V_{CC}$
(Note 4)	Supply Current	5.5		2.0	20.0	μΑ	or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

## **AC Electrical Characteristics**

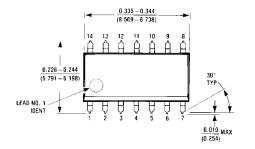
		V <sub>CC</sub>	T <sub>A</sub> = +25°C			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		
Symbol Parameter (V) $C_L = 50 \text{ pF}$			$C_L = 50 \text{ pF}$		Units			
		(Note 5)	Min	Тур	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	5.5	9.5	1.0	10.0	ns
		5.0	1.5	4.0	8.0	1.0	8.5	115
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	5.5	8.5	1.0	9.5	ns
		5.0	1.5	4.0	7.0	1.0	7.5	115

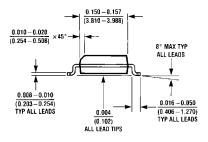
Note 5: Voltage Range 3.3 is  $3.3V \pm 0.3V$ Voltage Range 5.0 is  $5.0V \pm 0.5V$ 

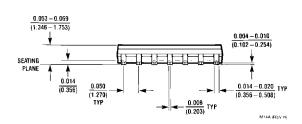
#### Capacitance

Symbol	Parameter	Тур	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	20.0	pF	$V_{CC} = 5.0V$

## Physical Dimensions inches (millimeters) unless otherwise noted

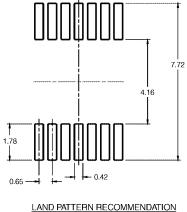


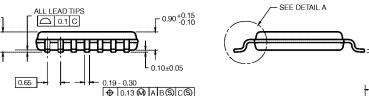




14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

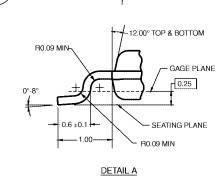
# Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 5.0±0.1 -A-6.4 4.4±0.1 -B-3.2 0.2 C B A ALL LEAD TIPS PIN #1 IDENT. ALL LEAD TIPS 1.2 MAX - 0.90 +0.15 -C-- 0.10±0.05 0.19 - 0.30 **♦** 0.13 **№** A B**⑤** C**⑤** NOTES:





- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

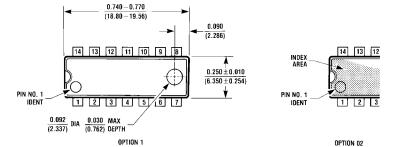
MTC14RevC3

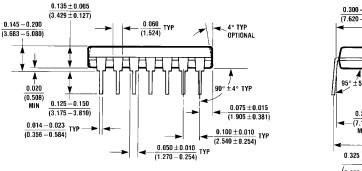


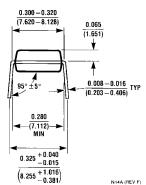
- 0.09-0.20

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)







14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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