74HC4051; 74HCT4051

8-channel analog multiplexer/demultiplexer

Product data sheet

1. General description

The 74HC4051; 74HCT4051 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). The device is specified in compliance with JEDEC standard no. 7A.

The 74HC4051; 74HCT4051 is an 8-channel analog multiplexer/demultiplexer with three digital select inputs (S0 to S2), an active-LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S0 to S2. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S0 to S2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S0 to S2, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 V to 10.0 V for 74HC4051 and 4.5 V to 5.5 V for 74HCT4051. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

2. Features

- Wide analog input voltage range: ±5 V
- Low ON-state resistance:
  - 80 Ω (typical) at $V_{CC} - V_{EE}$ = 4.5 V
  - 70 Ω (typical) at $V_{CC} - V_{EE}$ = 6.0 V
  - 60 Ω (typical) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation:
  - To enable 5 V logic to communicate with ±5 V analog signals
- Typical ‘break before make’ built in

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

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4. Quick reference data

Table 1: Quick reference data

V_{EE} = GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC4051						
t_{PZH}, t_{PZL}	turn-ON time	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V				
	$\overline{E}$ to V_{os}		-	22	-	ns
	Sn to V_{os}		-	20	-	ns
t_{PHZ}, t_{PLZ}	turn-OFF time	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V				
	$\overline{E}$ to V_{os}		-	18	-	ns
	Sn to V_{os}		-	19	-	ns
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance (per switch)	[1] [2]	-	25	-	pF
C_S	switch capacitance					
	independent input/output Yn		-	5	-	pF
	common input/output Z		-	25	-	pF
Type 74HCT4051						
t_{PZH}, t_{PZL}	turn-ON time	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V				
	$\overline{E}$ to V_{os}		-	22	-	ns
	Sn to V_{os}		-	24	-	ns
t_{PHZ}, t_{PLZ}	turn-OFF time	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V				
	$\overline{E}$ to V_{os}		-	16	-	ns
	Sn to V_{os}		-	20	-	ns
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance (per switch)	[1] [3]	-	25	-	pF
C_S	switch capacitance					
	independent input/output Yn		-	5	-	pF
	common input/output Z		-	25	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs;
C_L = output load capacitance in pF;
C_S = switch capacitance in pF;
V_{CC} = supply voltage in V.

[2] For 74HC4051 the condition is V_I = GND to V_{CC}.

[3] For 74HCT4051 the condition is V_I = GND to V_{CC} − 1.5 V.

5. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
Type 74HC4051				
74HC4051N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC4051D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4051DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4051PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4051BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
Type 74HCT4051				
74HCT4051N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT4051D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4051DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4051PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4051BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

8. Functional description

8.1 Function table

Table 4: Function table [1]

Input				Channel ON
$\overline{E}$	S2	S1	S0	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	-

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{EE} = GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage		[1]	–0.5	+11.0	V
I_{IK}	input clamping current	V_I < –0.5 V or V_I > V_{CC} + 0.5 V		-	±20	mA
I_{SK}	switch clamping current	V_S < –0.5 V or V_S > V_{CC} + 0.5 V		-	±20	mA
I_S	switch current	V_S = –0.5 V to (V_{CC} + 0.5 V)		-	±25	mA
I_{EE}	negative supply current			-	±20	mA
I_{CC}	quiescent supply current			-	50	mA
I_{GND}	ground supply current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
	DIP16 package		[2]	-	750	mW
	SO16, (T)SSOP16, and DHVQFN16 package		[3]	-	500	mW
P_S	power dissipation per switch			-	100	mW

[1] To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Yn. In this case there is no limit for the voltage drop across the switch, but the voltages at Yn and Z may not exceed V_{CC} or V_{EE}.

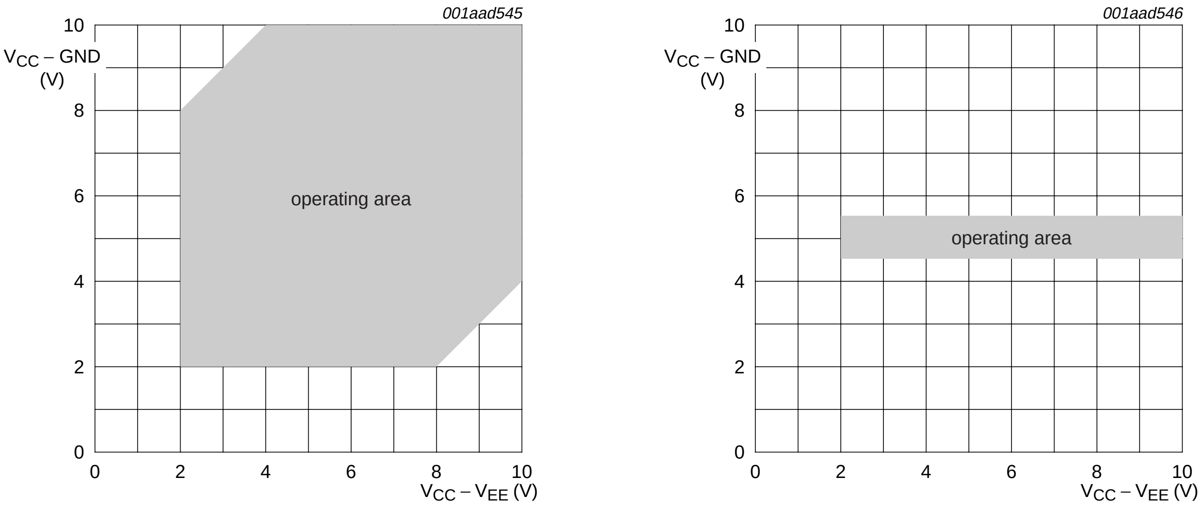
[2] For DIP16 packages, above 70 °C, P_{tot} derates linearly with 12 mW/K.

[3] For SO16, (T)SSOP16, and DHVQFN16 packages, above 70 °C, P_{tot} derates linearly with 8 mW/K.

10. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC4051						
ΔV_{CC}	supply voltage difference	see Figure 7				
	V_{CC} – GND		2.0	5.0	10.0	V
	V_{CC} – V_{EE}		2.0	5.0	10.0	V
V_I	input voltage		GND	-	V_{CC}	V
V_S	switch voltage		V_{EE}	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	-	6.0	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	6.0	400	ns
		V_{CC} = 10.0 V	-	6.0	250	ns
Type 74HCT4051						
ΔV_{CC}	supply voltage difference	see Figure 7				
	V_{CC} – GND		4.5	5.0	5.5	V
	V_{CC} – V_{EE}		2.0	5.0	10.0	V
V_I	input voltage		GND	-	V_{CC}	V
V_S	switch voltage		V_{EE}	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	-	6.0	500	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	6.0	500	ns
		V_{CC} = 10.0 V	-	6.0	500	ns



a. Type 74HC4051 b. Type 74HCT4051

Fig 7. Guaranteed operating area as a function of the supply voltages

11. Static characteristics

Table 7: R_{ON} resistance per switch for types 74HC4051 and 74HCT4051

$V_I = V_{IH}$ or V_{IL}; for test circuit see Figure 8.
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.
For 74HC4051: V_{CC} – GND or V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.
For 74HCT4051: V_{CC} – GND = 4.5 V and 5.5 V; V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
$R_{ON(peak)}$	ON-state resistance (peak)	V_{is} = V_{CC} to V_{EE}				
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA [1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA	-	100	180	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA	-	90	160	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA	-	70	130	Ω
$R_{ON(rail)}$	ON-state resistance (rail)	V_{is} = V_{EE}				
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA [1]	-	150	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA	-	80	140	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA	-	70	120	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA	-	60	105	Ω
		V_{is} = V_{CC}				
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA [1]	-	150	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA	-	90	160	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA	-	80	140	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA	-	65	120	Ω

Table 7: R_{ON} resistance per switch for types 74HC4051 and 74HCT4051 *…continued*

V_I = V_{IH} or V_{IL}; for test circuit see Figure 8.
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.
For 74HC4051: V_{CC} – GND or V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.
For 74HCT4051: V_{CC} – GND = 4.5 V and 5.5 V; V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta R_{ON(max)}$	maximum ON-state resistance variation between any two channels	V_{is} = V_{CC} to V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	9	-	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V		-	8	-	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V		-	6	-	Ω
T_{amb} = –40 °C to +85 °C							
$R_{ON(peak)}$	ON-state resistance (peak)	V_{is} = V_{CC} to V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	225	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	200	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	-	165	Ω
$R_{ON(rail)}$	ON-state resistance (rail)	V_{is} = V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	175	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	150	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	-	130	Ω
		V_{is} = V_{CC}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	200	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	175	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	-	150	Ω
T_{amb} = –40 °C to +125 °C							
$R_{ON(peak)}$	ON-state resistance (peak)	V_{is} = V_{CC} to V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	270	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	240	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	-	195	Ω
$R_{ON(rail)}$	ON-state resistance (rail)	V_{is} = V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	210	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	180	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	-	160	Ω
		V_{is} = V_{CC}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	240	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	210	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	-	180	Ω

Table 9: Static characteristics type 74HCT4051

Voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_{EE} = 0 V; V_I = V_{CC} or GND	-	-	0.1	µA
$I_{S(OFF)}$	switch OFF-state current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\|V_S\|$ = V_{CC} − V_{EE}; see Figure 10				
		per channel	-	-	±0.1	µA
		all channels	-	-	±0.4	µA
$I_{S(ON)}$	switch ON-state current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\|V_S\|$ = V_{CC} − V_{EE}; see Figure 11	-	-	±0.4	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{EE} = 0 V; V_{CC} = 5.5 V	-	-	8.0	µA
		V_{EE} = −5.0 V; V_{CC} = 5.0 V	-	-	16.0	µA
ΔI_{CC}	additional quiescent supply current per input pin	V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V; V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND				
	Sn input		-	50	180	µA
	$\overline{E}$ input		-	50	180	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_{EE} = 0 V; V_I = V_{CC} or GND	-	-	±1.0	µA
$I_{S(OFF)}$	switch OFF-state current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\|V_S\|$ = V_{CC} − V_{EE}; see Figure 10				
		per channel	-	-	±1.0	µA
		all channels	-	-	±4.0	µA
$I_{S(ON)}$	switch ON-state current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\|V_S\|$ = V_{CC} − V_{EE}; see Figure 11	-	-	±4.0	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{EE} = 0 V; V_{CC} = 5.5 V	-	-	80.0	µA
		V_{EE} = −5.0 V; V_{CC} = 5.0 V	-	-	160.0	µA
ΔI_{CC}	additional quiescent supply current per input pin	V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V; V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND				
	Sn input		-	-	225	µA
	$\overline{E}$ input		-	-	225	µA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_{EE} = 0 V; V_I = V_{CC} or GND	-	-	±1.0	µA

Table 9: Static characteristics type 74HCT4051 *…continued*

Voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{S(OFF)}$	switch OFF-state current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\lvert V_S\rvert$ = V_{CC} – V_{EE}; see Figure 10				
		per channel	-	-	±1.0	μA
		all channels	-	-	±4.0	μA
$I_{S(ON)}$	switch ON-state current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\lvert V_S\rvert$ = V_{CC} – V_{EE}; see Figure 11	-	-	±4.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{EE} = 0 V; V_{CC} = 5.5 V	-	-	160.0	μA
		V_{EE} = –5.0 V; V_{CC} = 5.0 V	-	-	320.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V; V_I = V_{CC} – 2.1 V; other inputs at V_{CC} or GND				
	Sn input		-	-	245	μA
	$\overline{E}$ input		-	-	245	μA

12. Dynamic characteristics

Table 10: Dynamic characteristics type 74HC4051

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF unless specified otherwise; for test circuit see Figure 14.

V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	R_L = ∞ Ω; see Figure 12				
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	14	60	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	5	12	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	4	10	ns
		V_{CC} = 4.5 V; V_{EE} = –4.5 V	-	4	8	ns
t_{PZH}, t_{PZL}	turn-ON time	R_L = 1 kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	V_{CC} = 2.0 V; V_{EE} = 0 V	-	72	345	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	29	69	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	22	-	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	21	59	ns
		V_{CC} = 4.5 V; V_{EE} = –4.5 V	-	18	51	ns
	Sn to V_{os}	V_{CC} = 2.0 V; V_{EE} = 0 V	-	66	345	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	28	69	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	20	-	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	19	59	ns
		V_{CC} = 4.5 V; V_{EE} = –4.5 V	-	16	51	ns

Table 11: Dynamic characteristics type 74HCT4051

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF and V_{CC} = 4.5 V unless specified otherwise; for test circuit see Figure 14.
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	$R_L = \infty\ \Omega$; see Figure 12					
		V_{EE} = 0 V		-	5	12	ns
		V_{EE} = –4.5 V		-	4	8	ns
t_{PZH}, t_{PZL}	turn-ON time	R_L = 1 kΩ; see Figure 13					
	$\overline{E}$ to V_{os}	V_{EE} = 0 V		-	26	55	ns
		V_{EE} = 0 V; V_{CC} = 5.0 V; C_L = 15 pF		-	22	-	ns
		V_{EE} = –4.5 V		-	16	39	ns
	Sn to V_{os}	V_{EE} = 0 V		-	28	55	ns
		V_{EE} = 0 V; V_{CC} = 5.0 V; C_L = 15 pF		-	24	-	ns
		V_{EE} = –4.5 V		-	16	39	ns
t_{PHZ}, t_{PLZ}	turn-OFF time	R_L = 1 kΩ; see Figure 13					
	$\overline{E}$ to V_{os}	V_{EE} = 0 V		-	19	45	ns
		V_{EE} = 0 V; V_{CC} = 5.0 V; C_L = 15 pF		-	16	-	ns
		V_{EE} = –4.5 V		-	16	32	ns
	Sn to V_{os}	V_{EE} = 0 V		-	23	45	ns
		V_{EE} = 0 V; V_{CC} = 5.0 V; C_L = 15 pF		-	20	-	ns
		V_{EE} = –4.5 V		-	16	32	ns
C_{PD}	power dissipation capacitance (per switch)		[1] [2]	-	25	-	pF
T_{amb} = –40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	$R_L = \infty\ \Omega$; see Figure 12					
		V_{EE} = 0 V		-	-	15	ns
		V_{EE} = –4.5 V		-	-	10	ns
t_{PZH}, t_{PZL}	turn-ON time	R_L = 1 kΩ; see Figure 13					
	$\overline{E}$ to V_{os}	V_{EE} = 0 V		-	-	69	ns
		V_{EE} = –4.5 V		-	-	49	ns
	Sn to V_{os}	V_{EE} = 0 V		-	-	69	ns
		V_{EE} = –4.5 V		-	-	49	ns
t_{PHZ}, t_{PLZ}	turn-OFF time	R_L = 1 kΩ; see Figure 13					
	$\overline{E}$ to V_{os}	V_{EE} = 0 V		-	-	56	ns
		V_{EE} = –4.5 V		-	-	40	ns
	Sn to V_{os}	V_{EE} = 0 V		-	-	56	ns
		V_{EE} = –4.5 V		-	-	40	ns
T_{amb} = –40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	$R_L = \infty\ \Omega$; see Figure 12					
		V_{EE} = 0 V		-	-	18	ns
		V_{EE} = –4.5 V		-	-	12	ns

Table 11: Dynamic characteristics type 74HCT4051 *…continued*

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF and $V_{CC} = 4.5$ V unless specified otherwise; for test circuit see Figure 14.
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PZH}, t_{PZL}	turn-ON time	$R_L = 1$ kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	$V_{EE} = 0$ V	-	-	83	ns
		$V_{EE} = -4.5$ V	-	-	59	ns
	Sn to V_{os}	$V_{EE} = 0$ V	-	-	83	ns
		$V_{EE} = -4.5$ V	-	-	59	ns
t_{PHZ}, t_{PLZ}	turn-OFF time	$R_L = 1$ kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	$V_{EE} = 0$ V	-	-	68	ns
		$V_{EE} = -4.5$ V	-	-	48	ns
	Sn to V_{os}	$V_{EE} = 0$ V	-	-	68	ns
		$V_{EE} = -4.5$ V	-	-	48	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs;
C_L = output load capacitance in pF;
C_S = switch capacitance in pF;
V_{CC} = supply voltage in V.

[2] For 74HCT4051 the condition is V_I = GND to $V_{CC} - 1.5$ V.

13. Waveforms

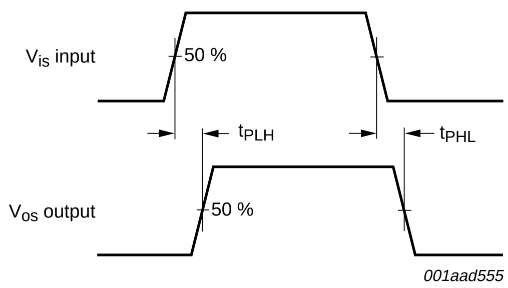


Fig 12. Input (V_{is}) to output (V_{os}) propagation delays

14. Additional dynamic characteristics

Table 14: Additional dynamic characteristics

Recommended conditions and typical values; GND = 0 V; T_{amb} = 25 °C.
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
d_{sin}	sine-wave distortion	R_L = 10 kΩ; C_L = 50 pF; see Figure 15				
		f_i = 1 kHz				
		V_{CC} = 2.25 V; V_{EE} = –2.25 V; $V_{is(p-p)}$ = 4.0 V	-	0.04	-	%
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; $V_{is(p-p)}$ = 8.0 V	-	0.02	-	%
		f_i = 10 kHz				
		V_{CC} = 2.25 V; V_{EE} = –2.25 V; $V_{is(p-p)}$ = 4.0 V	-	0.12	-	%
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; $V_{is(p-p)}$ = 8.0 V	-	0.06	-	%
$\alpha_{(ft)OFF}$	switch OFF-state signal feed-through suppression	R_L = 600 Ω; C_L = 50 pF; see Figure 16 [1]				
		V_{CC} = 2.25 V; V_{EE} = –2.25 V	-	–50	-	dB
		V_{CC} = 4.5 V; V_{EE} = –4.5 V	-	–50	-	dB
$V_{ct(p-p)}$	crosstalk voltage (peak-to-peak value)	R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; $\overline{E}$ or Sn square-wave between V_{CC} and GND; t_r = t_f = 6 ns; see Figure 17				
	between $\overline{E}$ or Sn and Yn or Z	V_{CC} = 4.5 V; V_{EE} = 0 V	-	110	-	mV
		V_{CC} = 4.5 V; V_{EE} = –4.5 V	-	220	-	mV
$f_{h(-3dB)}$	–3 dB high frequency	R_L = 50 Ω; C_L = 10 pF; see Figure 18 [2]				
		V_{CC} = 2.25 V; V_{EE} = –2.25 V	-	170	-	MHz
		V_{CC} = 4.5 V; V_{EE} = –4.5 V	-	180	-	MHz
C_S	switch capacitance					
	independent input/output Yn		-	5	-	pF
	common input/output Z		-	25	-	pF

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

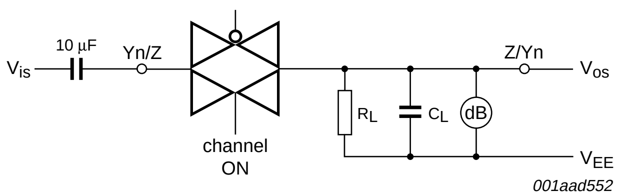
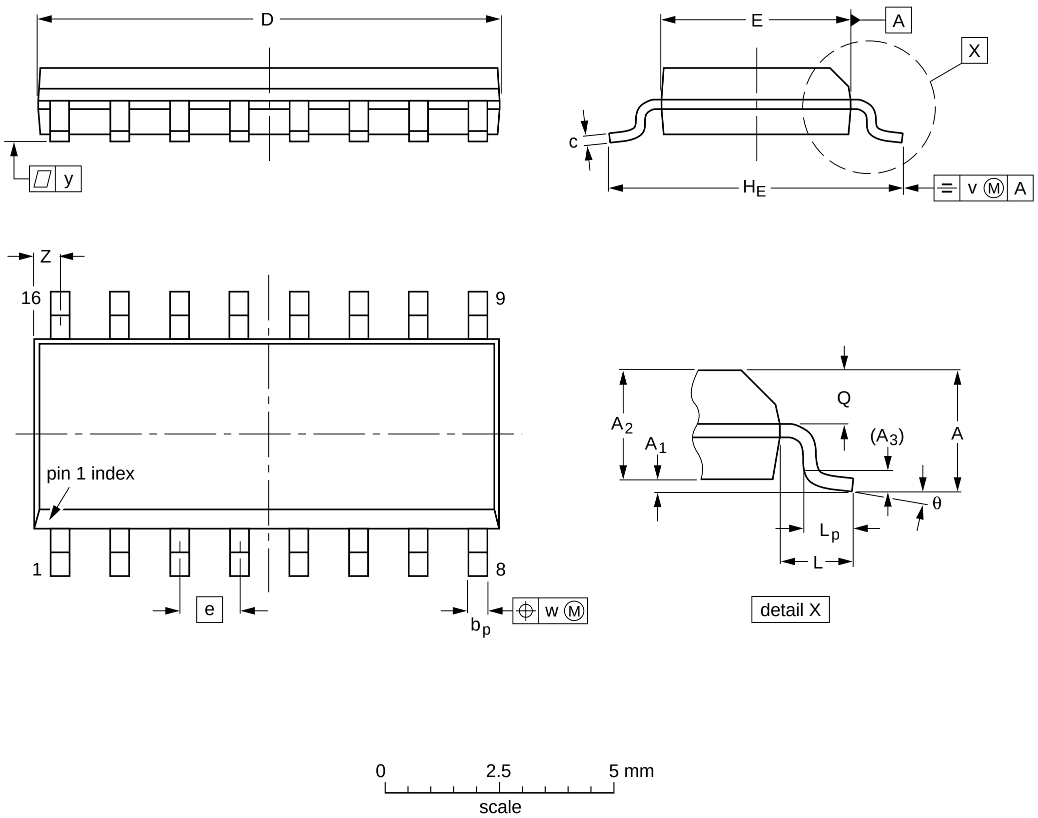


Fig 15. Test circuit for measuring sine-wave distortion

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				

Fig 20. Package outline SOT109-1 (SO16)