19-2328; Rev 2; 11/07

MAXIM

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

General Description

The MAX3372E–MAX3379E and MAX3390E–MAX3393E ±15kV ESD-protected level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. A low-voltage logic signal present on the V_L side of the device appears as a high-voltage logic signal on the V_{CC} side of the device, and vice-versa. The MAX3374E/MAX3375E/MAX3376E/MAX3379E and MAX3390E–MAX3393E unidirectional level translators level shift data in one direction ($V_L \rightarrow V_{CC}$ or $V_{CC} \rightarrow V_L$) on any single data line. The MAX3372E/MAX3373E and MAX3377E/MAX3378E bidirectional level translators utilize a transmission-gate-based design (Figure 2) to allow data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line. The MAX3372E–MAX3379E and MAX3390E–MAX3393E accept V_L from +1.2V to +5.5V and V_{CC} from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

All devices in the MAX3372E–MAX3379E, MAX3390E–MAX3393E family feature a three-state output mode that reduces supply current to less than 1µA, thermal short-circuit protection, and ±15kV ESD protection on the V_{CC} side for greater protection in applications that route signals externally. The MAX3372E/MAX3377E operate at a guaranteed data rate of 230kbps. Slew-rate limiting reduces EMI emissions in all 230kbps devices. The MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E operate at a guaranteed data rate of 8Mbps over the entire specified operating voltage range. Within specific voltage domains, higher data rates are possible. (See the *Timing Characteristics* table.)

The MAX3372E–MAX3376E are dual level shifters available in 3 x 3 UCSP™, 8-pin TDFN, and 8-pin SOT23-8 packages. The MAX3377E/MAX3378E/MAX3379E and MAX3390E–MAX3393E are quad level shifters available in 3 x 4 UCSP, 14-pin TDFN, and 14-pin TSSOP packages.

Applications

SPI™, MICROWIRE™, and I²C Level Translation
Low-Voltage ASIC Level Translation
Smart Card Readers
Cell-Phone Cradles
Portable POS Systems
Portable Communication Devices
Low-Cost Serial Interfaces
Cell Phones
GPS
Telecommunications Equipment

Features

- **Guaranteed Data Rate Options**
  - **230kbps**
  - **8Mbps (+1.2V ≤ V_L ≤ V_{CC} ≤ +5.5V)**
  - **10Mbps (+1.2V ≤ V_L ≤ V_{CC} ≤ +3.3V)**
  - **16Mbps (+1.8V ≤ V_L ≤ V_{CC} ≤ +2.5V and +2.5V ≤ V_L ≤ V_{CC} ≤ +3.3V)**
- **Bidirectional Level Translation (MAX3372E/MAX3373E and MAX3377E/MAX3378E)**
- **Operation Down to +1.2V on V_L**
- **±15kV ESD Protection on I/O V_{CC} Lines**
- **Ultra-Low 1µA Supply Current in Three-State Output Mode**
- **Low-Quiescent Current (130µA typ)**
- **UCSP, TDFN, SOT23, and TSSOP Packages**
- **Thermal Short-Circuit Protection**

Ordering Information

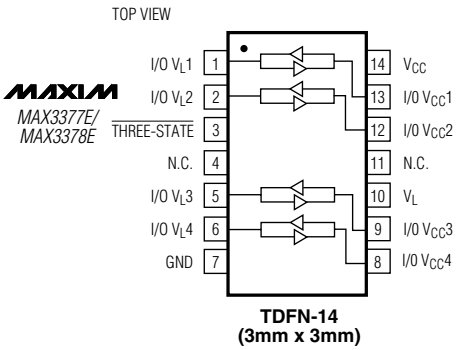
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3372EEKA+T	-40°C to +85°C	8 SOT23	K8S-3

+Denotes a lead-free package.
T = Tape and reel.

Ordering Information continued at end of data sheet.
Selector Guide appears at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.
SPI is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Pin Configurations



TDFN-14
(3mm x 3mm)

Pin Configurations continued at end of data sheet.

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC} .....-0.3V to +6V
I/O $V_{CC\_}$ .....-0.3V to (V_{CC} + 0.3V)
I/O $V_{L\_}$ .....-0.3V to (V_L + 0.3V)
$\overline{\text{THREE-STATE}}$ .....-0.3V to (V_L + 0.3V)
Short-Circuit Duration I/O V_L, I/O V_{CC} to GND.....Continuous
Short-Circuit Duration I/O V_L or I/O V_{CC} to GND
Driven from 40mA Source
(except MAX3372E and MAX3377E) .....Continuous

Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.9mW/°C above +70°C).....714mW
8-Pin TDFN (derate 18.2mW/°C above +70°C) 1455mW
3 x 3 UCSP (derate 4.7mW/°C above +70°C) 379mW
3 x 4 UCSP (derate 6.5mW/°C above +70°C) 579mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
14-Pin TDFN (derate 18.2mW/°C above +70°C) 1454mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to (V_{CC} + 0.3V), GND = 0, I/O $V_{L\_}$ and I/O $V_{CC\_}$ unconnected, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_L Supply Range	V_L		1.2		5.5	V
V_{CC} Supply Range	V_{CC}		1.65		5.50	V
Supply Current from V_{CC}	I_{QVCC}			130	300	µA
Supply Current from V_L	I_{QVL}			16	100	µA
V_{CC} Three-State Output Mode Supply Current	$I_{THREE-STATE-VCC}$	T_A = +25°C, $\overline{\text{THREE-STATE}}$ = GND		0.03	1	µA
V_L Three-State Output Mode Supply Current	$I_{THREE-STATE-VL}$	T_A = +25°C, $\overline{\text{THREE-STATE}}$ = GND		0.03	1	µA
Three-State Output Mode Leakage Current I/O $V_{L\_}$ and I/O $V_{CC\_}$	$I_{THREE-STATE-LKG}$	T_A = +25°C, $\overline{\text{THREE-STATE}}$ = GND		0.02	1	µA
$\overline{\text{THREE-STATE}}$ Pin Input Leakage		T_A = +25°C		0.02	1	µA
ESD PROTECTION						
I/O V_{CC} (Note 3)		IEC 1000-4-2 Air-Gap Discharge		±8		kV
		IEC 1000-4-2 Contact Discharge		±8		
		Human Body Model		±15		
LOGIC-LEVEL THRESHOLDS (MAX3372E/MAX3377E)						
I/O $V_{L\_}$ Input-Voltage High	V_{IHL}		V_L - 0.2			V
I/O $V_{L\_}$ Input-Voltage Low	V_{ILL}				0.15	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to (V_{CC} + 0.3V), GND = 0, I/O $V_{L\_}$ and I/O $V_{CC\_}$ unconnected, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Input-Voltage High	V_{IHC}		V_{CC} - 0.4			V
I/O $V_{CC\_}$ Input-Voltage Low	V_{ILC}				0.15	V
I/O $V_{L\_}$ Output-Voltage High	V_{OHL}	I/O $V_{L\_}$ source current = 20µA, I/O $V_{CC\_} \geq V_{CC}$ - 0.4V	0.67 × V_L			V
I/O $V_{L\_}$ Output-Voltage Low	V_{OLL}	I/O $V_{L\_}$ sink current = 20µA, I/O $V_{CC\_} \leq$ 0.15V			0.4	V
I/O $V_{CC\_}$ Output-Voltage High	V_{OHC}	I/O $V_{CC\_}$ source current = 20µA, I/O $V_{L\_} \geq V_L$ - 0.2V	0.67 × V_{CC}			V
I/O $V_{CC\_}$ Output-Voltage Low	V_{OLC}	I/O $V_{CC\_}$ sink current = 20µA, I/O $V_{L\_} \leq$ 0.15V			0.4	V
$\overline{\text{THREE-STATE}}$ Input-Voltage High	$V_{IL\text{-}\overline{\text{THREE-STATE}}}$		V_L - 0.2			V
$\overline{\text{THREE-STATE}}$ Input-Voltage Low	$V_{IL\text{-}\overline{\text{THREE-STATE}}}$				0.15	V
LOGIC-LEVEL THRESHOLDS (MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E)						
I/O $V_{L\_}$ Input-Voltage High	V_{IHL}		V_L - 0.2			V
I/O $V_{L\_}$ Input-Voltage Low	V_{ILL}				0.15	V
I/O $V_{CC\_}$ Input-Voltage High	V_{IHC}		V_{CC} - 0.4			V
I/O $V_{CC\_}$ Input-Voltage Low	V_{ILC}				0.15	V
I/O $V_{L\_}$ Output-Voltage High	V_{OHL}	I/O $V_{L\_}$ source current = 20µA, I/O $V_{CC\_} \geq V_{CC}$ - 0.4V	0.67 × V_L			V
I/O $V_{L\_}$ Output-Voltage Low	V_{OLL}	I/O $V_{L\_}$ sink current = 1mA, I/O $V_{CC\_} \leq$ 0.15V			0.4	V
I/O $V_{CC\_}$ Output-Voltage High	V_{OHC}	I/O $V_{CC\_}$ source current = 20µA, I/O $V_{L\_} \geq V_L$ - 0.2V	0.67 × V_{CC}			V
I/O $V_{CC\_}$ Output-Voltage Low	V_{OLC}	I/O $V_{CC\_}$ sink current = 1mA, I/O $V_{L\_} \leq$ 0.15V			0.4	V
$\overline{\text{THREE-STATE}}$ Input-Voltage High	$V_{IH\text{-}\overline{\text{THREE-STATE}}}$		V_L - 0.2			V
$\overline{\text{THREE-STATE}}$ Input-Voltage Low	$V_{IL\text{-}\overline{\text{THREE-STATE}}}$				0.15	V

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to (V_{CC} + 0.3V), GND = 0, R_{LOAD} = 1MΩ, I/O test signal of Figure 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MAX3372E/MAX3377E (C_{LOAD} = 50pF)							
I/O $V_{CC\_}$ Rise Time (Note 4)	t_{RVCC}				1100		ns
I/O $V_{CC\_}$ Fall Time (Note 5)	t_{FVCC}				1000		ns
I/O $V_{L\_}$ Rise Time (Note 4)	t_{RVL}				600		ns
I/O $V_{L\_}$ Fall Time (Note 5)	t_{FVL}				1100		ns
Propagation Delay	I/O_{VL-VCC}	Driving I/O $V_{L\_}$				1.6	µs
	I/O_{VCC-VL}	Driving I/O $V_{CC\_}$				1.6	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded				500	ns
Maximum Data Rate		C_L = 25pF		230			kbps
MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E (C_{LOAD} = 15pF, Driver Output Impedance ≤ 50Ω)							
+1.2V ≤ V_L ≤ V_{CC} ≤ +5.5V							
I/O $V_{CC\_}$ Rise Time (Note 4)	t_{RVCC}				7	25	ns
		Open-drain driving			170	400	
I/O $V_{CC\_}$ Fall Time (Note 5)	t_{FVCC}				6	37	ns
		Open-drain driving			20	50	
I/O $V_{L\_}$ Rise Time (Note 4)	t_{RVL}				8	30	ns
		Open-drain driving			180	400	
I/O $V_{L\_}$ Fall Time (Note 5)	t_{LFV}				3	30	ns
		Open-drain driving			30	60	
Propagation Delay	I/O_{VL-VCC}	Driving I/O $V_{L\_}$			5	30	ns
			Open-drain driving		210	1000	
	I/O_{VCC-VL}	Driving I/O $V_{CC\_}$			4	30	
			Open-drain driving		190	1000	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded				20	ns
			Open-drain driving			50	
Maximum Data Rate				8			Mbps
		Open-drain driving		500			kbps

TIMING CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to (V_{CC} + 0.3V), GND = 0, R_{LOAD} = 1MΩ, I/O test signal of Figure 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
+1.2V ≤ V_L ≤ V_{CC} ≤ +3.3V						
I/O $V_{CC\_}$ Rise Time (Note 4)	t_{RVCC}				25	ns
I/O $V_{CC\_}$ Fall Time (Note 5)	t_{FVCC}				30	ns
I/O $V_{L\_}$ Rise Time (Note 4)	t_{RVL}				30	ns
I/O $V_{L\_}$ Fall Time (Note 5)	t_{FVL}				30	ns
Propagation Delay	I/O_{VL-VCC}	Driving I/O $V_{L\_}$			20	ns
	I/O_{VCC-VL}	Driving I/O $V_{CC\_}$			20	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded			10	ns
Maximum Data Rate			10			Mbps
+2.5V ≤ V_L ≤ V_{CC} ≤ +3.3V						
I/O $V_{CC\_}$ Rise Time (Note 4)	t_{RVCC}				15	ns
I/O $V_{CC\_}$ Fall Time (Note 5)	t_{FVCC}				15	ns
I/O $V_{L\_}$ Rise Time (Note 4)	t_{RVL}				15	ns
I/O $V_{L\_}$ Fall Time (Note 5)	t_{FVL}				15	ns
Propagation Delay	I/O_{VL-VCC}	Driving I/O $V_{L\_}$			15	ns
	I/O_{VCC-VL}	Driving I/O $V_{CC\_}$			15	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded			10	ns
Maximum Data Rate			16			Mbps
+1.8V ≤ V_L ≤ V_{CC} ≤ +2.5V						
I/O $V_{CC\_}$ Rise Time (Note 4)	t_{RVCC}				15	ns
I/O $V_{CC\_}$ Fall Time (Note 5)	t_{FVCC}				15	ns
I/O $V_{L\_}$ Rise Time (Note 4)	t_{RVL}				15	ns
I/O $V_{L\_}$ Fall Time (Note 5)	t_{FVL}				15	ns
Propagation Delay	I/O_{VL-VCC}	Driving I/O $V_{L\_}$			15	ns
	I/O_{VCC-VL}	Driving I/O $V_{CC\_}$			15	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded			10	ns
Maximum Data Rate			16			Mbps

Note 1: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 2: For normal operation, ensure V_L < (V_{CC} + 0.3V). During power-up, V_L > (V_{CC} + 0.3V) will not damage the device.

Note 3: To ensure maximum ESD protection, place a 1µF capacitor between V_{CC} and GND. See *Applications Circuits*.

Note 4: 10% to 90%

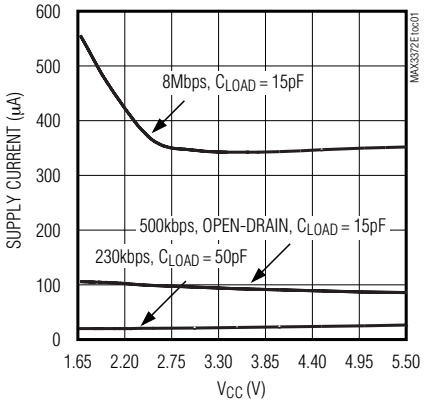
Note 5: 90% to 10%

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

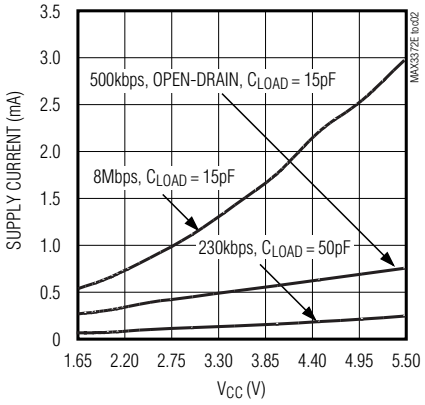
Typical Operating Characteristics

(R_{LOAD} = 1MΩ, T_A = +25°C, unless otherwise noted. All 230kbps TOCs apply to MAX3372E/MAX3377E only. All 8Mbps and 500kbps TOCs apply to MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E only.)

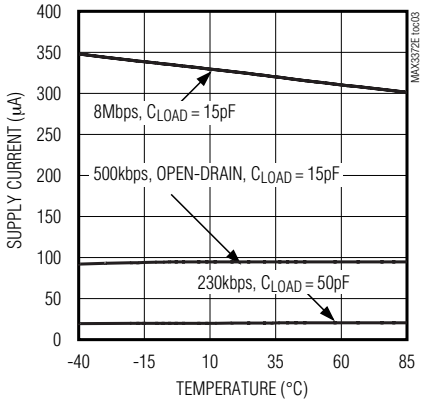
V_L SUPPLY CURRENT vs. SUPPLY VOLTAGE (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V)



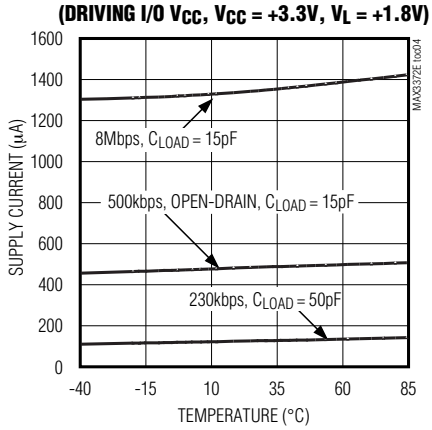
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V)



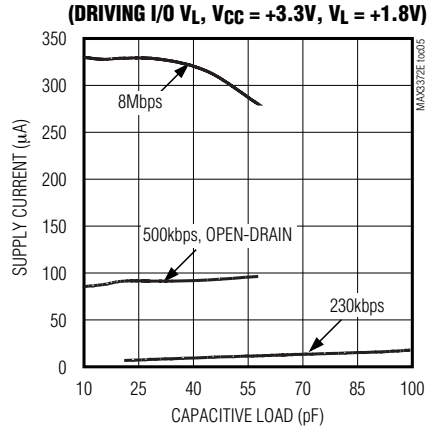
V_L SUPPLY CURRENT vs. TEMPERATURE (DRIVING I/O V_{CC}, V_{CC} = +3.3V, V_L = +1.8V)



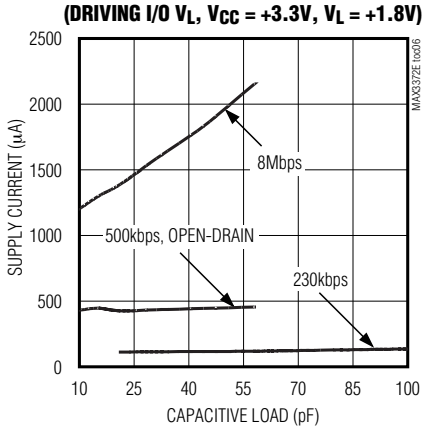
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (DRIVING I/O V_{CC}, V_{CC} = +3.3V, V_L = +1.8V)



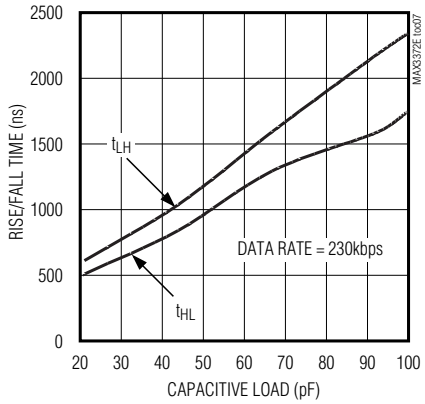
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V)



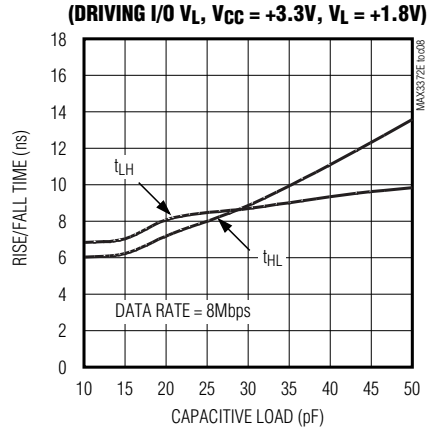
V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V)



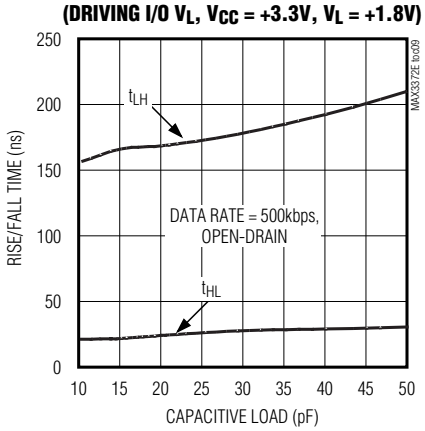
RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V)



RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V)



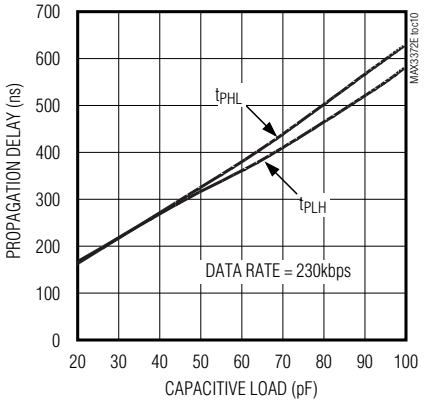
RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V)



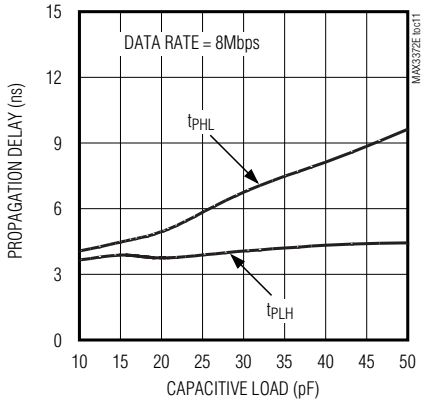
Typical Operating Characteristics (continued)

(R_{LOAD} = 1MΩ, T_A = +25°C, unless otherwise noted. All 230kbps TOCs apply to MAX3372E/MAX3377E only. All 8Mbps and 500kbps TOCs apply to MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E only.)

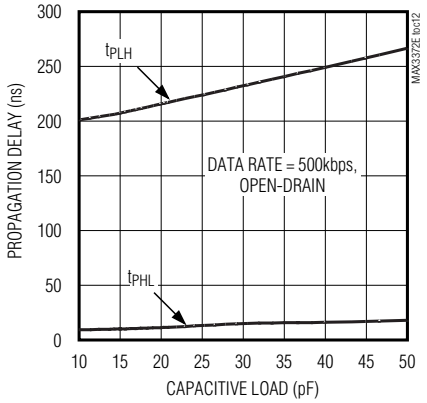
PROPAGATION DELAY vs. CAPACITIVE LOAD (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V)



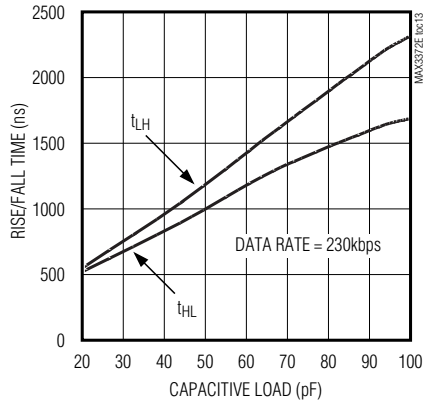
PROPAGATION DELAY vs. CAPACITIVE LOAD (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V)



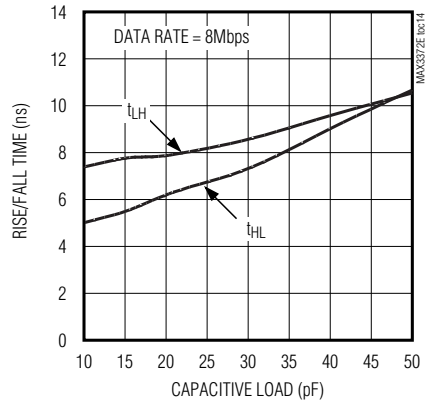
PROPAGATION DELAY vs. CAPACITIVE LOAD (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V)



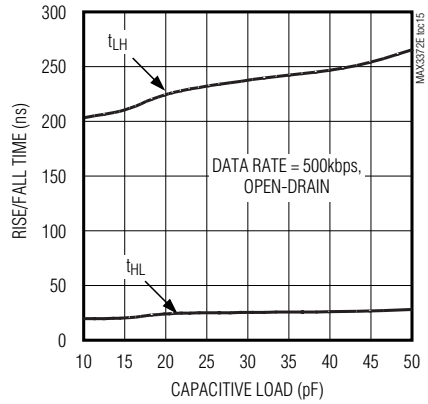
RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_L, V_{CC} = +2.5V, V_L = +1.8V)



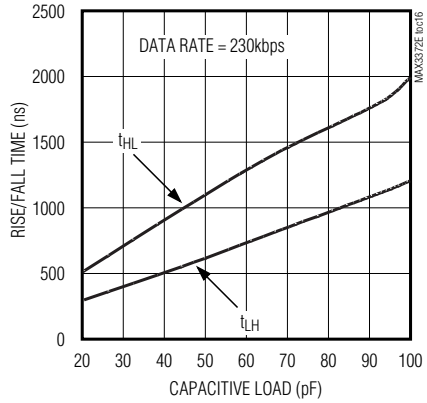
RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_L, V_{CC} = +2.5V, V_L = +1.8V)



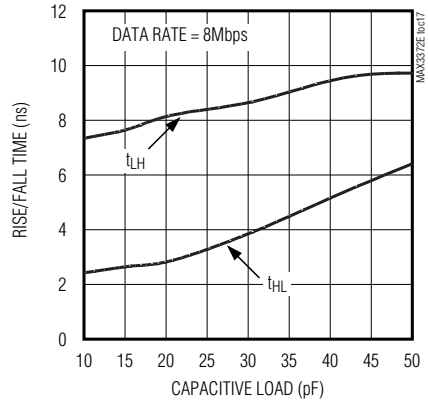
RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_{CC}, V_{CC} = +2.5V, V_L = +1.8V)



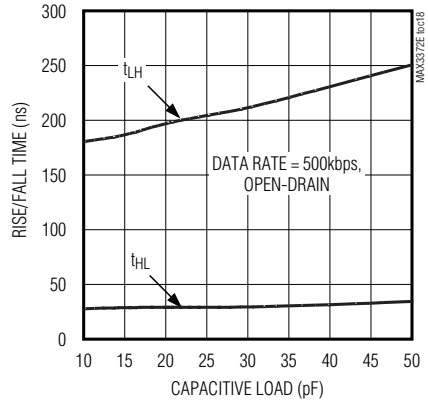
RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_{CC}, V_{CC} = +3.3V, V_L = +1.8V)



RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_{CC}, V_{CC} = +3.3V, V_L = +1.8V)



RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_{CC}, V_{CC} = +3.3V, V_L = +1.8V)

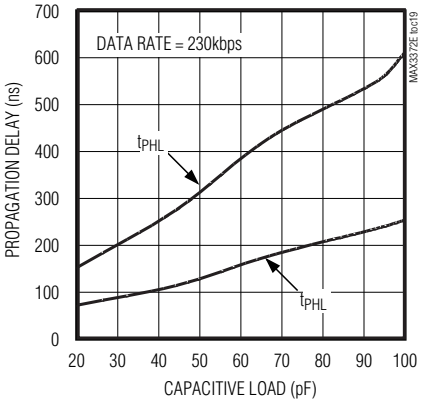


±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

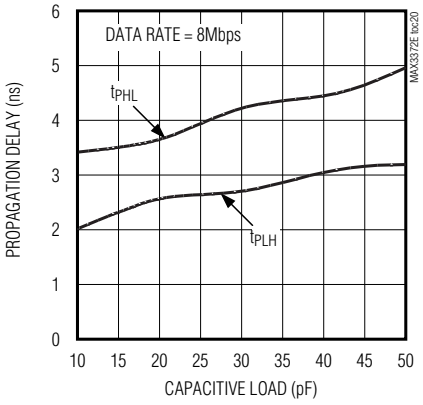
Typical Operating Characteristics (continued)

(R_{LOAD} = 1MΩ, T_A = +25°C, unless otherwise noted. All 230kbps TOCs apply to MAX3372E/MAX3377E only. All 8Mbps and 500kbps TOCs apply to MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E only.)

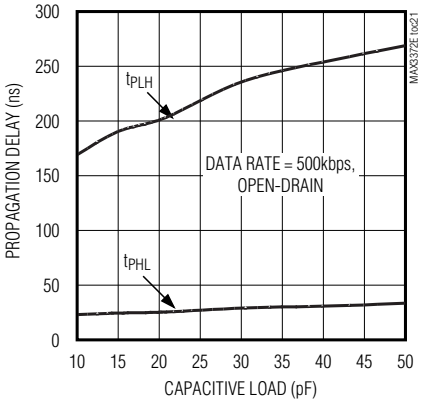
PROPAGATION DELAY vs. CAPACITIVE LOAD (DRIVING I/O V_{CC}, V_{CC} = +3.3V, V_L = +1.8V)



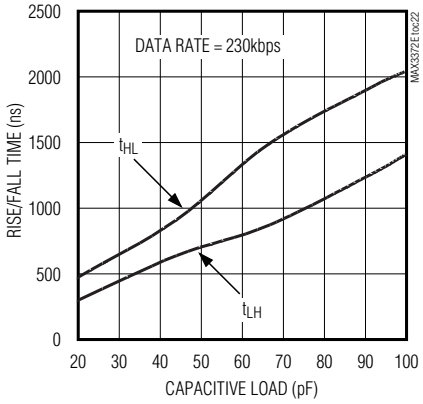
PROPAGATION DELAY vs. CAPACITIVE LOAD (DRIVING I/O V_{CC}, V_{CC} = +3.3V, V_L = +1.8V)



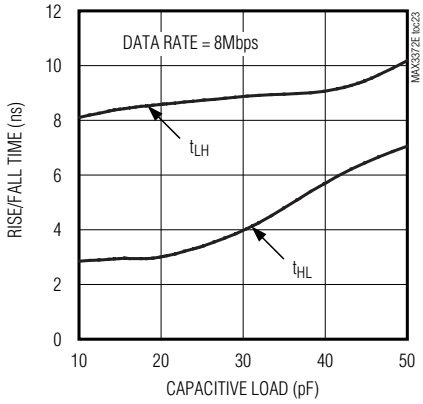
PROPAGATION DELAY vs. CAPACITIVE LOAD (DRIVING I/O V_{CC}, V_{CC} = +3.3V, V_L = +1.8V)



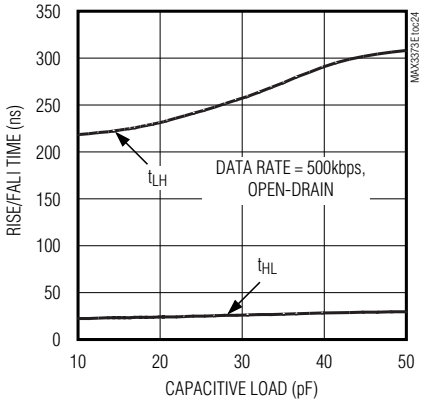
RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_{CC}, V_{CC} = +2.5V, V_L = +1.8V)



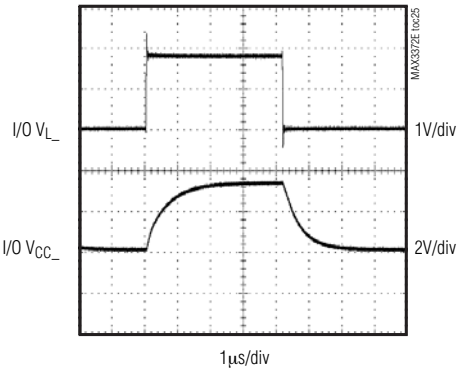
RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_{CC}, V_{CC} = +2.5V, V_L = +1.8V)



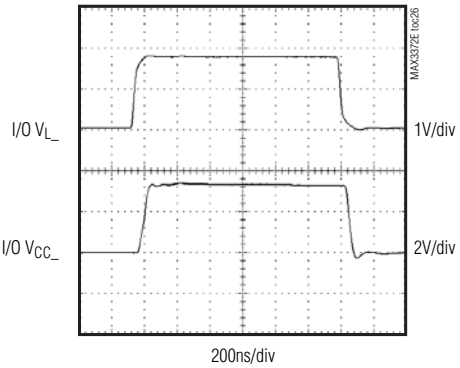
RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING I/O V_{CC}, V_{CC} = +2.5V, V_L = +1.8V)



RAIL-TO-RAIL DRIVING (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V, C_{LOAD} = 50pF, DATA RATE = 230kbps)



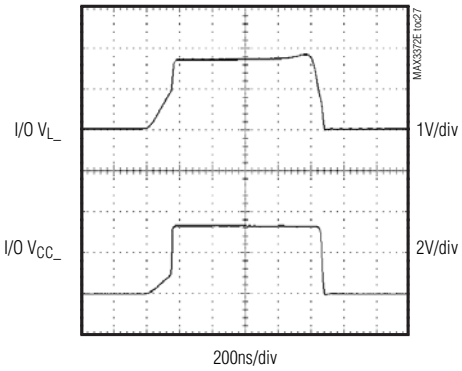
RAIL-TO-RAIL DRIVING (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V, C_{LOAD} = 15pF, DATA RATE = 8Mbps)



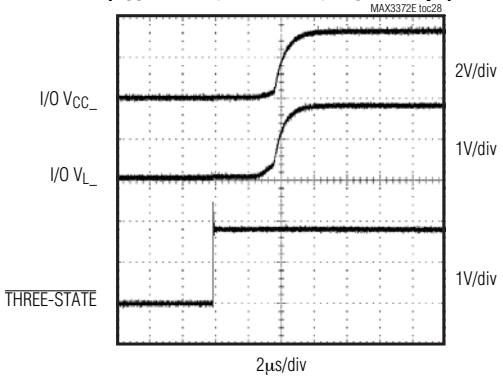
Typical Operating Characteristics (continued)

(R_{LOAD} = 1MΩ, T_A = +25°C, unless otherwise noted. All 230kbps TOCs apply to MAX3372E/MAX3377E only. All 8Mbps and 500kbps TOCs apply to MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E only.)

OPEN-DRAIN DRIVING (DRIVING I/O V_L, V_{CC} = +3.3V, V_L = +1.8V, C_{LOAD} = 15pF, DATA RATE = 500kbps)



EXITING THREE-STATE OUTPUT MODE (V_{CC} = +3.3V, V_L = +1.8V, C_{LOAD} = 50pF)



Pin Description

PIN						NAME	FUNCTION
3 x 4 UCSP	TSSOP	SOT23-8	3 x 3 UCSP	TDFN 8	TDFN 14		
A1	2	5	C2	6	1	I/O V_L1	Input/Output 1. Referenced to V_L. (Note 6)
A2	3	4	C3	8	2	I/O V_L2	Input/Output 2. Referenced to V_L. (Note 6)
A3	4	—	—	—	5	I/O V_L3	Input/Output 3. Referenced to V_L. (Note 6)
A4	5	—	—	—	6	I/O V_L4	Input/Output 4. Referenced to V_L. (Note 6)
B1	14	7	A1	4	14	V_{CC}	V_{CC} Input Voltage +1.65V ≤ V_{CC} ≤ +5.5V.
B2	1	3	C1	7	10	V_L	Logic Input Voltage +1.2V ≤ V_L ≤ (V_{CC} + 0.3V)
B3	8	6	B1	5	3	$\overline{\text{THREE-STATE}}$	Three-State Output Mode Enable. Pull $\overline{\text{THREE-STATE}}$ low to place device in three-state output mode. I/O $V_{CC\_}$ and I/O $V_{L\_}$ are high impedance in three-state output mode. **Note:** Logic referenced to V_L (for logic thresholds see the *Electrical Characteristics* table).
B4	7	2	B3	2	7	GND	Ground
C1	13	8	A2	3	13	I/O V_{CC}1	Input/Output 1. Referenced to V_{CC}. (Note 6)
C2	12	1	A3	1	12	I/O V_{CC}2	Input/Output 2. Referenced to V_{CC}. (Note 6)
C3	11	—	—	—	9	I/O V_{CC}3	Input/Output 3. Referenced to V_{CC}. (Note 6)
C4	10	—	—	—	8	I/O V_{CC}4	Input/Output 4. Referenced to V_{CC}. (Note 6)
—	6, 9	—	B2	—	4, 11	N.C.	No Connection. Not internally connected.
—	—	—	—	EP	EP	EP	Exposed Pad. Connect to ground.

Note 6: For unidirectional devices (MAX3374E/MAX3375E/MAX3376E/MAX3379E and MAX3390E–MAX3393E) see the *Pin Configurations* for input/output configurations.

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

Detailed Description

The MAX3372E–MAX3379E and MAX3390E–MAX3393E ESD-protected level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. A low-voltage logic signal present on the V_L side of the device appears as a high-voltage logic signal on the V_{CC} side of the device, and vice-versa. The MAX3374E/MAX3375E/MAX3376E/MAX3379E and MAX3390E–MAX3393E unidirectional level translators level shift data in one direction ($V_L \rightarrow V_{CC}$ or $V_{CC} \rightarrow V_L$) on any single data line. The MAX3372E/MAX3373E and MAX3377E/MAX3378E bidirectional level translators utilize a transmission-gate-based design (see Figure 2) to allow data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line. The MAX3372E–MAX3379E and MAX3390E–MAX3393E accept V_L from +1.2V to +5.5V and V_{CC} from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

All devices in the MAX3372E–MAX3379E, MAX3390E–MAX3393E family feature a three-state output mode that reduces supply current to less than 1µA, thermal short-circuit protection, and ±15kV ESD protection on the V_{CC} side for greater protection in applications that route signals externally. The MAX3372E/MAX3377E operate at a guaranteed data rate of 230kbps. Slew-rate limiting reduces EMI emissions in all 230kbps devices. The MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E operate at a guaranteed data rate of 8Mbps over the entire specified operating voltage range. Within specific voltage domains, higher data rates are possible. (See the *Timing Characteristics* table.)

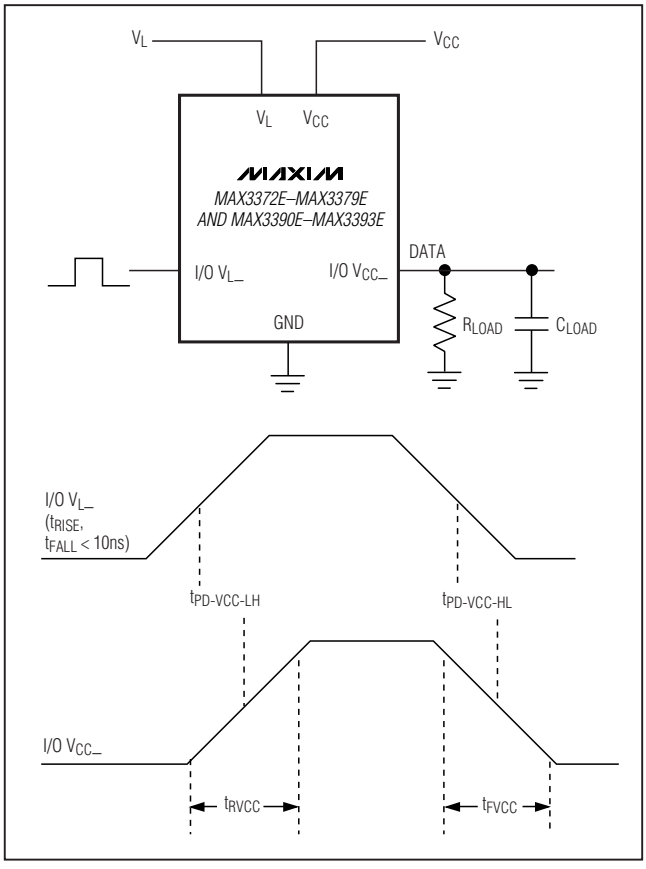


Figure 1a. Rail-to-Rail Driving I/O V_L

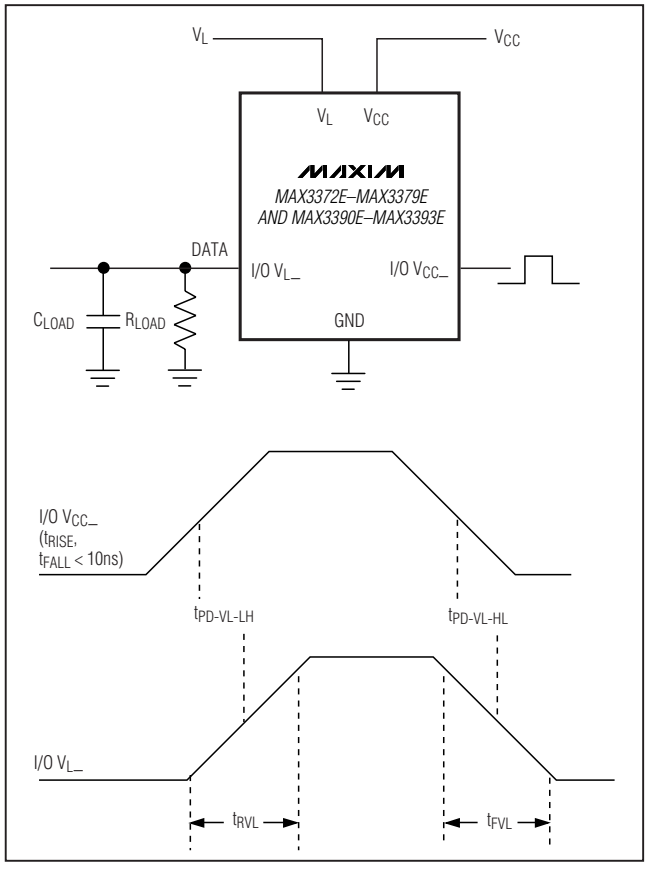


Figure 1b. Rail-to-Rail Driving I/O V_{CC}

Level Translation

For proper operation ensure that +1.65V ≤ V_{CC} ≤ +5.5V, +1.2V ≤ V_L ≤ +5.5V, and V_L ≤ (V_{CC} + 0.3V). During power-up sequencing, V_L ≥ (V_{CC} + 0.3V) will not damage the device. During power-supply sequencing, when V_{CC} is floating and V_L is powering up, a current may be sourced, yet the device will not latch up. The speed-up circuitry limits the maximum data rate for devices in the MAX3372E–MAX3379E, MAX3390E–MAX3393E family to 16Mbps. The maximum data rate also depends heavily on the load capacitance (see the *Typical Operating Characteristics*), output impedance of the driver, and the operational voltage range (see the *Timing Characteristics* table).

Speed-Up Circuitry

The MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E feature a one-shot generator that decreases the rise time of the output. When triggered, MOSFETs PU1 and PU2 turn on for a short time to pull up I/O $V_{L\_}$ and I/O $V_{CC\_}$ to their respective supplies (see Figure 2b). This greatly reduces the rise time and propagation delay for the low-to-high transition. The scope photo of Rail-to-Rail Driving for 8Mbps Operation in the *Typical Operating Characteristics* shows the speed-up circuitry in operation.

Rise-Time Accelerators

The MAX3373E–MAX3376E/MAX3378E/MAX3379E and the MAX3390E–MAX3393E have internal rise-time accelerators allowing operation up to 16Mbps. The rise-time accelerators are present on both sides of the device and act to speed up the rise time of the input and output of the device, regardless of the direction of the data. The triggering mechanism for these accelerators is both level and edge sensitive. To prevent false triggering of the rise-time accelerators, signal fall times of less than 20ns/V are recommended for both the inputs and outputs of the device. Under less noisy conditions, longer signal fall times may be acceptable.

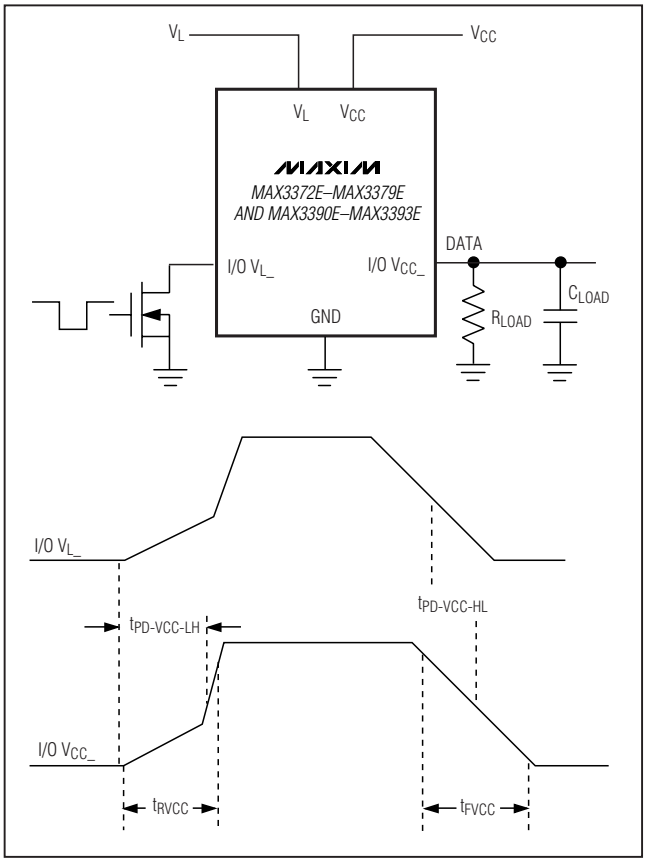


Figure 1c. Open-Drain Driving I/O V_{CC}

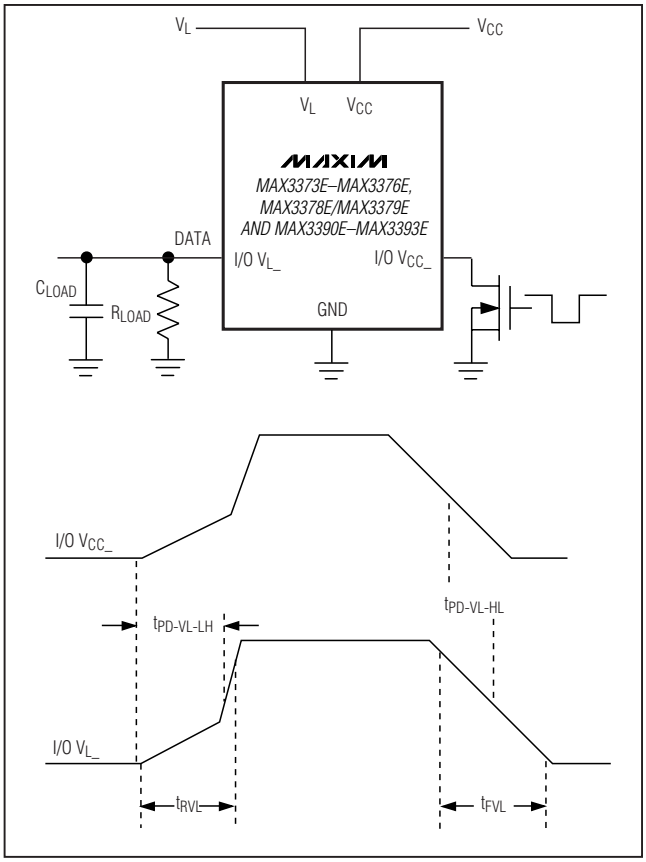


Figure 1d. Open-Drain Driving I/O V_L

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

Three-State Output Mode

Pull $\overline{\text{THREE-STATE}}$ low to place the MAX3372E–MAX3379E and MAX3390E–MAX3393E in three-state output mode. Connect $\overline{\text{THREE-STATE}}$ to V_L (logic-high) for normal operation. Activating the three-state output mode disconnects the internal 10kΩ pullup resistors on the I/O V_{CC} and I/O V_L lines. This forces the I/O lines to a high-impedance state, and decreases the supply current to less than 1µA. The high-impedance I/O lines in three-state output mode allow for use in a multidrop network. When in three-state output mode, do not allow the voltage at I/O $V_{L\_}$ to exceed (V_L + 0.3V), or the voltage at I/O $V_{CC\_}$ to exceed (V_{CC} + 0.3V).

Thermal Short-Circuit Protection

Thermal overload detection protects the MAX3372E–MAX3379E and MAX3390E–MAX3393E from short-circuit fault conditions. In the event of a short-circuit fault, when the junction temperature (T_J) reaches +152°C, a thermal sensor signals the three-state output mode logic to force the device into three-state output mode. When T_J has cooled to +142°C, normal operation resumes.

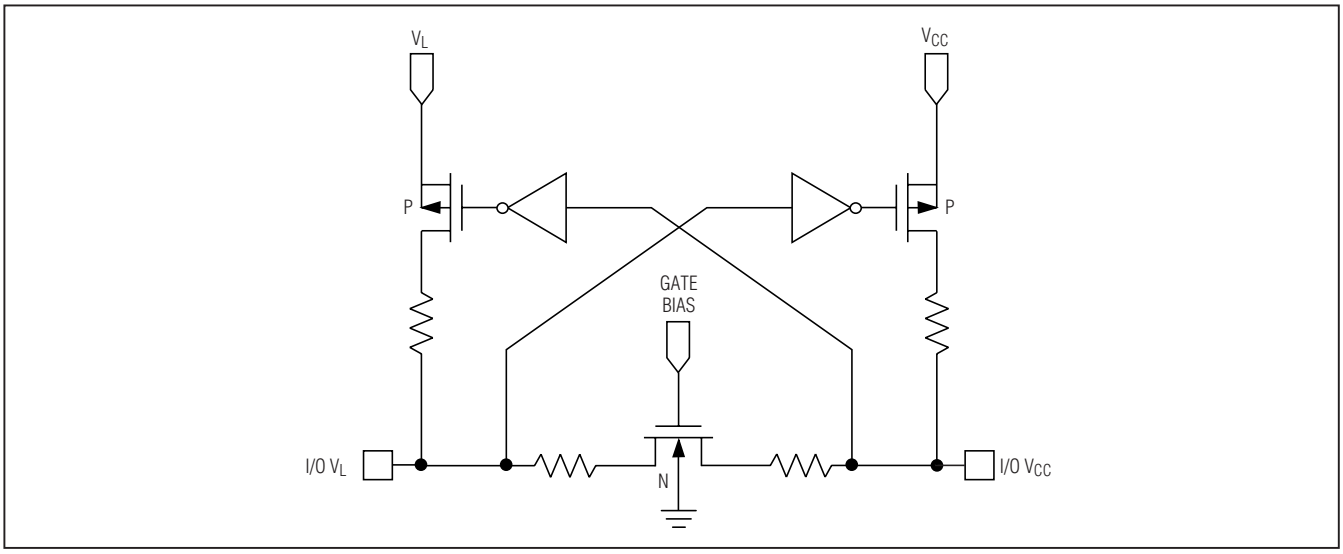


Figure 2a. Functional Diagram, MAX3372E/MAX3377E (1 I/O line)

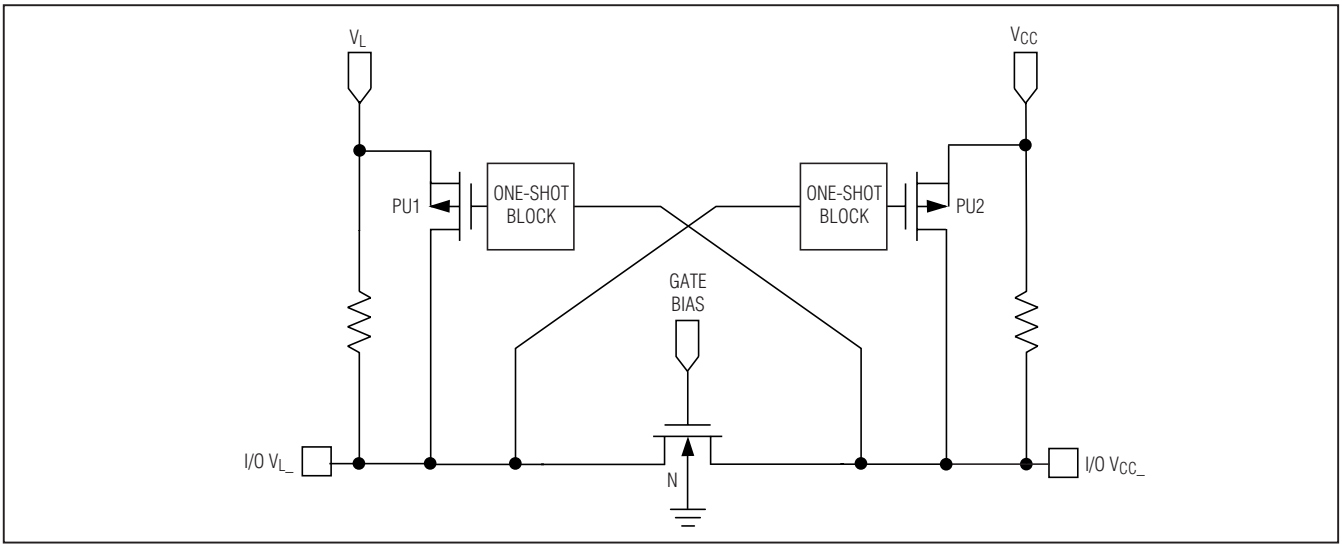


Figure 2b. Functional Diagram, MAX3373E/MAX3378E (1 I/O line)

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The I/O V_{CC} lines have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, three-state output mode, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways. The I/O V_{CC} lines of this product family are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±8kV using the Contact Discharge method specified in IEC 1000-4-2
3) ±10kV using IEC 1000-4-2's Air-Gap Discharge method

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 3a shows the Human Body Model and Figure 3b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3372E–MAX3379E and MAX3390E–MAX3393E help to design equipment that meets Level 3 of IEC 1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 4a shows the IEC 1000-4-2 model, and Figure 4b shows the current waveform for the ±8kV, IEC 1000-4-2, Level 4, ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just inputs and outputs. Therefore, after PCB assembly, the Machine Model is less relevant to I/O ports.

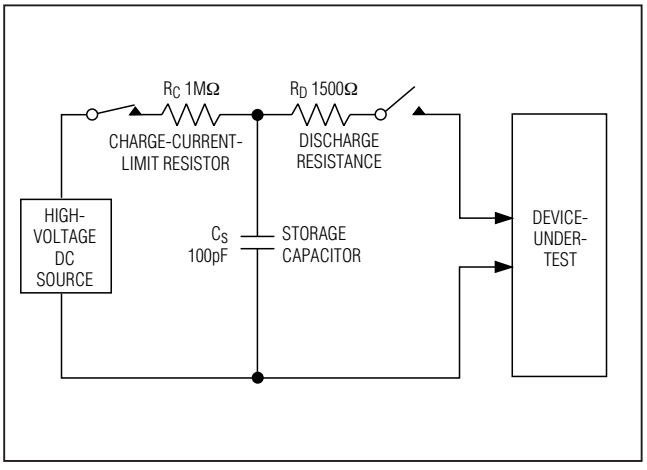


Figure 3a. Human Body ESD Test Model

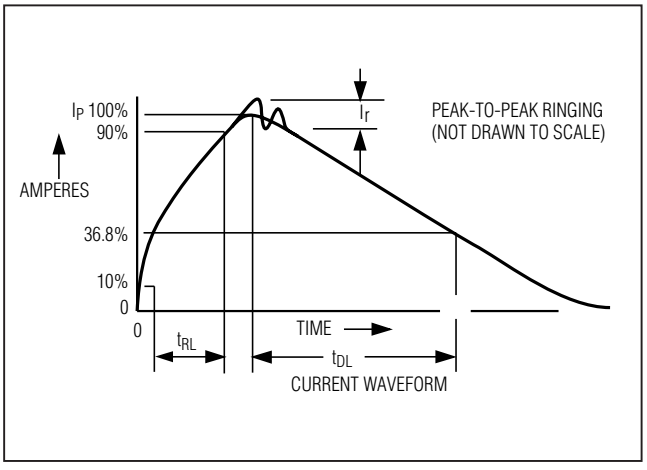


Figure 3b. Human Body Current Waveform

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

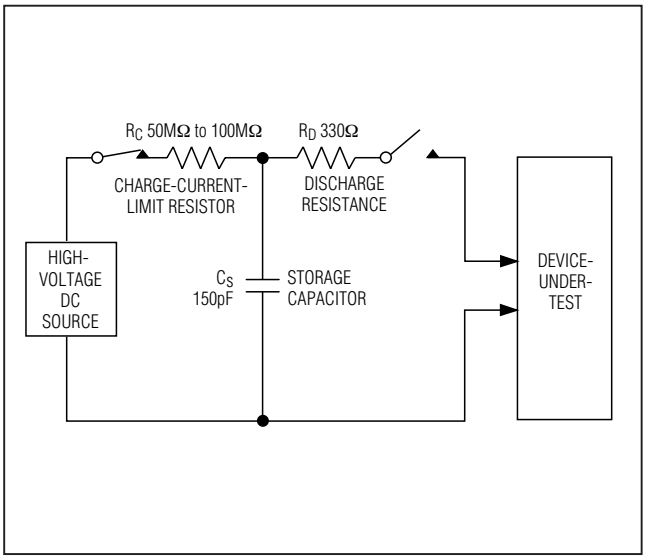


Figure 4a. IEC 1000-4-2 ESD Test Model

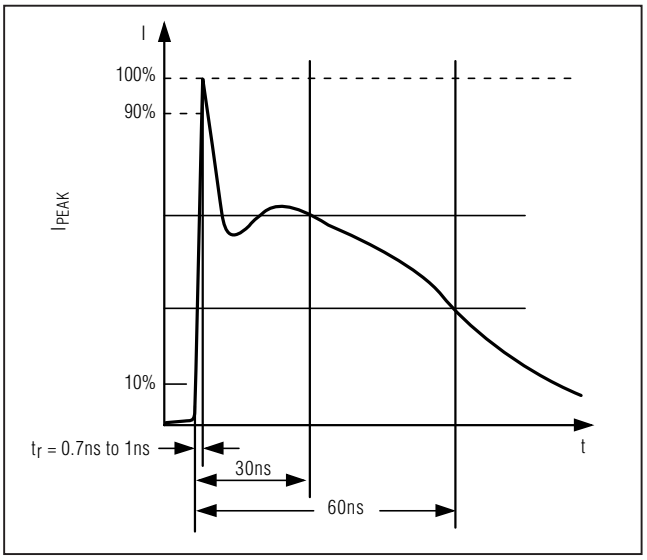


Figure 4b. IEC 1000-4-2 ESD Generator Current Waveform

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of transmitting incorrect data, bypass V_L and V_{CC} to ground with a 0.1µF capacitor. See the *Typical Operating Circuit.* To ensure full ±15kV ESD protection, bypass V_{CC} to ground with a 1µF capacitor. Place all capacitors as close to the power-supply inputs as possible.

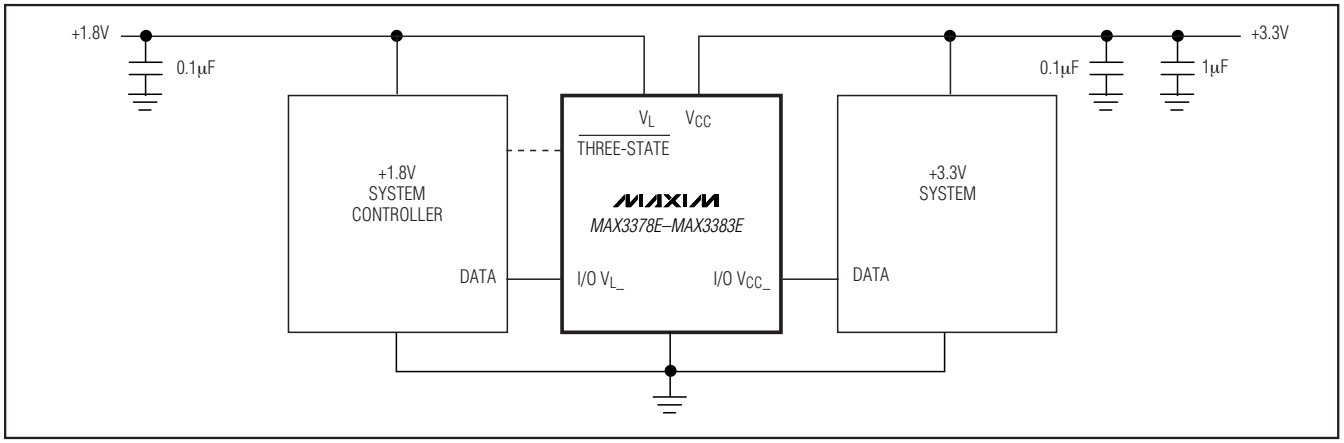
I²C Level Translation

The MAX3373E–MAX3376E, MAX3378E/MAX3379E and MAX3390E–MAX3393E level-shift the data present on the I/O lines between +1.2V and +5.5V, making them ideal for level translation between a low-voltage ASIC and an I²C device. A typical application involves interfacing a low-voltage microprocessor to a 3V or 5V D/A converter, such as the MAX517.

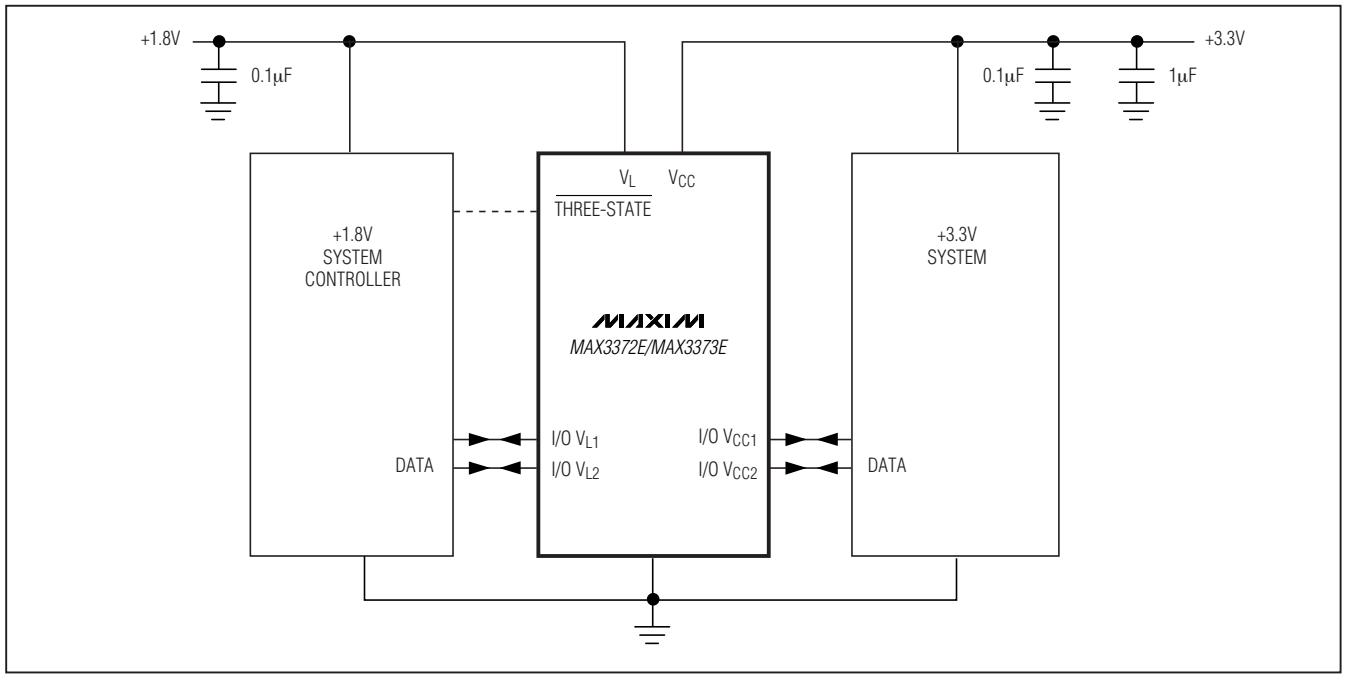
Push-Pull vs. Open-Drain Driving

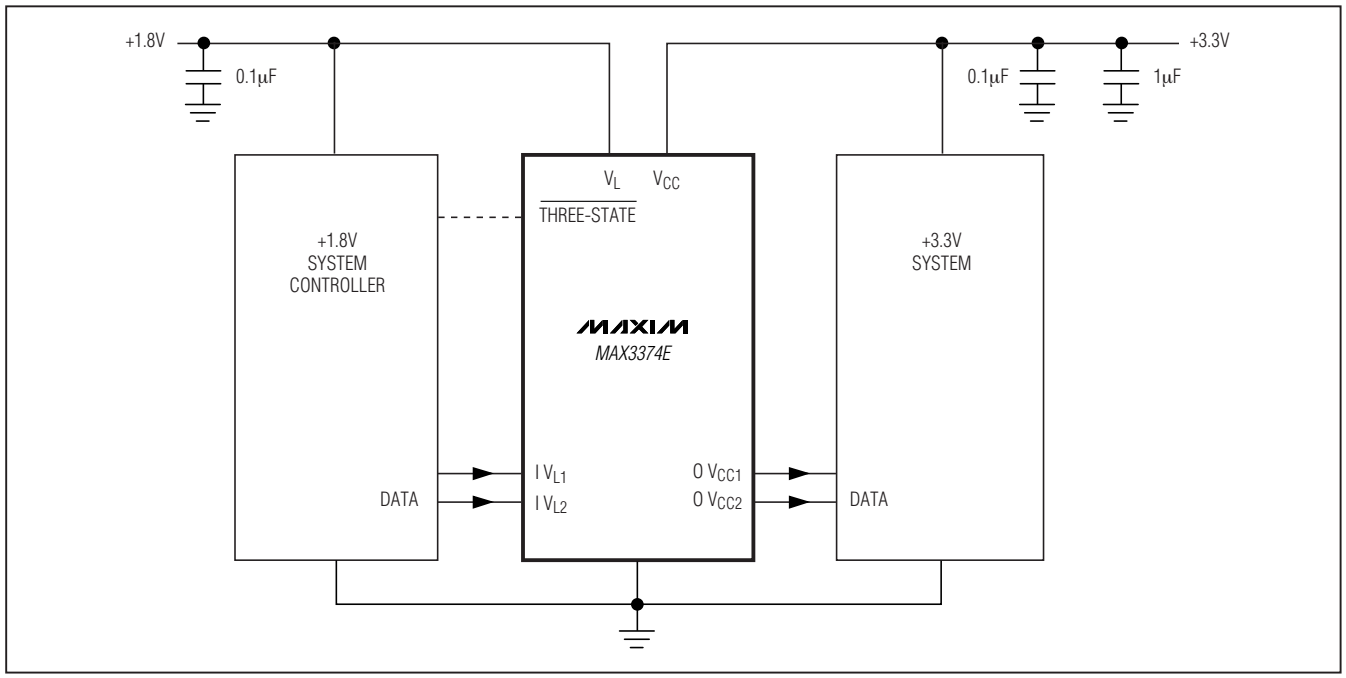
All devices in the MAX3372E–MAX3379E and MAX3390E–MAX3393E family may be driven in a push-pull configuration. The MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E include internal 10kΩ resistors that pull up I/O $V_{L\_}$ and I/O $V_{CC\_}$ to their respective power supplies, allowing operation of the I/O lines with open-drain devices. See the *Timing Characteristics* table for maximum data rates when using open-drain drivers.

Typical Operating Circuit



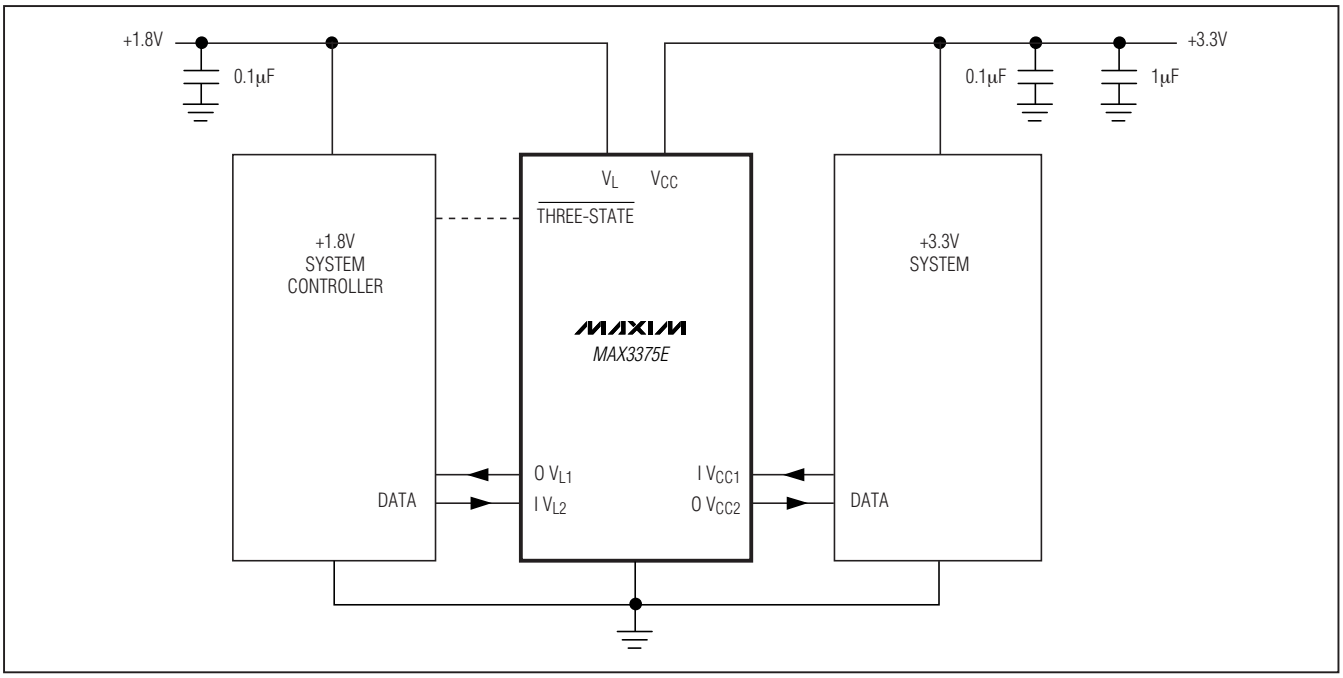
Applications Circuits

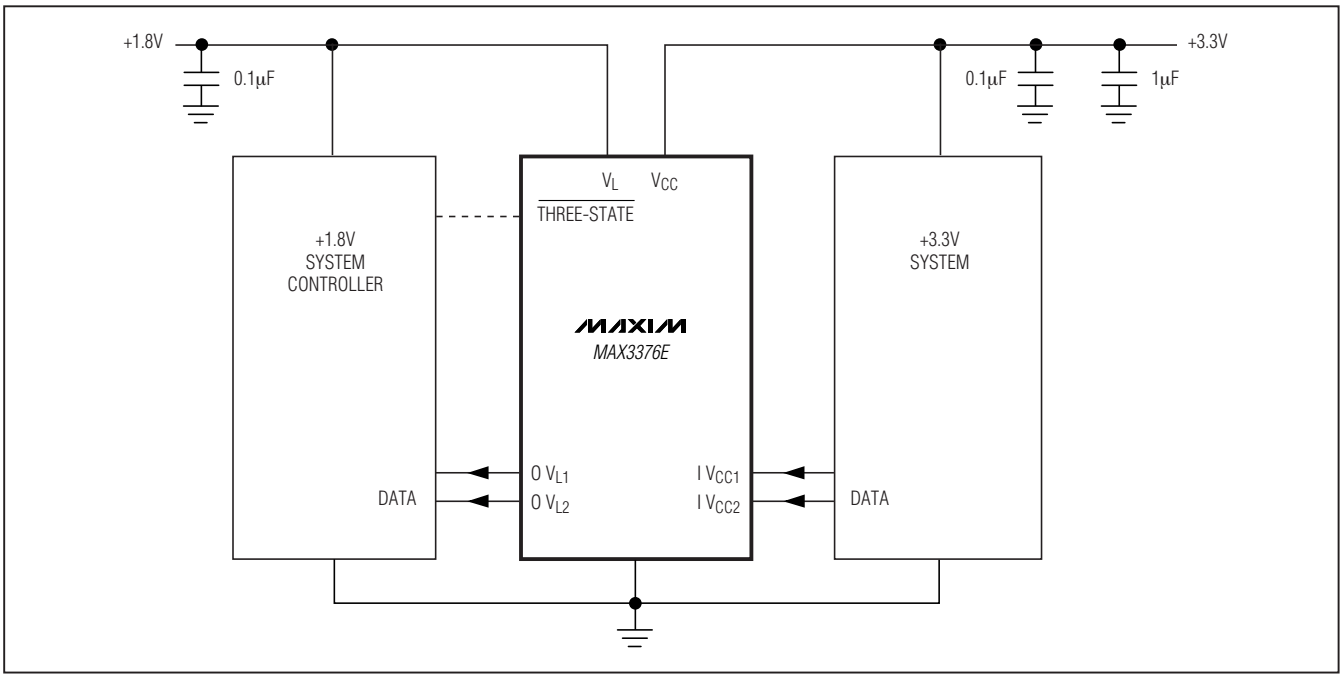




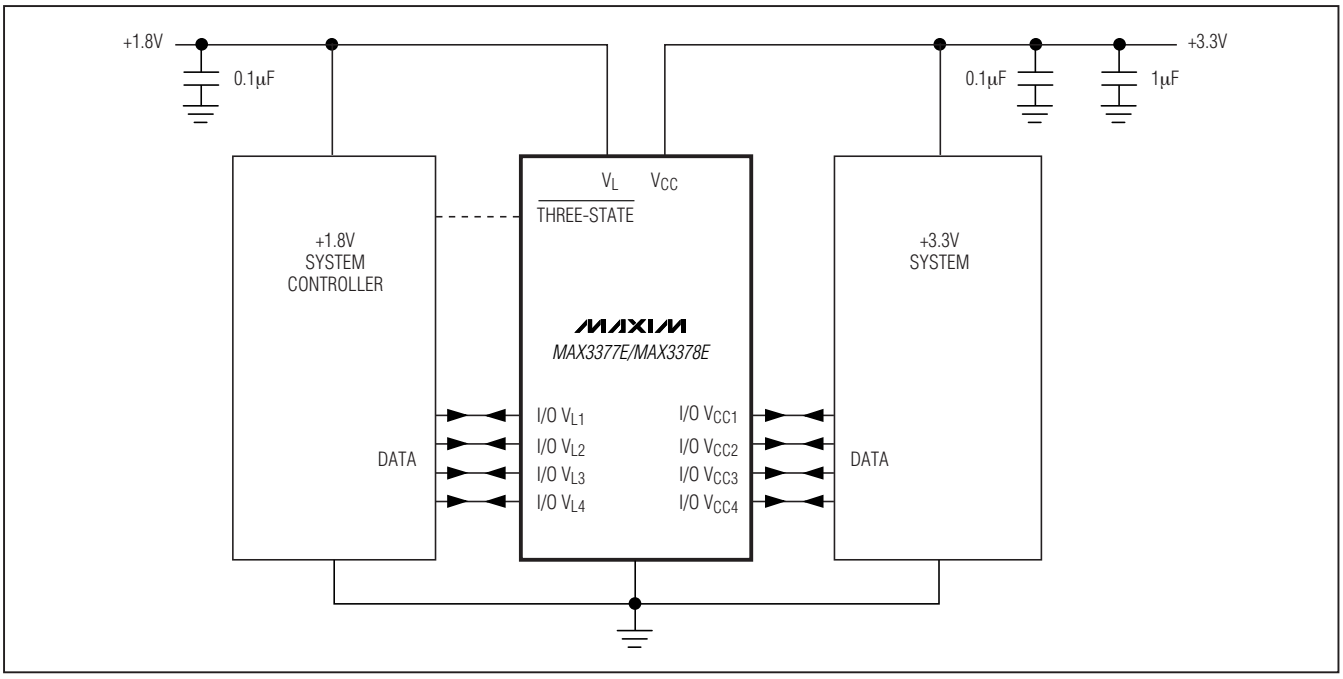
±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

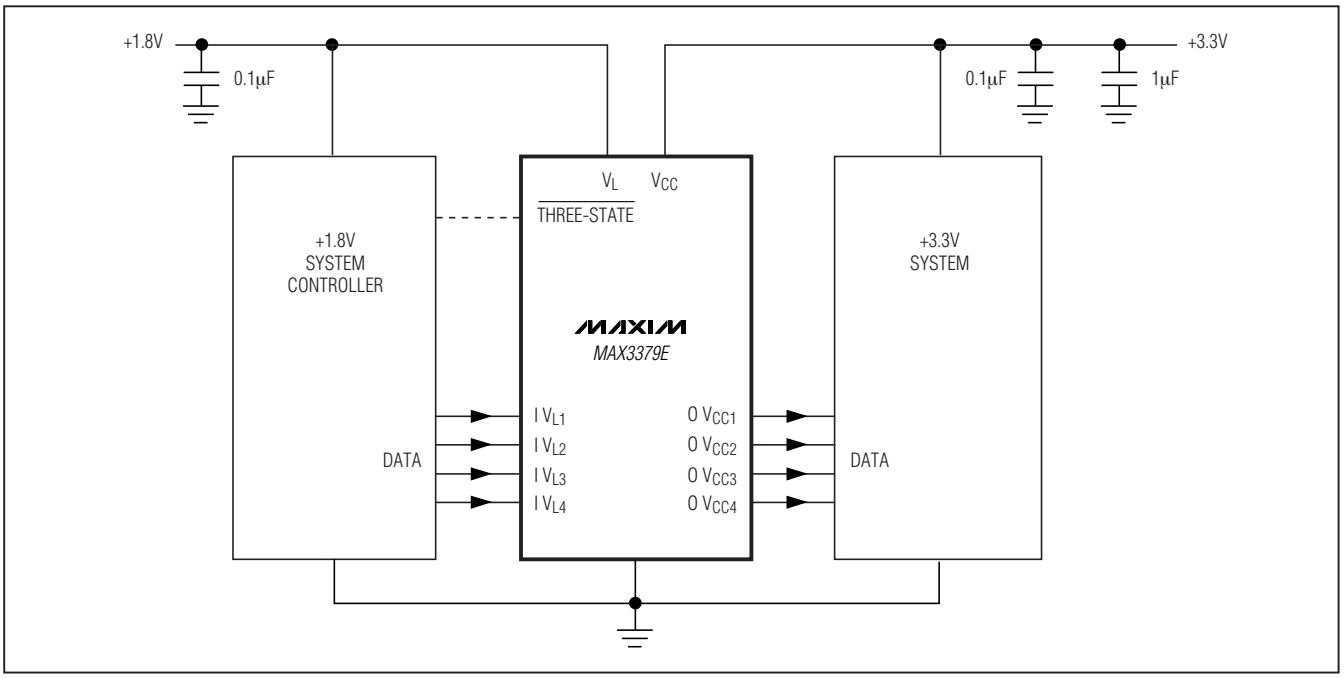
Applications Circuits (continued)





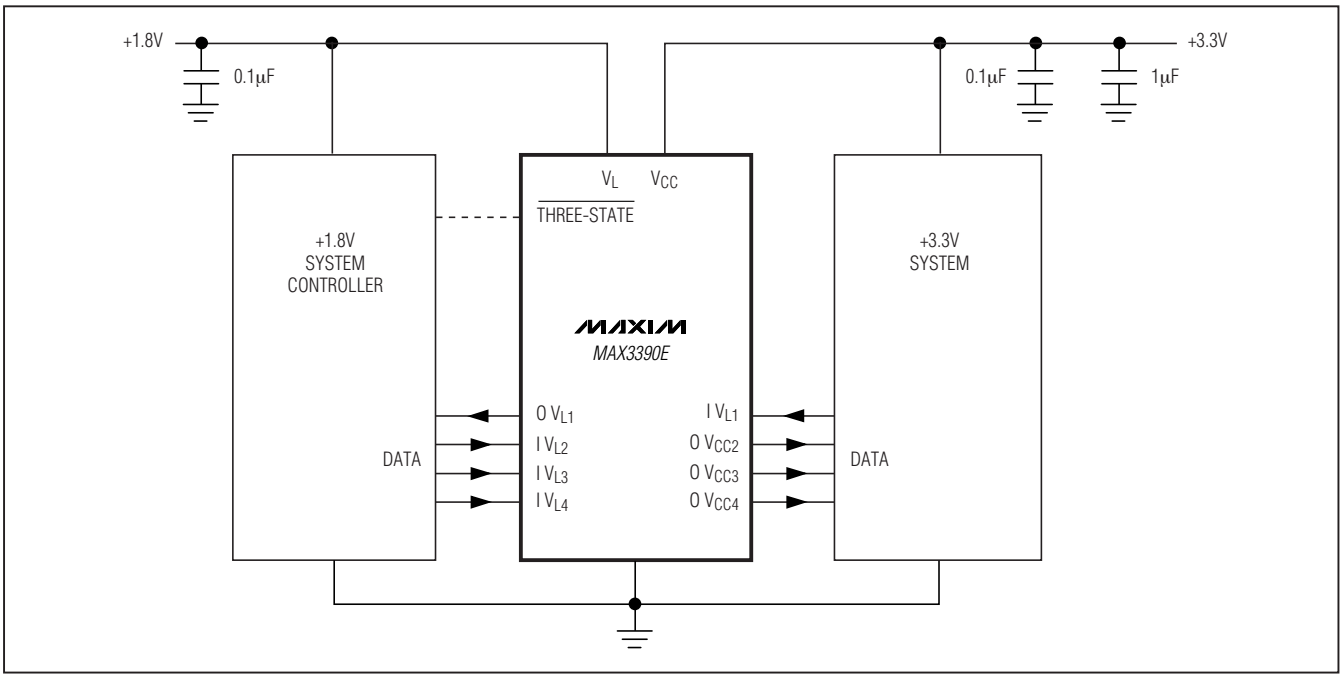
Applications Circuits (continued)

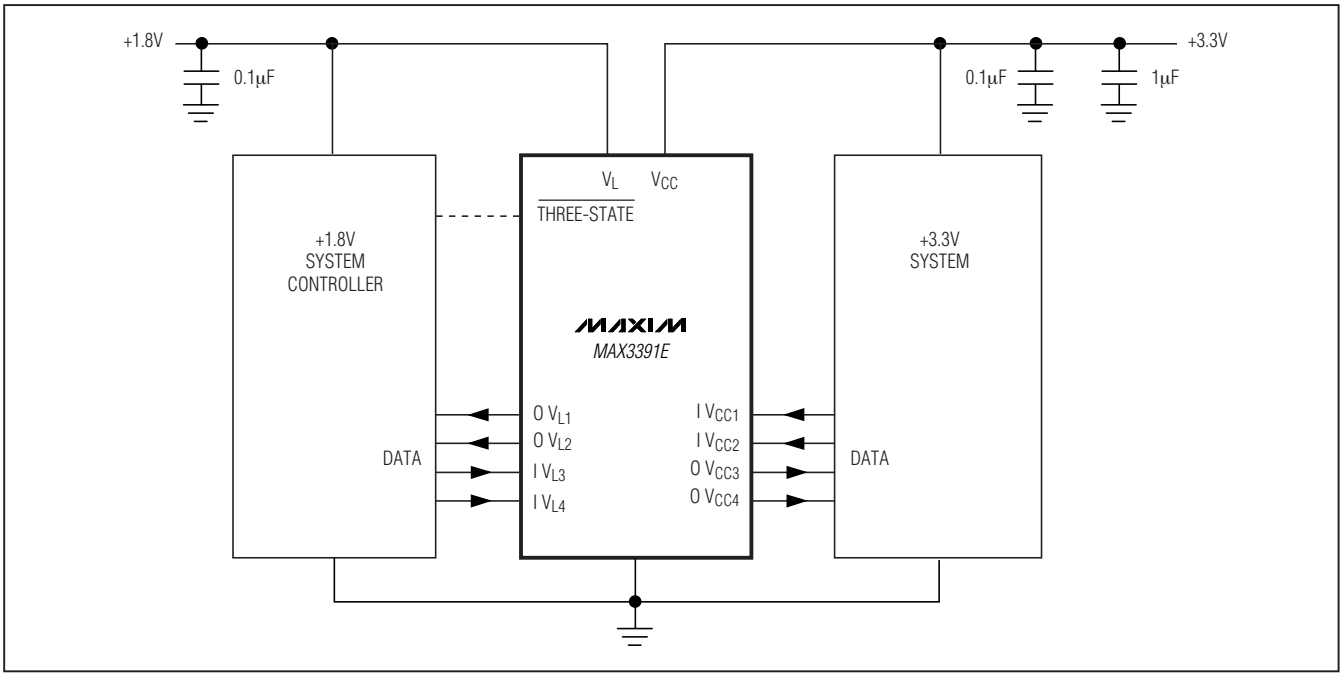




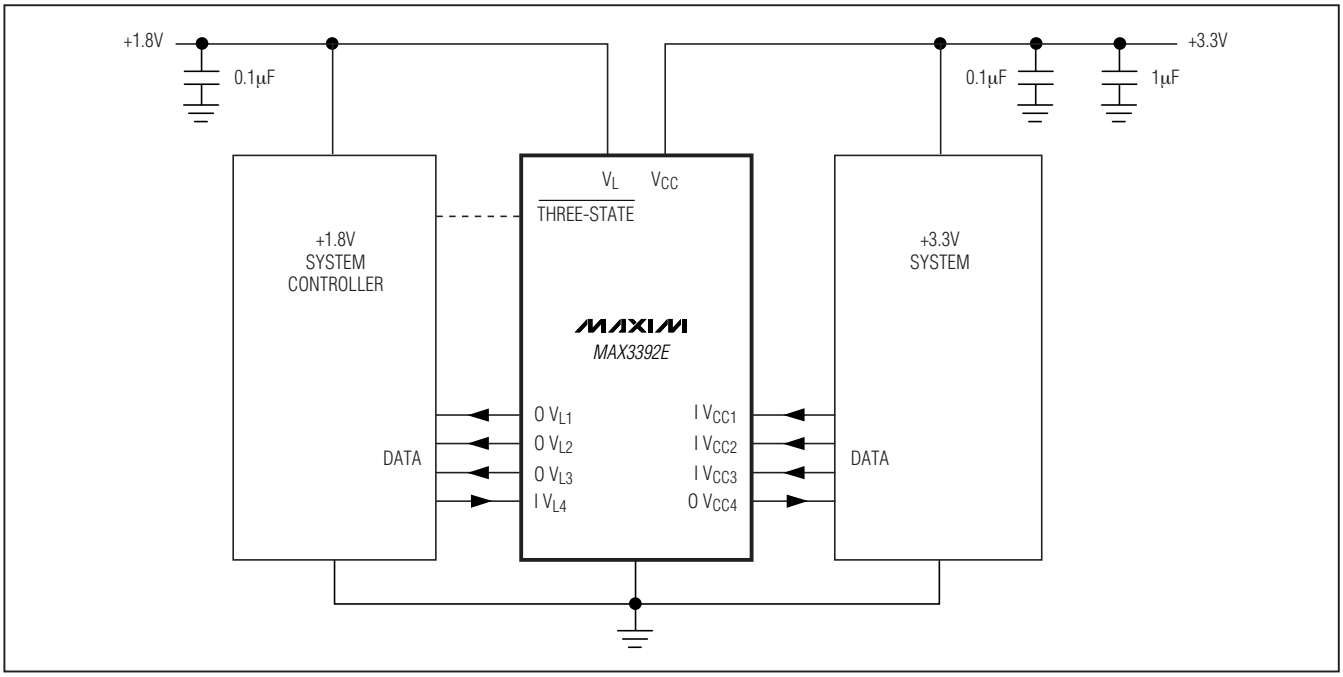
±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

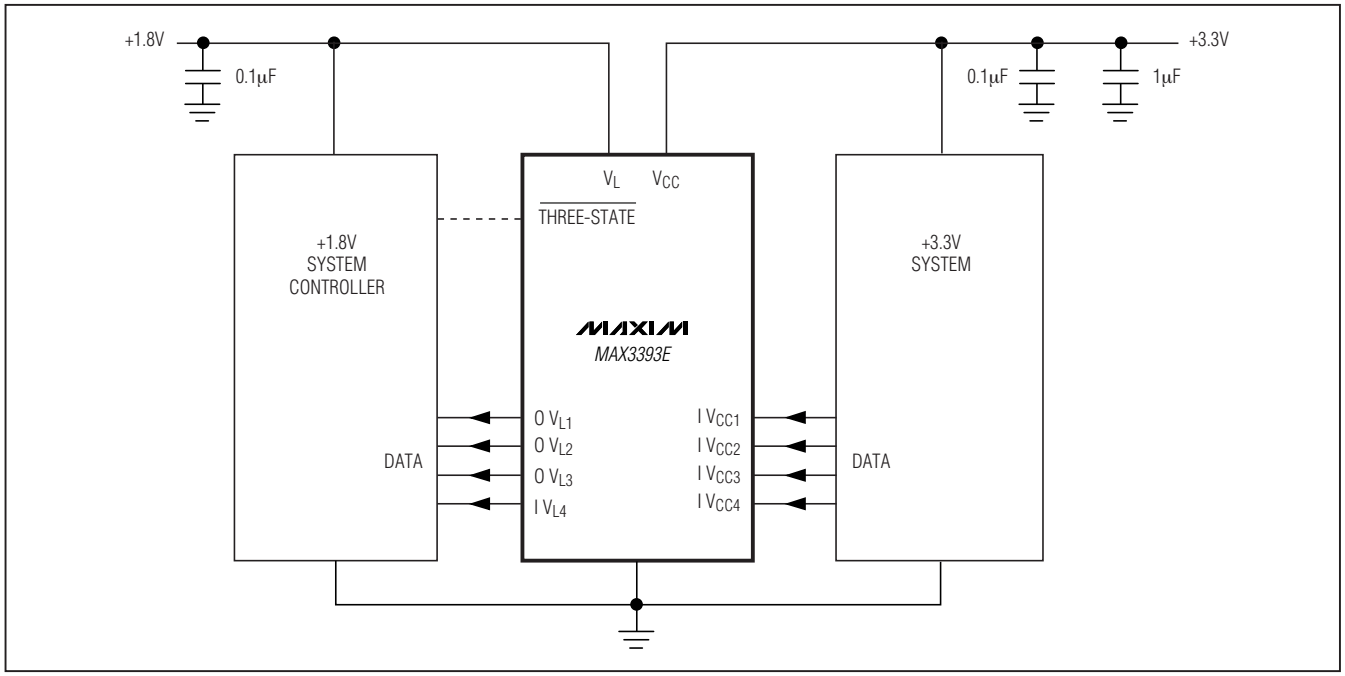
Applications Circuits (continued)





Applications Circuits (continued)





±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

Selector Guide

PART	LEVEL TRANS-LATION	Tx/Rx†	DATA RATE	TOP MARK
MAX3372EEKA+T	✓ Bi	2/2	230kbps	AAKO
MAX3372EEBL+T	✓ Bi	2/2		AAR
MAX3372EETA+T	✓ Bi	2/2		AQG
MAX3373EEKA+T	✓ Bi	2/2	8Mbps*	AAKS
MAX3373EEBL+T	✓ Bi	2/2		AAZ
MAX3373EETA+T	✓ Bi	2/2		AQH
MAX3374EEKA+T	Uni	2/0		AALH
MAX3374EEBL+T	Uni	2/0		ABA
MAX3374EETA+T	Uni	2/0		AQI
MAX3375EEKA+T	Uni	1/1		AALI
MAX3375EEBL+T	Uni	1/1		ABB
MAX3375EETA+T	Uni	1/1		AQJ
MAX3376EEKA+T	Uni	0/2		AALG
MAX3376EEBL+T	Uni	0/2		AAV
MAX3376EETA+T	Uni	0/2		AQK
MAX3377EEUD	✓ Bi	4/4	230kbps	—
MAX3377EEBC+T	✓ Bi	4/4		AAX
MAX3377EETD+T	✓ Bi	4/4		AAG
MAX3378EEUD	✓ Bi	4/4	8Mbps*	—
MAX3378EEBC+T	✓ Bi	4/4		AAY
MAX3378EETD+T	✓ Bi	4/4		AAH
MAX3379EEUD	Uni	4/0		—
MAX3379EEBC+T	Uni	4/0		AAZ
MAX3379EETD+T	Uni	4/0		AAI
MAX3390EEUD	Uni	3/1		—
MAX3390EEBC+T	Uni	3/1		ABA
MAX3390EETD+T	Uni	3/1		AAJ
MAX3391EEUD	Uni	2/2		—
MAX3391EEBC+T	Uni	2/2		ABB
MAX3391EETD+T	Uni	2/2		AAK
MAX3392EEUD	Uni	1/3		—
MAX3392EEBC+T	Uni	1/3		ABC
MAX3392EETD+T	Uni	1/3		AAL
MAX3393EEUD	Uni	0/4		—
MAX3393EEBC+T	Uni	0/4		ABD
MAX3393EETD+T	Uni	0/4		AAM

†*Tx = V_L → V_{CC}, Rx = V_{CC} → V_L*

**Higher data rates are possible (see the Timing Characteristics table).*

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3372EEBL+T	-40°C to +85°C	9 UCSP (1.5mm x 1.5mm)	B9-2
MAX3372EETA+T	-40°C to +85°C	8 TDFN-EP** (3mm x 3mm)	T833-2
MAX3373EEKA+T	-40°C to +85°C	8 SOT23	K8S-3
MAX3373EEBL+T	-40°C to +85°C	9 UCSP (1.5mm x 1.5mm)	B9-2
MAX3373EETA+T	-40°C to +85°C	8 TDFN-EP** (3mm x 3mm)	T833-2
MAX3374EEKA+T	-40°C to +85°C	8 SOT23	K8S-3
MAX3374EEBL+T	-40°C to +85°C	9 UCSP (1.5mm x 1.5mm)	B9-2
MAX3374EETA+T	-40°C to +85°C	8 TDFN-EP** (3mm x 3mm)	T833-2
MAX3375EEKA+T	-40°C to +85°C	8 SOT23	K8S-3
MAX3375EEBL+T	-40°C to +85°C	9 UCSP (1.5mm x 1.5mm)	B9-2
MAX3375EETA+T	-40°C to +85°C	8 TDFN-EP** (3mm x 3mm)	T833-2
MAX3376EEKA+T	-40°C to +85°C	8 SOT23	K8S-3
MAX3376EEBL+T	-40°C to +85°C	9 UCSP (1.5mm x 1.5mm)	B9-2
MAX3376EETA+T	-40°C to +85°C	8 TDFN-EP** (3mm x 3mm)	T833-2
MAX3377EEUD	-40°C to +85°C	14 TSSOP	U14-1
MAX3377EEBC+T	-40°C to +85°C	9 UCSP (1.5mm x 1.5mm)	B12-1
MAX3377EETD+T	-40°C to +85°C	14 TDFN-EP** (3mm x 3mm)	T1433-2
MAX3378EEUD	-40°C to +85°C	14 TSSOP	U14-1
MAX3378EEBC+T	-40°C to +85°C	12 UCSP (1.5mm x 2.0mm)	B12-1
MAX3378EETD+T	-40°C to +85°C	14 TDFN-EP** (3mm x 3mm)	T1433-2

+Denotes a lead-free package.
***EP = Exposed pad.*
T = Tape and reel.

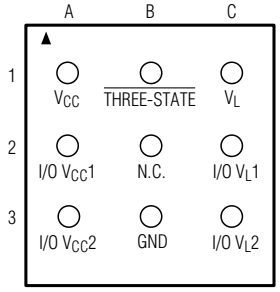
Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3379EEUD†	-40°C to +85°C	14 TSSOP	U14-1
MAX3379EEBC+T†	-40°C to +85°C	12 UCSP (1.5mm x 2.0mm)	B12-1
MAX3379EETD+T†	-40°C to +85°C	14 TDFN-EP** (3mm x 3mm)	T1433-2
MAX3390EEUD†	-40°C to +85°C	14 TSSOP	U14-1
MAX3390EEBC+T†	-40°C to +85°C	12 UCSP (1.5mm x 2.0mm)	B12-1
MAX3390EETD+T	-40°C to +85°C	14 TDFN-EP** (3mm x 3mm)	T1433-2
MAX3391EEUD†	-40°C to +85°C	14 TSSOP	U14-1
MAX3391EEBC+T†	-40°C to +85°C	12 UCSP (1.5mm x 2.0mm)	B12-1
MAX3391EETD+T	-40°C to +85°C	14 TDFN-EP** (3mm x 3mm)	T1433-2
MAX3392EEUD†	-40°C to +85°C	14 TSSOP	U14-1
MAX3392EEBC+T†	-40°C to +85°C	12 UCSP (1.5mm x 2.0mm)	B12-1
MAX3392EETD+T	-40°C to +85°C	14 TDFN-EP** (3mm x 3mm)	T1433-2
MAX3393EEUD†	-40°C to +85°C	14 TSSOP	U14-1
MAX3393EEBC+T†	-40°C to +85°C	12 UCSP (1.5mm x 2.0mm)	B12-1
MAX3393EETD+T†	-40°C to +85°C	14 TDFN-EP** (3mm x 3mm)	T1433-2

+Denotes a lead-free package.
***EP = Exposed pad.*
T = Tape and reel.
†Future product—contact factory for availability.

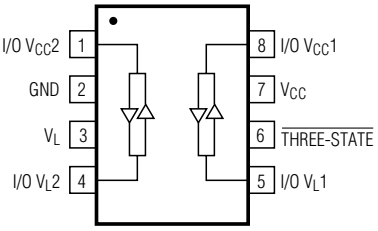
±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

Pin Configurations (continued)

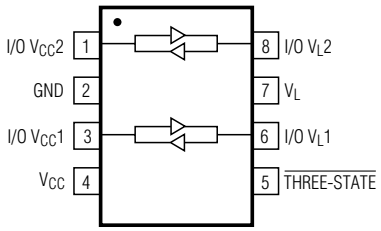


9 UCSP (1.5mm x 1.5mm)
BOTTOM VIEW

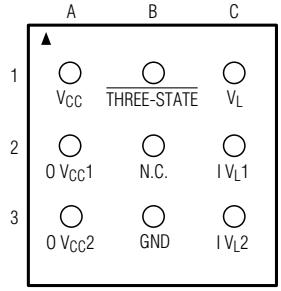
MAX3372E
MAX3373E



SOT23-8
TOP VIEW

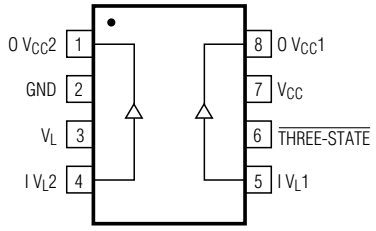


TDFN-8 (3mm x 3mm)
TOP VIEW

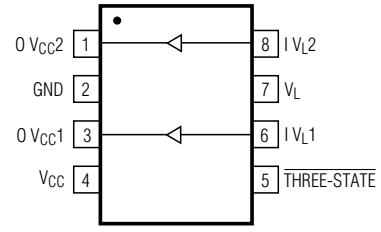


9 UCSP (1.5mm x 1.5mm)
BOTTOM VIEW

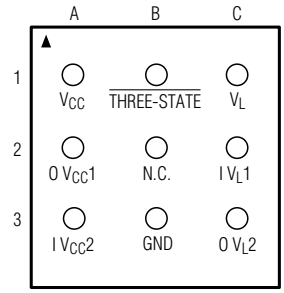
MAX3374E



SOT23-8
TOP VIEW

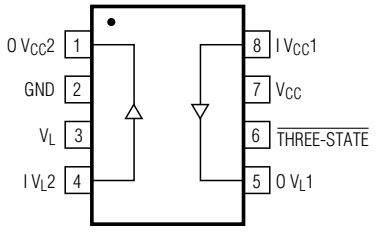


TDFN-8 (3mm x 3mm)
TOP VIEW

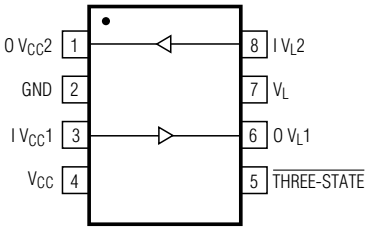


9 UCSP (1.5mm x 1.5mm)
BOTTOM VIEW

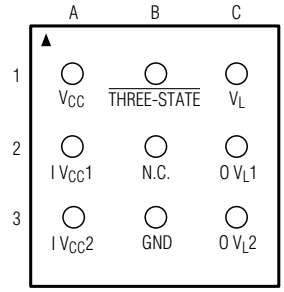
MAX3375E



SOT23-8
TOP VIEW

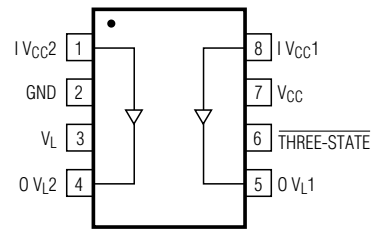


TDFN-8 (3mm x 3mm)
TOP VIEW

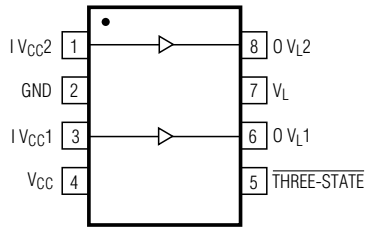


9 UCSP (1.5mm x 1.5mm)
BOTTOM VIEW

MAX3376E

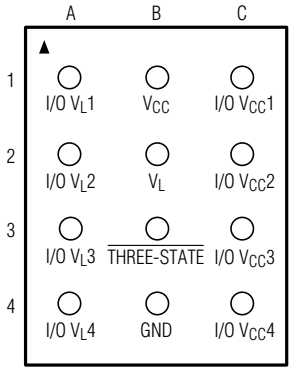


SOT23-8
TOP VIEW



TDFN-8 (3mm x 3mm)
TOP VIEW

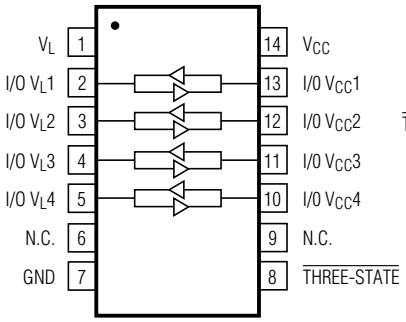
Pin Configurations (continued)



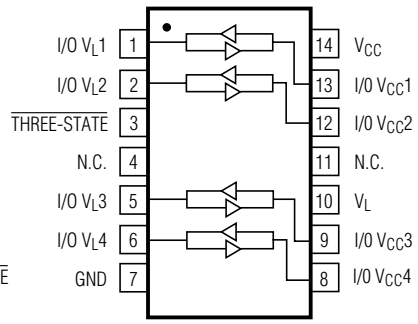
12 UCSP (1.5mm x 2.0mm)
BOTTOM VIEW

MAXIM

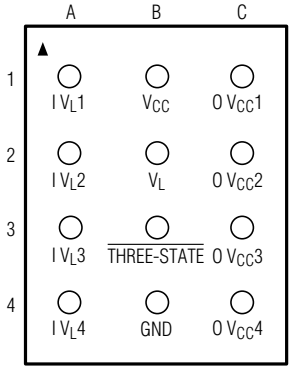
MAX3377E
MAX3378E



TSSOP-14
TOP VIEW



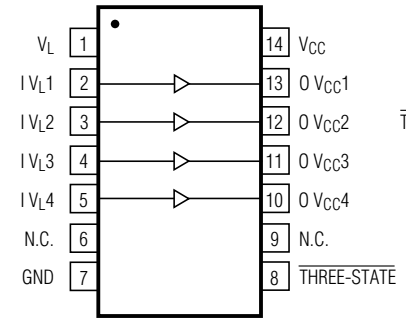
TDFN-14 (3mm x 3mm)
TOP VIEW



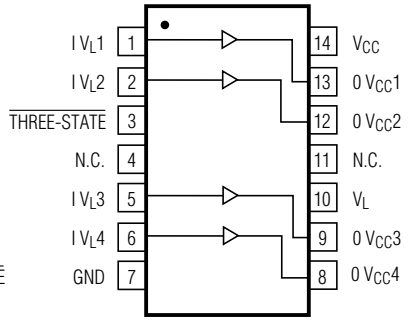
12 UCSP (1.5mm x 2.0mm)
BOTTOM VIEW

MAXIM

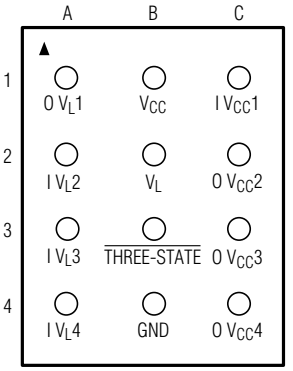
MAX3379E



TSSOP-14
TOP VIEW



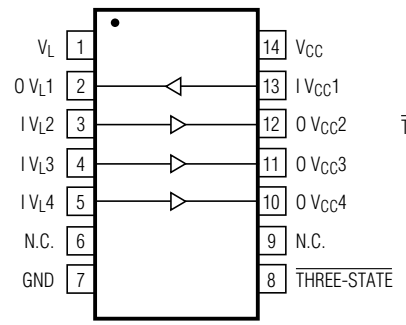
TDFN-14 (3mm x 3mm)
TOP VIEW



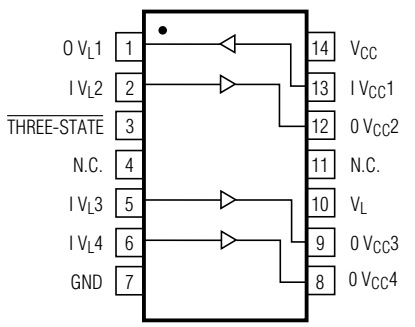
12 UCSP (1.5mm x 2.0mm)
BOTTOM VIEW

MAXIM

MAX3390E



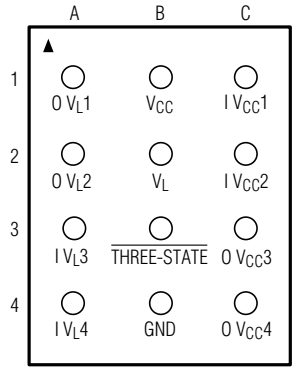
TSSOP-14
TOP VIEW



TDFN-14 (3mm x 3mm)
TOP VIEW

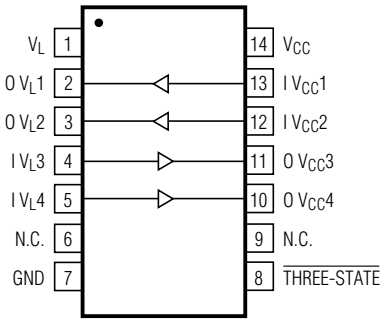
±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

Pin Configurations (continued)

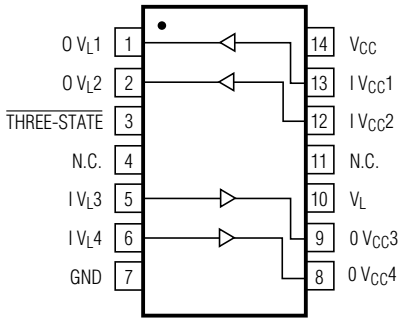


12 UCSP (1.5mm x 2.0mm)
BOTTOM VIEW

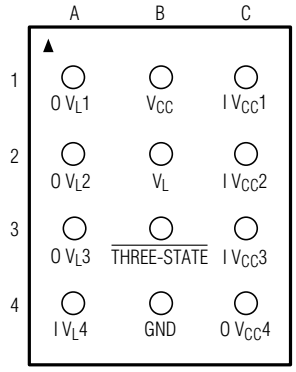
MAXIM
MAX3391E



TSSOP-14
TOP VIEW

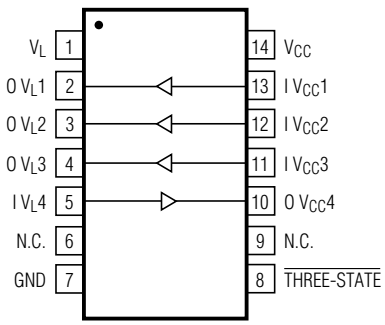


TDFN-14 (3mm x 3mm)
TOP VIEW

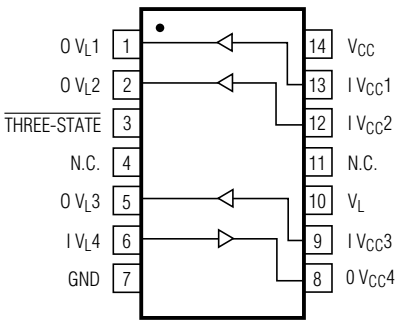


12 UCSP (1.5mm x 2.0mm)
BOTTOM VIEW

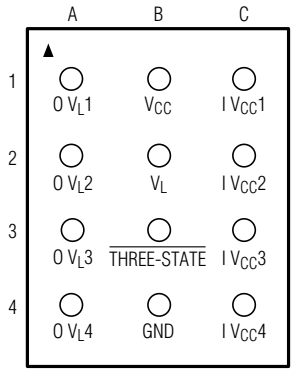
MAXIM
MAX3392E



TSSOP-14
TOP VIEW

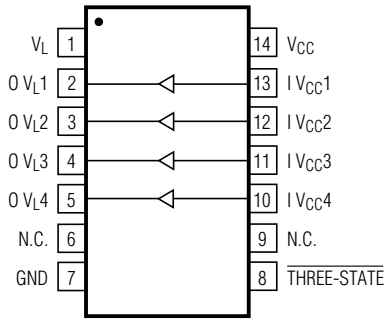


TDFN-14 (3mm x 3mm)
TOP VIEW

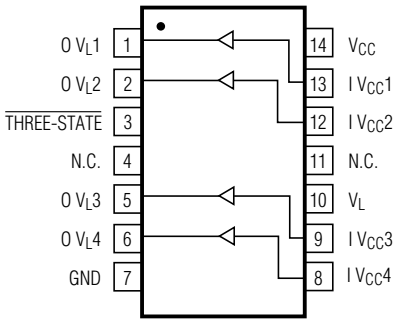


12 UCSP (1.5mm x 2.0mm)
BOTTOM VIEW

MAXIM
MAX3393E



TSSOP-14
TOP VIEW

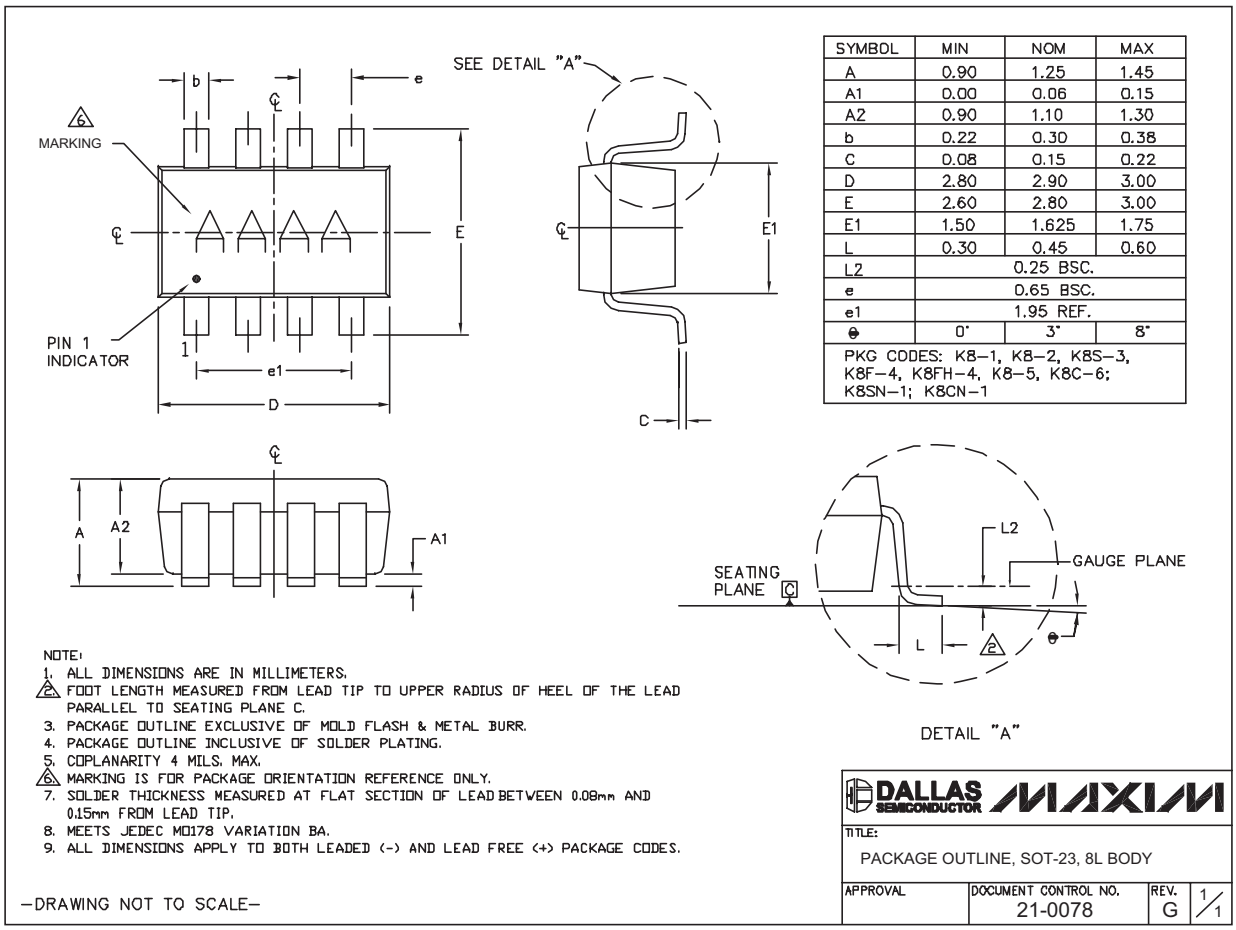


TDFN-14 (3mm x 3mm)
TOP VIEW

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOT23, 8L.EPS



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2		0.25 BSC.	
e		0.65 BSC.	
e1		1.95 REF.	
θ	0°	3°	8°

PKG CODES: K8-1, K8-2, K8S-3, K8F-4, K8FH-4, K8-5, K8C-6; K8SN-1; K8CN-1

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	G	1/1

Chip Information

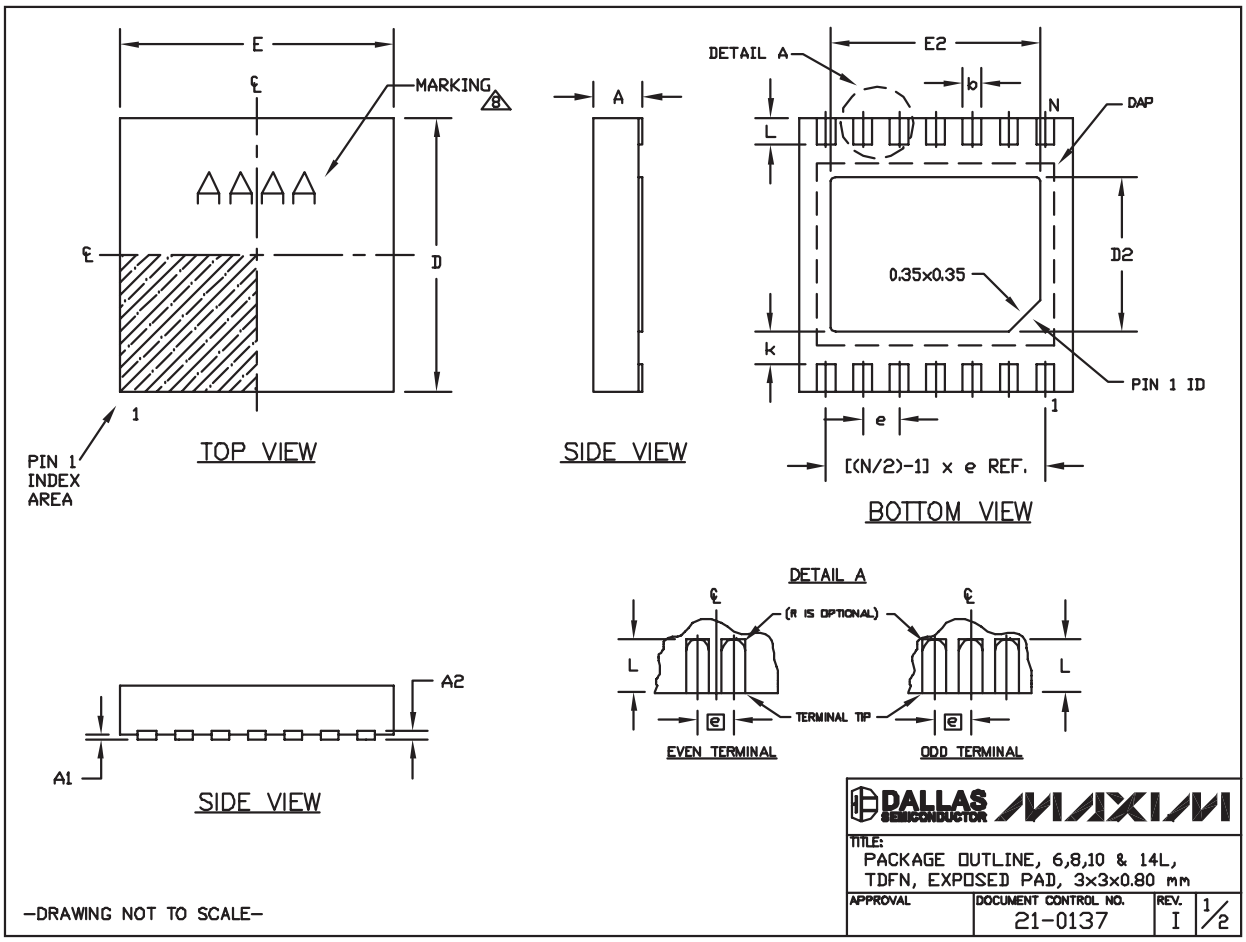
TRANSISTOR COUNT: MAX3372E–MAX3376E: 189
MAX3377E–MAX3379E,
MAX3390E–MAX3393E: 295

PROCESS: BiCMOS

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

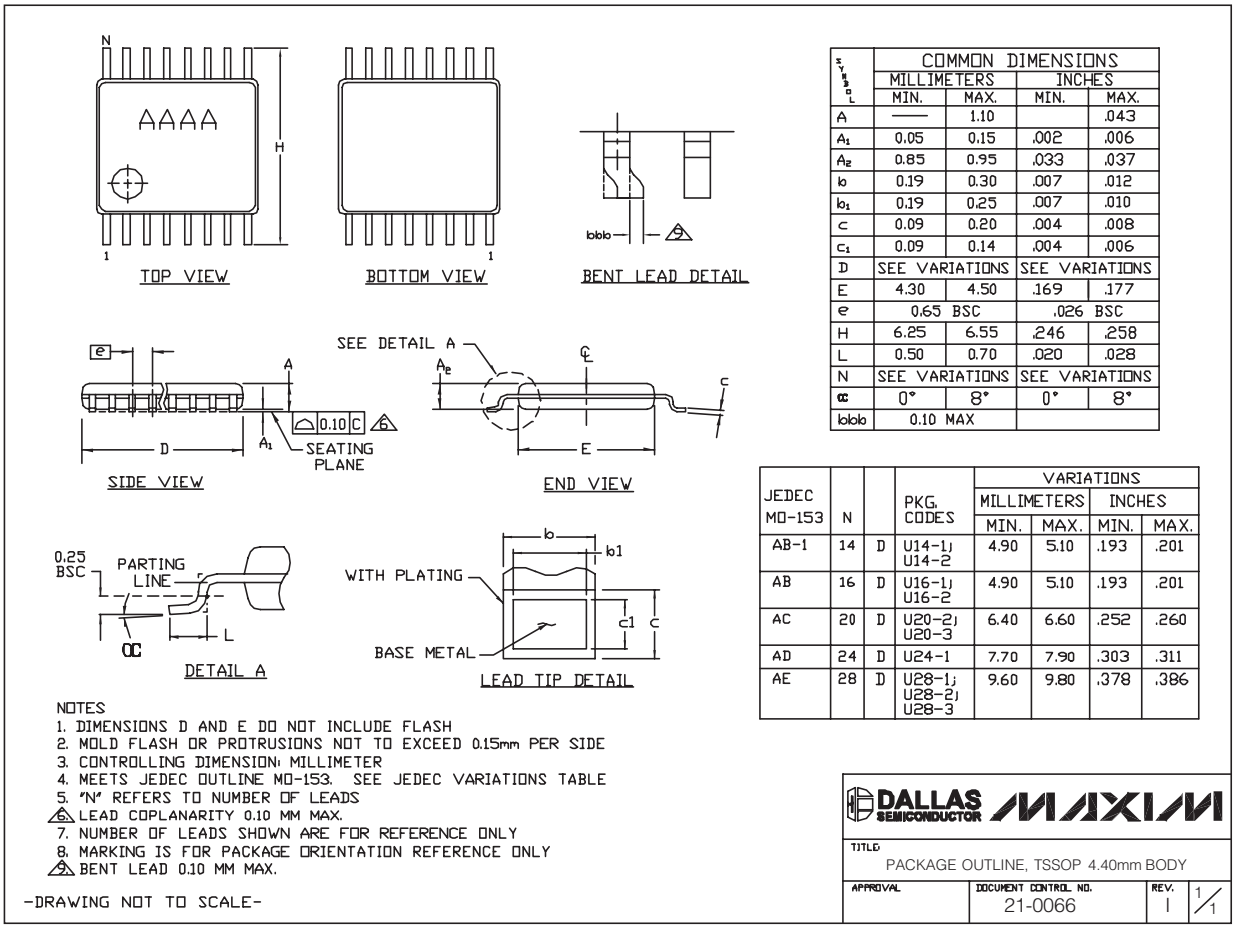
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1, U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1, U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2, U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1, U28-2, U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

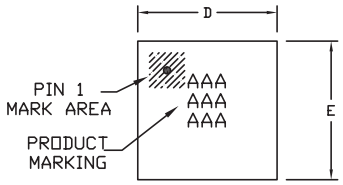
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	I	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

9LUCSP, 3x3.EPS

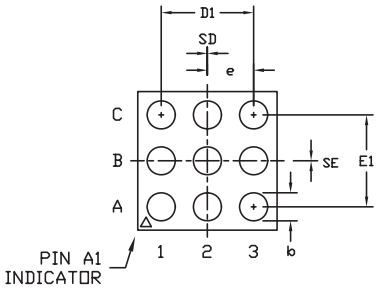


TOP VIEW

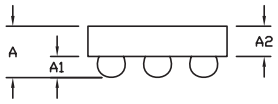
COMMON DIMENSIONS	
A	0.62±0.05–0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.52±0.05	1.52±0.05	A2, B1, B2, B3, C2
B9-8	1.98±0.05	1.75±0.05	B1, B2, B3

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 3x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0093	L	1/1

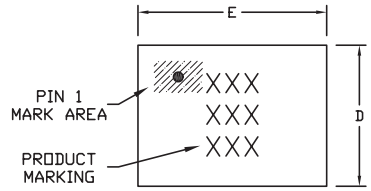
-DRAWING NOT TO SCALE-

±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

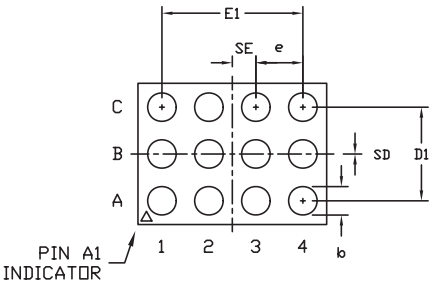
12L, UCSP 4x3.EPS



TOP VIEW

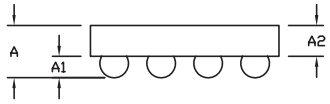
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 4x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0104	F	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/02	Initial Release	—
1	12/06	Addition of 12-bump ECSP packaging	–
2	11/07	Addition of lead-free options	1, 20–31