Serial Data Receiver

LIU-01

FEATURES

- Recovers Data From Lines Varying From 0 ft. to Over 6000 ft.
- Wide Data Range, Under 300bps to Over 6Mbps
- Accepts RZ and NRZ Data Formats
- Accepts Unipolar and Bipolar Transmission Formats
- Single +5Volt Operation
- Automatic Gain/ Equalization Control; Dynamic Range>60dB
- TTL/CMOS Compatible Clock and Data Outputs
- Provides LOSS-OF-CARRIER Output
- Suitable for T1, E1, T1C, T2, DDS, and LAN Applications
- Meets CCITT and ATT Specifications for ISDN Compatibility

APPLICATIONS

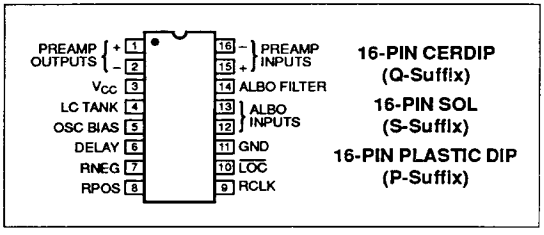
- PBXs and LANs Using Twisted-Pair, Coax, or Fiber Optic Cable
- ISDN Compatible Equipment: Computers, FAX Machines, Test Equipment
- Industrial Communications/Process Control
- Digital Multiplexers, CSUs, and Switching Equipment

GENERAL DESCRIPTION

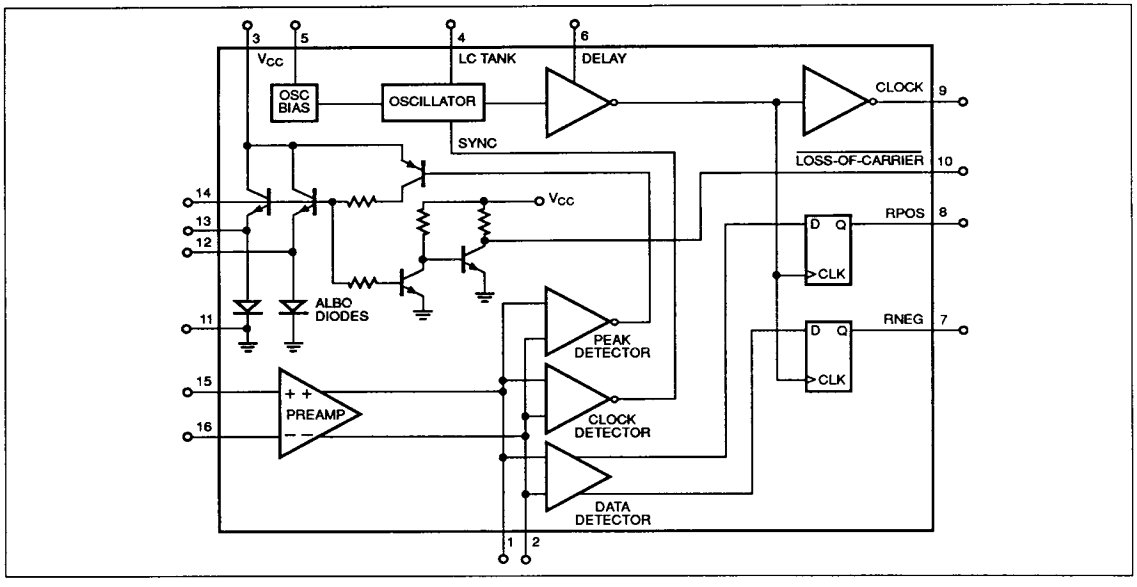
The LIU-01 is a versatile monolithics receiver for use in serial data transmission networks. It allows the recovery of data transmitted in both RZ and NRZ formats over lines from 0 ft. to over 6000 ft. The LIU-01 separates the clock from data and presents both clock and data as TTL/CMOS compatible outputs. A LOSS-OF-CARRIER output is also provided to indicate that the incoming signal has fallen below a usable level. The LIU-01 incorporates a high gain preamplifier and dual ALBO ports enabling it to automatically

Continued

PIN CONNECTIONS



FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION *Continued*

adjust for the signal attenuation and frequency distortion encountered at varying lengths of twisted-pair, coax, or fiber optic transmission lines. It will tolerate an input signal range of over 60dB and can handle data rates ranging from less than 300bps to greater than 6Mbps.

The LIU-01 meets all CCITT and ATT specifications for an ISDN compatible receiver interface. Additionally, it is directly compatible with the R8070 and, with one additional inverter gate, the DS2180 digital T1 transeivers.

ORDERING INFORMATION †

PACKAGE		OPERATING TEMPERATURE RANGE
CERDIP 16-PIN	PLASTIC 16-PIN	
LIU01FQ	LIU01FP	XIND
—	LIU-1FS††	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS

Maximum Voltage, Pin 3 to Pin 11 ..... 6.5V, –0.5V
Maximum Voltage, Any Pin Except 12 and 13 ..... V_{CC}
Maximum Sinking Current, Any Pin 20mA
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Soldering Temperature ..... +300°C
Junction Temperature ..... +150°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_{CC} = 5V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	LIU-01F MIN	LIU-01F TYP	LIU-01F MAX	UNITS
SUPPLY						
Supply Current	I_{CC}	(Note 1)	–	20	28	mA
Supply Voltage	V_{CC}		4.75	5.0	5.5	V
PREAMPLIFIER						
Preamplifier Open-Loop Gain	A_O	$\Delta A_V(Diff)/(2\Delta_{VIN}(Diff))$	52	56	–	dB
Preamplifier Bandwidth	B_W	–3dB (Note 2)	6	9	–	MHz
Preamplifier Input Impedance, Differential	Z_{IN}	f = 1.544MHz	–	50	–	kΩ
Preamplifier Input Offset Voltage	V_{OS}	(Note 1)	–	0.8	5	mV
Preamplifier Output Impedance	Z_{OUT}		–	50	100	Ω
Preamplifier Output High	V_{OHA}	T_A = +25°C	3.8	4.0	–	V
Preamplifier Output Low	V_{OLA}	T_A = +25°C	–	1.0	1.2	V
Preamplifier Input Bias Current	I_B	(Note 1)	–	1	4	µA
Preamplifier Input Offset Current	I_{OS}	(Note 1)	–	0.01	0.5	µA
Preamplifier Output Self-Bias Voltage	V_{DC}	T_A = +25°C	–	2.5	–	V
OUTPUT DRIVE						
Output High Voltage, $\overline{LOC}$	V_{OHC}	I_L = 100µA	3.5	4.0	–	V
Output Low Voltage, $\overline{LOC}$	V_{OLC}	I_L = 5mA	–	0.22	0.4	V
Output High Voltage, RPOS, RNEG, RCLK	V_{OHD}	I_L = 400µA	3.2	3.5	–	V
Output Low Voltage, RPOS, RNEG, RCLK	V_{OLD}	I_L = - 5mA	–	0.15	0.4	V

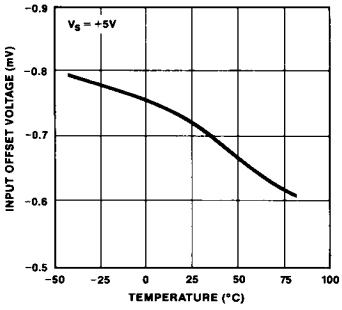
ELECTRICAL CHARACTERISTICS at V_{CC} = 5V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	LIU-01F MIN	TYP	MAX	UNITS
Output Pulse Rise-Time	T_{OR}		–	20	–	ns
Output Pulse Fall-Time	T_{OF}		–	20	–	ns
Output Pulse-Width, RPOS, RNEG	P_{WD}	f = 1.544MHz	–	648	–	ns
Output Pulse-Width, RCLK	P_{WC}	f = 1.544MHz	–	280	–	ns
CLOCK CIRCUIT						
Oscillator Bias Voltage	V_{BIAS}	$V_{PIN\,5}$	–	4	–	V
Tank Emitter-Follower Base Current	I_{TB}	(Note 1)	–	5	–	µA
Oscillator Bias Current	I_{OSC}		–	720	–	µA
Oscillator Injection Current	I_{INH}		–	200	–	µA
Data Sampling Interval	T_{DS}		–	20	–	ns
Delay Circuit Resistor	R_d	Measured from Pin 6 to Pin 3 T_A = +25°C	700	1000	1300	Ω
ALBO						
ALBO Threshold	V_{TA}	Differential Voltage, measured between Pins 1 and 2, required to activate the Peak Detector	1.35	1.5	1.65	V
ALBO Threshold ±Differential	V_{TAD}		–	–	75	mV
ALBO ON Voltage	V_{O14}	Measured at Pin 14, $[V_{PIN\,1} - V_{PIN\,2}]$ = ALBO Threshold + 20mV	1.0	1.7	4.0	V
ALBO OFF Voltage V_{F14}		Measured at Pins 12, 13, 14 (Note 1)	–	–	75	mV
Minimum ALBO Diode Resistance	R_D MIN		–	6	15	Ω
Maximum ALBO Diode Impedance	R_D MAX	f = 1.544MHz (Note 2)	20	30	–	kΩ
ALBO Diode Impedance Matching		R_D = 100Ω	–	10	–	%
DATA/CLOCK THRESHOLDS						
Clock Threshold	V_{TC}	Differential Voltage, measured between Pins 1 and 2, required to activate the Peak Detector	0.92	1.05	11.22	V
Clock Threshold as % of ALBO Voltage	$V_{TC\%}$		68	71	74	%
Data Threshold	V_{TD}	Differential Voltage, measured between Pins 1 and 2, required to activate the Peak Detector	0.62	0.75	0.90	V
Data Threshold as % of ALBO Voltage	$T_{CD\%}$		46	50	54	%

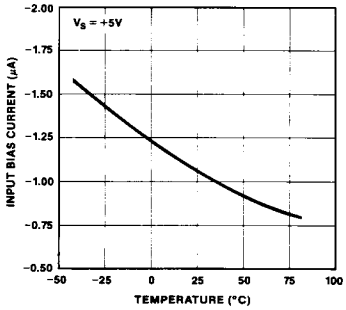
NOTES:
1. Preamplifier self-biased $V_{PIN\,1} \approx V_{PIN\,2} \approx V_{PIN\,15} \approx V_{PIN\,16}$.
2. Guaranteed by design.

TYPICAL ELECTRICAL CHARACTERISTICS

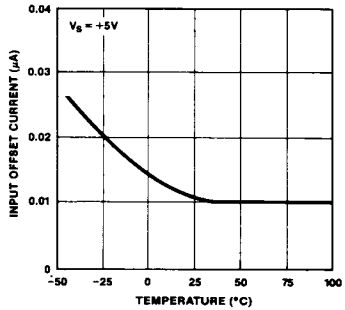
INPUT OFFSET VOLTAGE vs TEMPERATURE



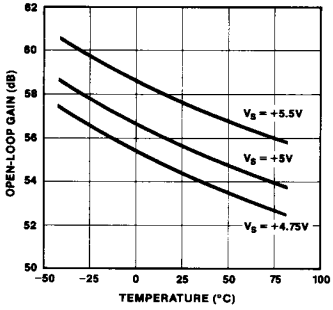
INPUT BIAS CURRENT vs TEMPERATURE



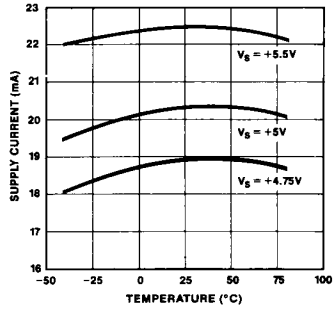
INPUT OFFSET CURRENT vs TEMPERATURE



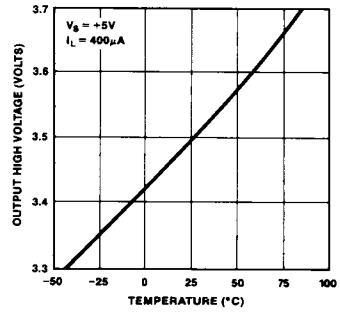
OPEN-LOOP GAIN vs TEMPERATURE



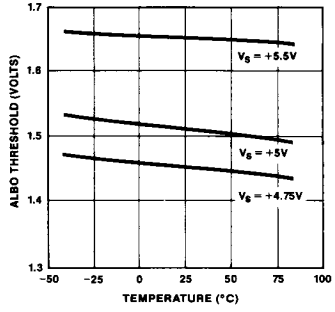
SUPPLY CURRENT vs TEMPERATURE



OUTPUT HIGH VOLTAGE (V_{OHD}) vs TEMPERATURE



ALBO THRESHOLD vs TEMPERATURE



APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The Preamplifier: The LIU-01 contains a differential-input, differential-output preamplifier with a gain-bandwidth product of over 5GHz. Internally, the preamp outputs drive a differential signal into a set of threshold comparators. The external inverting preamp output is normally used only for biasing. The differential inputs and the external noninverting output behave as a conventional op amp. Thus, the preamplifier open-loop gain, A_{VOL}, is specified as $\Delta V_O(+)/\Delta V_{IN}(Diff)$. Preamplifier bandwidth, typically 9MHz, is the frequency at which A_{VOL} has fallen 3dB from its DC value. Unlike a 741-type op amp whose single-pole open-loop gain response provides unity gain stability, the LIU-01's preamplifier has been optimized for maximum gain-bandwidth product and exhibits a multiple-pole gain roll-off beyond 10MHz. The preamp's open-loop gain and phase vs. frequency characteristics are shown in Figure 1. Specific points on these characteristic curves are listed in Table 1. The curves imply that the LIU-01 requires a minimum closed-loop gain of 200 for stability. By providing 46dB of feedback loop attenuation at 20MHz, the preamp will be stable with about 35° of phase margin. To aid in modeling the frequency response of the LIU-01 preamp, Table 2 lists the approximate locations of the first 6 open-loop poles.

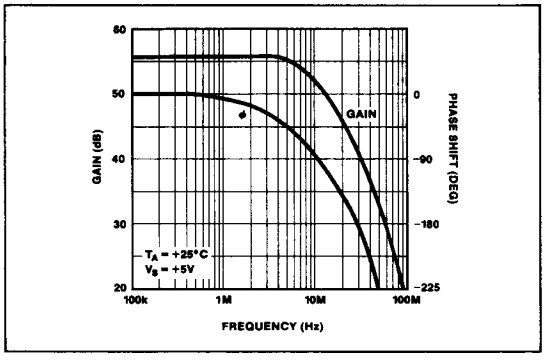


FIGURE 1: *LIU-01 preamplifier gain/phase vs frequency.*

TABLE 1: Typical Preamp Gain/Phase Response

FREQUENCY (MHz)	A_{VOL} (dB)	PHASE (DEG)
1.0	55.7	−8.7
1.544	55.7	−14.0
9.0	52.7	−82.7
20.0	45.8	−145.7
30.0	40.8	−180.8

TABLE 2: LIU-01 Preamp Model

A_{VOL}	R_O	OPEN-LOOP POLES
		12MHz
56dB	50Ω	20MHz
		4 × 135MHz

The LIU-01's preamp is designed to operate around a balanced DC common-mode bias level equal to roughly 50% of the supply voltage on both its inputs and outputs. This allows the outputs to achieve maximum swing when amplifying an AC coupled, bipolar signal. It also produces zero differential preamp output voltage for zero input signal. Operating from a +5V supply, the preamp outputs will balance at approximately +2.5V allowing an output voltage swing of ±1.5V around this bias level as illustrated in Figure 2.

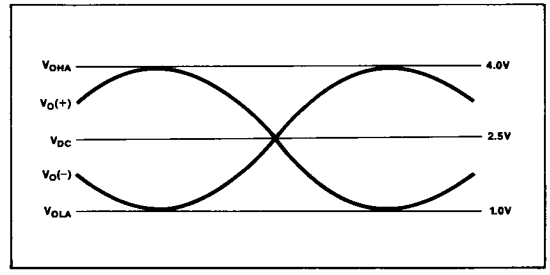


FIGURE 2: *The differential outputs of the LIU-01's preamplifier swing symmetrically around a DC bias point of about 2.5V. $V_O(-)$ is inverted with respect to $V_O(+)$ about this point.*

Figures 3 and 4 show two methods of configuring the preamp to automatically self-bias both the inputs and outputs to an optimum level. The single resistor and capacitor used in Figure 3 extracts the DC average of the inverting output and feeds it back to the noninverting input to establish the input common-mode level. This negative feedback will force the outputs to center their swing around the DC level at which $V_O(Diff) = 0V$. This type of self-biasing is practical only when the preamp is passing a balanced, AC coupled, bipolar signal. If the preamp must preserve the DC level of an unbalanced, unipolar signal, then a self-biasing scheme as is shown in Figure 4 is required. This network sets the input common-mode level by establishing the DC average of both differential outputs. In this way, the input common-mode level will always be that voltage at which $V_O(Diff) = 0V$ regardless of the input signal.

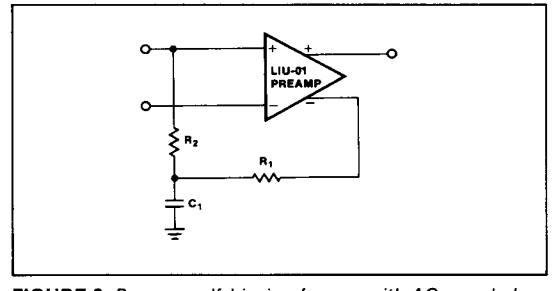


FIGURE 3: *Preamp self-biasing for use with AC coupled, balanced bipolar signals.*

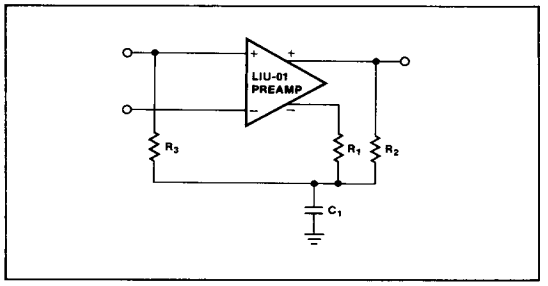


FIGURE 4: *Universal preamplifier self-biasing technique allowing unipolar signal amplification.*

Threshold Comparators: The LIU-01 contains three pairs of threshold comparators to monitor the differential outputs of the preamplifier. Each of the six comparators is set to detect a specific differential preamp output level. Three comparators measure positive differentials and three measure negative differentials. The individual thresholds are labeled as positive and negative Peak, Clock and Data as shown in Figure 5.

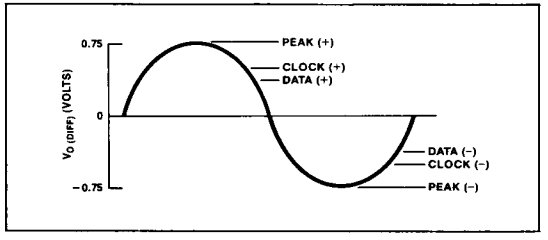


FIGURE 5: *Six threshold comparators detect positive and negative differential preamp output levels.*

The Peak detector outputs are used to perform an AGC-type function (ALBO) to maintain a constant preamp output level. The Clock detector thresholds are set at 71% of the Peak levels. When the Clock thresholds are reached, the comparators send a synchronization pulse to the on-board oscillator to lock its frequency to that of the incoming signal. The Data detector thresholds are set at 50% of the Peak levels for maximum noise immunity. The outputs of these comparators provide the digital data which is clocked into the output latches. A preamp differential output which exceeds the positive Data threshold represents a digital "1" and produces a high output on RPOS. Exceeding the negative Data threshold, also a digital "1", produces a high output on RNEG. A preamp output which exceeds neither Data threshold, a digital "0", produces a low output on both RPOS and RNEG.

ALBO/LOC: Both the ALBO and LOC functions are driven from the Peak threshold detector outputs. The ALBO, Automatic Line Build-Out, circuitry consists of two current driven diodes which act as variable impedance elements enabling the LIU-01 to close an AGC loop around the preamplifier. As a Peak level is detected, a current pulse is sourced into the ALBO diodes. These pulses are averaged to a DC current by an external ALBO filter capacitor. As the current flowing through the diodes increases, their incremental impedance is lowered as described by the exponential I-V curve for a diode-connected NPN transistor shown in Figure 6. The impedance of the NPN transistor emitters which source the current to the ALBO diodes follows an identical curve. Because the bases of these transistors look like an AC short to ground by virtue of the external ALBO filter capacitor, the total AC impedance of each ALBO port looks like the parallel combination of two diodes:

Equation 1 $$R_D \cong \frac{0.026V}{2I_D} + R_{STRAY}$$

where I_D equals the DC current flowing through the diodes and R_{STRAY} represents the stray resistance inherent in the LIU-01, about 3Ω. The longer a Peak level is detected, the greater I_D becomes, lowering R_D. When no Peak levels are detected, the voltage on the ALBO filter capacitor becomes zero, shutting off current to the diodes. Under this condition, the stray pin capacitance of about 3pF will limit maximum ALBO impedance. A 1.544MHz signal will see an effective port ALBO impedance of about 30kΩ. In addition to shutting off the ALBO diodes, the loss of voltage on the ALBO filter will trigger the simple two-transistor comparator that forms the Loss-of-Carrier detector, $\overline{LOC}$, bringing that output low. This signal can be used to warn the digital system receiving the data from the LIU-01 that the incoming signal has fallen below a manageable level and any data output under this condition may be false. If a Peak level is again detected and ALBO filter voltage rises above about 0.7V, $\overline{LOC}$ will return high indicating that the received data is again valid.

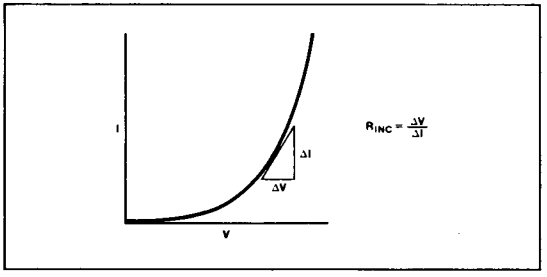


FIGURE 6: *The incremental impedance of the diode-connected NPN transistor used as the ALBO diode is dependent on the DC bias current flowing through it.*

The Oscillator: The LIU-01's on-board oscillator is designed to be free-running at a frequency, f_o, set by an external inductor and capacitor, where $f_o \cong 1/(2\pi\sqrt{LC})$. The phase and exact frequency of the oscillator are synchronized to the incoming data signal by the Clock threshold comparators. Each time the preamplifier's differential output exceeds the Clock thresholds, the comparator's outputs inject a current pulse into the LC tank oscillator aligning its oscillation with the incoming signal. During periods

where no Clock levels are detected by the comparators, the LC tank's oscillation will relax back to its own resonant frequency. An internal comparator is used to square the LC tank's sinusoidal oscillation into a digital level clock. This comparator incorporates a delay function to allow the user to control when the clock edge will reach the output latches. The clock signal then passes through an inverter buffer and is presented as a TTL/CMOS compatible output, RCLK.

The Output Latches: Two edge-triggered, D-type latches provide the TTL/CMOS compatible digital data outputs, RPOS and RNEG, of the LIU-01. The digital information at the outputs of the Data threshold comparators is clocked into these latches on the rising edge of the internal clock. This corresponds to RPOS and RNEG both being updated on the falling edge of the output clock. The latched data outputs will remain stable until they are updated again by the next clock cycle, therefore, the rising edge of the RCLK can be used directly to shift RPOS and RNEG into a shift register or onto a microprocessor bus. The timing of the LIU-01 digital outputs is illustrated in Figure 7. The output architecture of the LIU-01 is directly compatible with the R8070 digital transceiver. Unlike the R8070, the DS2180 digital transceiver clocks data in on the falling edge of the input clock. Using an inverting gate to invert RCLK enables the LIU-01 to shift data into the DS2180.

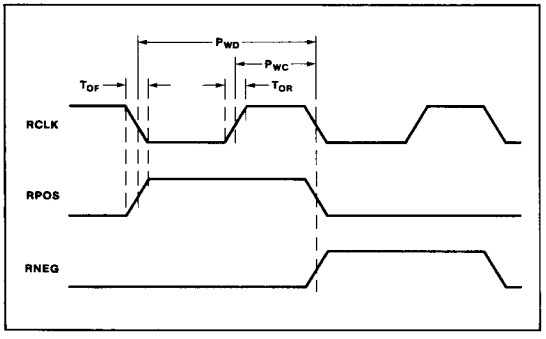


FIGURE 7: *The LIU-01's output timing insures that the data outputs are stable on the rising edge of RCLK. Skew between outputs is typically 10ns.*

DESIGNING WITH THE LIU-01

DESIGNING A WIDEBAND AMPLIFIER

Figure 8 shows a typical configuration using the LIU-01's preamplifier to create a high gain, wideband amplifier. The capacitor C_1 determines the amplifier's low frequency gain roll-off while resistors R_1 and R_2 set the AC closed-loop gain. At DC, the amplifier is in unity gain. A zero at $\omega_1 = 1/(R_2C_1)$ causes the AC gain to rise until a pole is reached at $\omega_2 = 1/(R_1C_1)$. The final value of closed-loop signal gain is equal to:

Equation 2 $$A_{VCL} = \frac{A_{VOL}}{1 + \left(\frac{A_{VOL}R_1}{R_2}\right)}$$

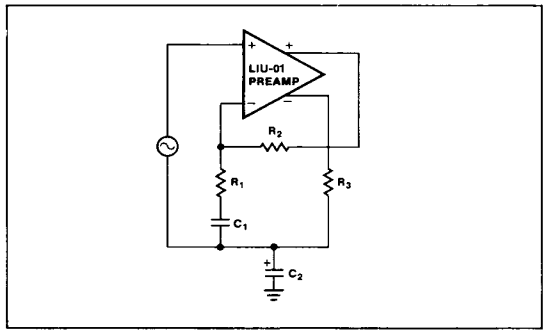


FIGURE 8: *Typical noninverting preamplifier gain configuration with self-biasing.*

To ensure preamp stability, the ratio R_2/R_1 must be a minimum of 200 to a bandwidth of at least 20MHz. Low value resistors should be used for R_2 and R_1 to minimize the effects of stray capacitance in the feedback loop. Since PC board applications exhibit at least 2pF of stray feedback capacitance (equal to about 4kΩ impedance at 20MHz), R_1 should be less than 20Ω.

Because the preamp's differential output voltage is monitored by the internal threshold comparators, any output offset will degrade the symmetry of positive and negative threshold levels. Operating the preamplifier in DC unity gain is instrumental in minimizing the output offset voltage. Offset can be further reduced by balancing the preamp's DC input source impedance. Preamp output loading in the form of feedback and biasing networks should also be balanced to ensure uniform inverting action between the two preamp outputs.

AGC USING THE ALBO DIODES

The variable impedance action of the LIU-01's internal ALBO diodes can be used to create a wide dynamic range AGC loop with the preamplifier as shown in Figure 9. While the preamp operates at a fixed AC gain, the input signal is variably attenuated by the impedance-divider networks of R_1/Z_{D_1} and R_2/Z_{D_2}. As the input signal magnitude increases and the preamp's outputs cross the Peak thresholds, ALBO diode impedance decreases providing more signal attenuation prior to the preamplifier input. If input signal magnitude decreases, diode impedance will increase, reducing signal attenuation. The result is a constant preamp input level creating a constant preamp output amplitude.

The DC blocking capacitors C_1 and C_2 are required to remove from the signal path the DC bias voltage, 0V to 0.8V, of the ALBO diodes. These capacitors also create a frequency dependency by adding a pole/zero pair in the attenuation characteristics of each ALBO diode stage. Figure 10 illustrates the gain vs. frequency response of the first ALBO stage assuming that $R_1 \ll R_2$ and $Z_{D_1} \ll R_1$. As Z_{D_1} changes depending on input signal amplitude, ω_z also changes. At $Z_{D_1} = R_D MAX$, $\omega_z = \omega_p$, and the stage gain equals unity with flat frequency response. At $Z_{D_1} = R_D MIN$, there is maximum separation between ω_z and ω_p and a maximum attenuation equal to approximately Z_{D_1}/R_1. Combining the effects of two ALBO stages allows the programming of two variable-duration poles and a gain ranging from unity to $(Z_{D_1}Z_{D_2})/(R_1R_2)$.

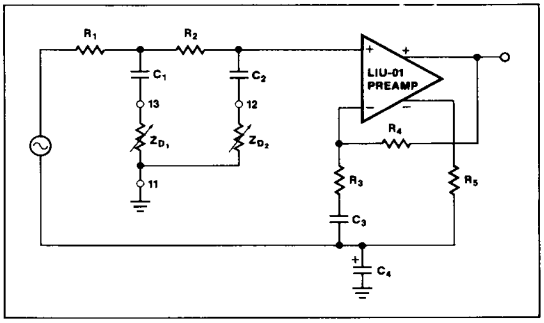


FIGURE 9: *By attenuating the input signal through impedance dividers, the ALBO network simulates the attenuation and frequency characteristics of maximum line length.*

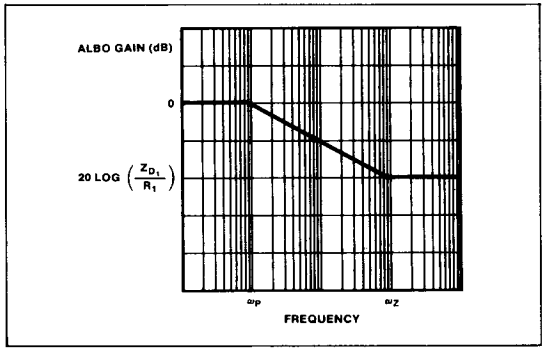


FIGURE 10: *The ALBO impedance creates frequency dependent attenuation.*

DESIGNING THE LC TANK OSCILLATOR

The oscillator on-board the LIU-01 is based on a pulsed LC resonant tank and produces a continuous "square-wave" clock output even in the absence of an incoming data signal. Connected as shown in Figure 11, the oscillator input, Pin 4, oscillates sinusoidally about the 4V oscillator bias, Pin 5. The nominal oscillation frequency, f_o, is given by the formula:

Equation 3 $$f_O = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}$$

which takes into account the effect of the damping resistor, R. The damping resistor is used to reduce the Q of the LC tank where:

Equation 4 $$Q = R\sqrt{\frac{C}{L}}$$

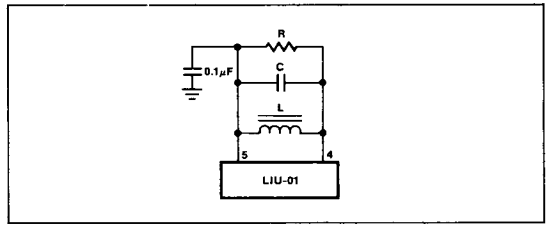


FIGURE 11: *A simple LRC resonant tank oscillator is used by the LIU-01 to recover the encoded clock from an incoming data signal.*

As the Q of the tank is reduced, the oscillation frequency becomes more easily pulled away from f_o by the synchronizing pulses of the Clock threshold comparators. A low Q, 2 to 10, is desirable for the receiver's oscillator because often the incoming data bit stream is timed at a clock rate slightly different from f_o. The bit stream may also contain timing jitter where each data bit or packet of bits arrives with a slightly different clock timing. To ensure that no data bits are missed under these conditions, the LIU-01's oscillator must be flexible enough to track the clock frequency carried within the incoming bit stream. However, if the LIU-01's clock output is to be used to retransmit the recovered data, a higher Q, 10 to 30, is recommended as it greatly reduces transmitted jitter while still remaining flexible enough to tolerate input signal jitter.

The damping resistor also determines the amplitude of the LC tank's oscillation. Assuming R is the only dissipative element in the tank, its value can be calculated as a function of the peak-to-peak oscillation amplitude on Pin 4:

Equation 5 $$R = \frac{\pi V_{p\text{-}p}}{4(720\mu A)}$$

where 720μA equals the oscillator bias current, I_{OSC}. To avoid driving the tank oscillation onto the oscillator clamping diode contained within LIU-01, $V_{p\text{-}p}$ should be set less than $1.2V_{p\text{-}p}$. Letting R = 1.1kΩ sets an optimum oscillation level of $1V_{p\text{-}p}$ for the LIU-01.

The values for L and C can be calculated by choosing the desired Q and f_o and then substituting Equation 4 into Equation 3. The generalized formulas for L and C become:

Equation 6 $$C = \frac{\sqrt{4Q^2 - 1}}{4\pi f_O R}$$

Equation 7 $$L = \frac{CR^2}{Q^2}$$

Note that to maintain a sustained oscillation during the absence of an incoming data bit stream, the Q of the LC tank must be greater than 1.

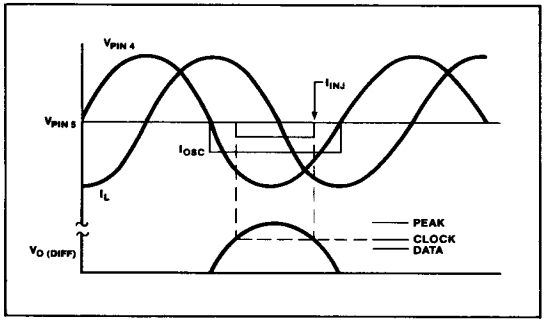


FIGURE 12: *The LC tank is synchronized to the incoming data when the clock detector injection current, I_{INJ}, is centered inside the oscillator's bias current pulse.*

When an incoming data bit stream is of sufficient amplitude to cross the Clock detectors' thresholds, a pulse of current is injected into the tank to synchronize the oscillator frequency to that of the incoming encoded clock. When synchronization is achieved, the various voltage and current waveforms are aligned as shown in Figure 12.

For maximum noise and jitter immunity, the clock edge which latches data into the D-type output latches should appear centered in the period where valid data is present. This active clock edge, generated by the negative-going "zero crossing" of the oscillation voltage on Pin 4, which leads by 90° in phase the center of the synchronized data bit. To accommodate this phenomena, a capacitor is used on Pin 6 to delay the clock edge as it passes to the D-latches. For the LIU-01, the value of this capacitor is calculated as:

Equation 8 $$C_{DELAY} = \frac{1}{5R_D f_O} - \frac{16ns}{R_D}$$

taking into account the value of the internal delay resistor, R_D = 1kΩ nominal, and a small propagation delay associated with the logic gates inside the LIU-01.

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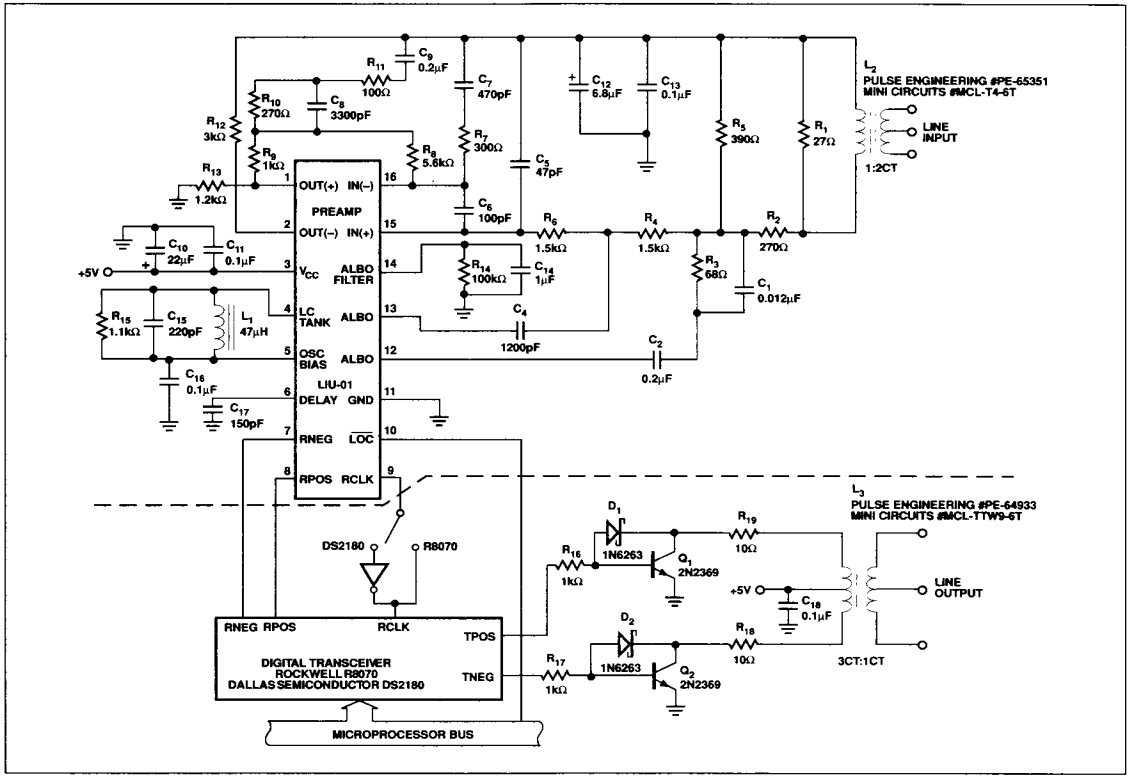

FIGURE 13: *The LIU-01 enables this 4-wire transceiver to recover T1 data at 1.544Mbits/s with an input signal level varying from 0dB to less than –38dB. The ALBO/equalization network is compatible with unshielded #22AWG twisted-pair wire measuring 16pf/ft.*

TYPICAL APPLICATIONS

The circuit shown in Figure 13 is a complete bidirectional 4-wire T1 line interface. The LIU-01's oscillator tank is tuned to recover a 1.544MHz clock with a Q of about 2.4 for excellent jitter tolerance. The line input network, including the preamplifier feedback loop and ALBO diodes, is designed to compensate for the losses and distortion of the #22AWG unshielded twisted-pair wire transmission line whose characteristics of loss vs. frequency vs. length are shown in Figure 14. The goal of the receiver's equalization network is to allow the recovery of 1.544Mb/s T1 format with an input level that varies from 0dB ($6V_{p-p}$) to –38dB ($75mV_{p-p}$) measured at a frequency 1/2 the data rate, 772kHz. At 0 ft. of transmission line, the receiver's incoming signal is at 0dB level with no frequency distortion. By 3000 feet, the signal is at –12dB level and falling at –6dB/octave, single-pole roll-off, between 770kHz and 1.544MHz. At 6000 feet of transmission line, the signal falls to –24dB with a –12dB/octave, double-pole frequency roll-off.

Data rate and transmission line characteristics play an important role in determining the maximum line length from which the LIU-01 can recover data. From Figure 14 it can be seen that #22AWG twisted-pair wire exhibits much less loss and frequency distortion at lower frequencies. Thus, the LIU-01 can recover data from much longer transmission lines if a lower data rate is used. Similarly, using a transmission line with less loss and frequency distortion will allow the LIU-01 to recover higher speed data over longer line lengths.

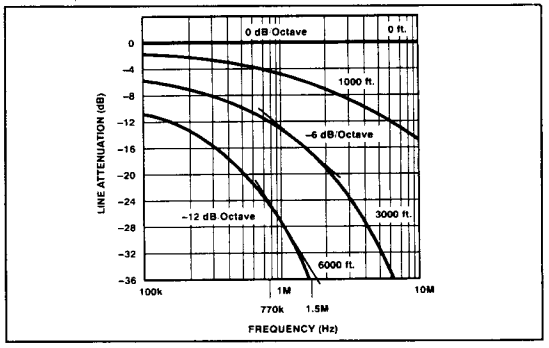

FIGURE 14: *Both line attenuation and frequency distortion become worse as line length increases.*

In the receiver's equalization network, R_7 and C_7 form one zero while R_9, R_{10} and C_8 create a second zero in addition to signal gain. At long transmission line length, this provides a double-zero rise plus gain to equalize the line's double-pole roll-off and attenuation. At short line length, the two ALBO diodes will be driven ON by the increased input signal amplitude and will create two poles in the equalization network as well as attenuation. At 0 ft., the two ALBO poles cancel the two network zeros, matching the line's flat frequency response and reducing the overall network gain to –12dB to accomodate the peak threshold comparators. The oscilloscope photos in Figure 15a and b show both 0dB and –36dB incoming signal levels and the timing of the LIU-01 digital outputs.

While RCLK, RPOS, and RNEG can be connected directly to the receive inputs of the R8070 digital transceiver, an inverter gate must be used on RCLK when interfacing to the DS2180 which clocks in data on the negative edge of the received clock. To complete the line interface, a simple transmitter consisting of Q_1, Q_2, and their Schottky diode clamps is driven through R_{16} and R_{17} directly from the TPOS and TNEG outputs of the digital transceiver, as shown in Figure 13.

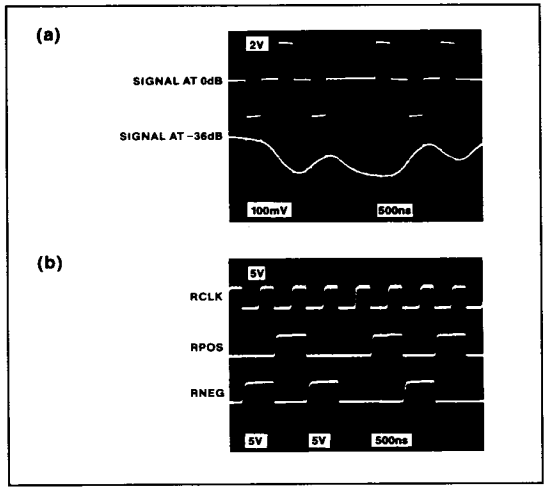

FIGURE 15: *The LIU-01 receives the signal, as shown in (a), ranging in amplitude from 0dB to –36dB and produces TTL/CMOS compatible digital outputs (b).*

When designing a system with the LIU-01 receiver, every precaution should be taken to minimize the exposure of the sensitive analog circuit inputs to high frequency noise. Both the ground plane and the signal traces should be placed on the component side of the printed circuit board with the ground trace used to isolate the analog inputs from the digital outputs. All digital circuitry should be placed well away from the analog inputs.

Ideally though, the LIU-01's digital outputs should be connected directly to the receiving digital system by the shortest possible path to avoid the additional stray loading and noise radiation of long digital traces. If more than two digital inputs are to be driven by any of the LIU-01's outputs, or if the output traces are over 3 inches long, it is recommended that a CMOS 74HCT08 placed adjacent to the LIU-01 be used to buffer its outputs.

The oscilloscope photos in Figure 16 show the LIU-01's preamplifier output, pin #1, as it receives data patterns of a) 1-of-9 and b) QRSS at the end of 6000 ft. of transmission line. The nearly ideal equalization can be seen as the distinct half-sinusoidal pulses are recreated with no appreciable overshoot or undershoot resulting in the "wide-open" eye-pattern with better than 10dB interference margin, or signal-to-noise ratio, capability. With careful circuit layout, digital clock noise has been held to only about 50mV high frequency spikes. This same circuit can receive data without error from 0 ft. up to 9000 ft. of #22AWG transmission line.

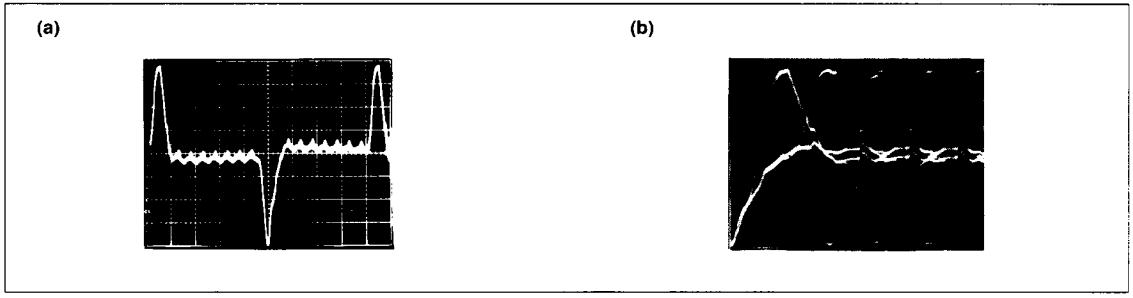

FIGURE 16: *The LIU-01's preamplifier output, pin #1, should produce half-sinusoidal pulses of recovered data signal when properly equalized for the transmission line. The circuit of Figure 13 has excellent response as shown here receiving at 6000 ft. a 1-of-9 pattern, a, and a QRSS pattern, b.*

In some applications, such as passive transmission line monitoring, the receiver must not terminate the line, but instead appears as a very high impedence load. To accomodate this need and still provide a low source impedence to the LIU-01, a buffer amplifier can be used as shown in Figure 17. The JFET input of BUF-03 presents a very high impedence to the transmission line while driving the equalization network with less than 10Ω output impedence at 1.544MHz. This buffering technique works well when analog supply voltages of at least ±8 volts are available to power the buffer. Figure 18 shows another technique for buffering the LIU-01 from the transmission line using only a single +5 volt supply. The emitter-follower transistor, Q1, appears to the line to be about a 50kΩ impedence at 1.544MHz.

With a nominal collector current of 4mA set by the 500Ω emitter resistor, Q1 drives the LIU-01's network with about 8Ω output impedence. The AC coupling capacitor, C_C, is required to remove the DC level shift of Q1's base-emitter voltage drop.

In Figure 19, the LIU-01 is used as an in-line monitor allowing data and clock to be read from the transmission line while simultaneously retransmitting a regenerated 0dB T1 signal. The data outputs RPOS and RNEG are logically recombined with RCLK by the 74HC00 which also acts directly as output line driver. The Schottky diode, D_1, along with R_1 and C_1 stretch the duty cycle of RCLK from a nominal 43% to 50% as required for T1 transmission.

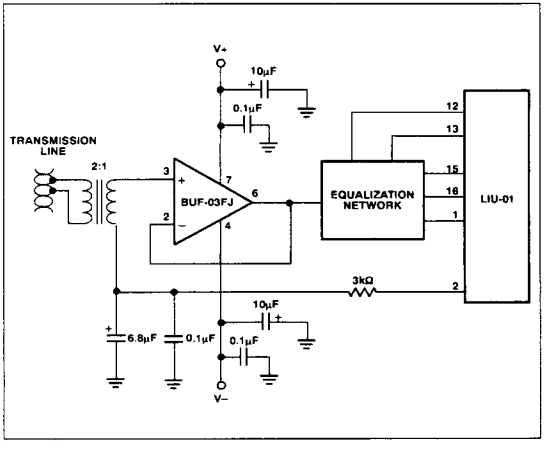

FIGURE 17: *The OP-42 provides high impedance input to the equalization network without raising the source impedance to the LIU-01 preamplifier.*

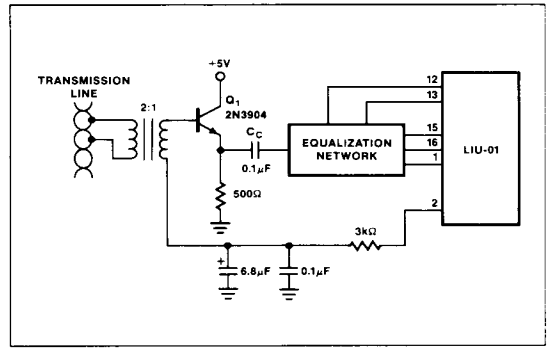

FIGURE 18: *Emitter-follower Q_1 acts as buffer between the equalization network and the transmission line while operating from only a +5V supply.*

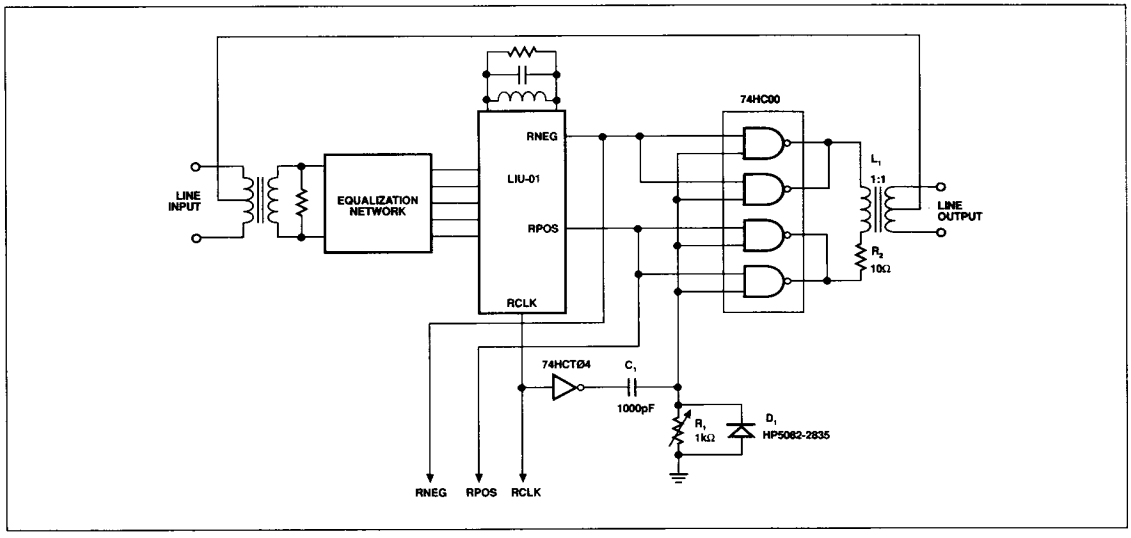

FIGURE 19: *The LIU-01 acts an in-line monitor/repeater using 74HC00 as an output driver. D_1, R_1, and C_1 stretch the duty cycle of RCLK to 50%. The value of R_1 depends on the operating data rate.*