L9218A/G Low-Cost Line Interface

Features

- Basic forward battery only SLIC functionality at a low cost
- Pin compatible with Agere Systems Inc. L9219 and L9217 SLIC
- Low active power (typical 138 mW during on-hook transmission)
- Low-power scan mode for low-power, on-hook power dissipation (59 mW typical)
- Minimal external components
- Distortion-free, on-hook transmission
- Convenient operating states:
  - — Forward battery low current limit
  - — Forward battery high current limit
  - — Low-power scan
  - — Disconnect (high impedance)
- Adjustable supervision functions:
  - — Off-hook detector with hysteresis
  - — Ring trip detector
- Logic controlled high and low current limit
- Two gain options to optimize the codec interface
- Thermal protection with thermal shutdown indication

Description

This general-purpose electronic subscriber loop interface circuit (SLIC) is optimized for low cost, while still providing a satisfactory set of features.

The L9218 is pin-for-pin compatible with the Agere L9219 and L9217 SLICs.

The L9218 requires a 5 V power supply and single battery to operate. This is a forward battery only device. Additionally, a low-power scan mode, wherein all circuitry except the off-hook supervision is shut down to conserve power, is available.

Via the logic inputs, a low or high current limit may be selected. The low value is set via a single external resistor, and the high value is 1.4 times the low value.

Device overhead is fixed and is adequate for 3.14 dBm into 900 Ω of on-hook transmission.

Both the loop supervision and ring trip supervision functions are offered with user-controlled thresholds via external resistors.

The L9218 is offered with a receive gain that is optimized for interface to a first-generation type codec (L9218A). It is also offered with a gain option that is optimized for interface to a third- or fourth-generation type codec (L9218G). In both cases, minimizing external components required at this interface. In the receive direction, the device may be dc-coupled to a third-generation codec. No dc blocking capacitors are needed.

Data control is via a parallel data control scheme.

The device is available in a 28-pin PLCC package. It is built by using a 90 V complementary bipolar (CBIC) process.

Table of Contents

Contents — Page

Figures — Page

Tables — Page

Description (continued)

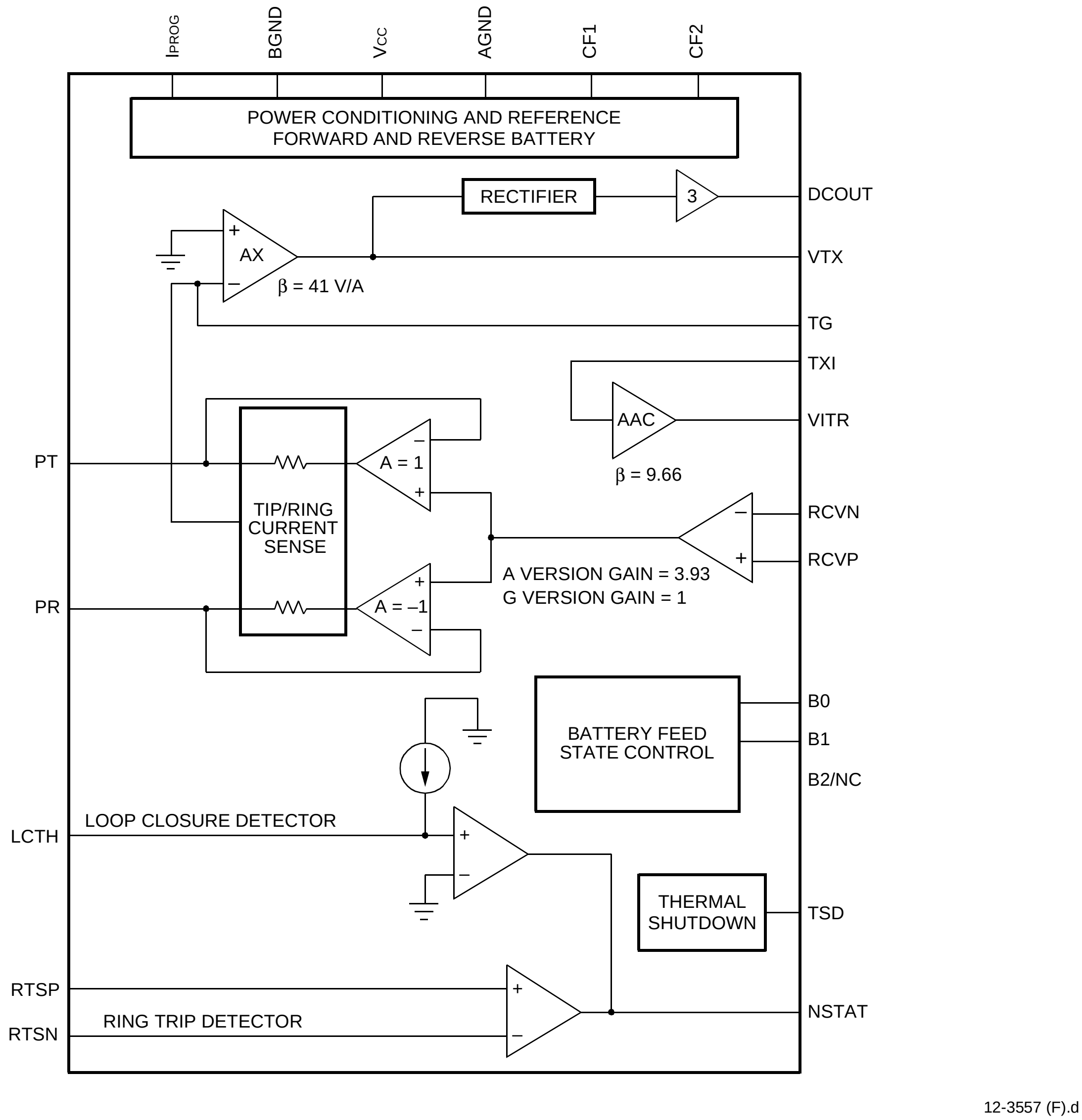


Figure 1. Functional Diagram

Pin Information

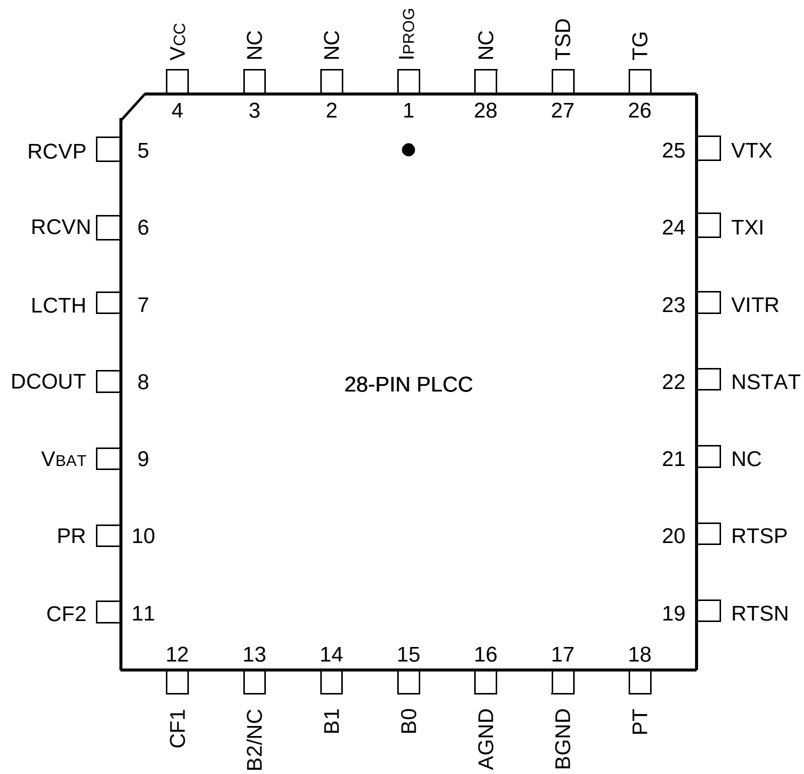


Figure 2. 28-Pin PLCC

Table 1. Pin Descriptions

PLCC	Symbol	Type	Description
1	IPROG	I	**Current-Limit Program Input.** A resistor to DCOUT sets the dc current limit of the device.
2	NC	—	**No Connect.**
3	NC	—	**No Connect.**
4	VCC	—	**5 V Power Supply.**
5	RCVP	I	**Receive ac Signal Input (Noninverting).** This high-impedance input controls the ac differential voltage on tip and ring.
6	RCVN	I	**Receive ac Signal Input (Inverting).** This high-impedance input controls the ac differential voltage on tip and ring.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

PLCC	Symbol	Type	Description
7	LCTH	I	**Loop Closure Threshold Input.** Connect a resistor to VTX to set off-hook threshold.
8	DCOUT	O	**dc Output Voltage.** This output is a voltage that is directly proportional to the absolute value of the differential tip/ring current.
9	VBAT	—	**Battery Supply.** Negative high-voltage power supply.
10	PR	I/O	**Protected Ring.** The output of the ring driver amplifier and input to loop sensing circuitry. Connect to the loop through overvoltage protection.
11	CF2	—	**Filter Capacitor 2.** Connect a 0.1 µF capacitor from this pin to AGND.
12	CF1	—	**Filter Capacitor 1.** Connect a 0.47 µF capacitor from this pin to pin CF2.
13	B2/NC	—	**Dummy Pin.** Used for exact pin-for-pin compatibility with L9219. There is no physical connection to this pin, however, it may be connected to the B2 control latch to get an exact PWB footprint match with L9219.
14	B1	I	**State Control Input.** B0 and B1 determine the state of the SLIC. See Table 2. Pin B1 has an internal pull-down.
15	B0	I	**State Control Input.** B0 and B1 determine the state of the SLIC. See Table 2. Pin B0 has an internal pull-down.
16	AGND	—	**Analog Signal Ground.**
17	BGND	—	**Battery Ground.** Ground return for the battery supply.
18	PT	I/O	**Protected Tip.** The output of the tip driver amplifier and input to loop-sensing circuitry. Connect to loop through overvoltage protection.
19	RTSN	I	**Ring Trip Sense Negative.** Connect this pin to the ringing generator signal through a high-value resistor.
20	RTSP	I	**Ring Trip Sense Positive.** Connect this pin to the ring relay and the ringer series resistor through a high-value resistor.
21	NC	—	**No Connect.**
22	NSTAT	O	**Loop Detector Output/Ring Trip Detector Output.** When low, this logic output indicates that an off-hook condition exists or that ringing is tripped.
23	VITR	O	**Transmit ac Output Voltage.** This output is a voltage that is directly proportional to the differential tip/ring current.
24	TXI	—	**ac/dc Separation.** Connect a 0.1 µF capacitor from this point to VTX.
25	VTX	O	**Transmit ac/dc Output Voltage.** This output is a voltage that is directly proportional to the differential tip/ring current.
26	TG	—	**Transmit Gain.** Connect an 8.06 kΩ from TG to VTX to set the transmit gain of the SLIC.
27	TSD	O	**Thermal Shutdown.** When high, this logic output indicates the device is in thermal shutdown.
28	NC	—	**No Connect.**

Functional Description

Table 2. Input State Coding

B0	B1	State/Definition
1	1	**Powerup, Forward Battery.** Normal talk and battery feed state. Pin PT is positive with respect to PR. On-hook transmission is enabled. Low current limit is selected.
1	0	**Powerup, Forward Battery.** Normal talk and battery feed state. Pin PT is positive with respect to PR. On-hook transmission is enabled. High current limit is selected.
0	0	**Disconnect.** The tip and ring amplifiers are turned off, and the SLIC goes to a high-impedance state (>100 kΩ). Supervision outputs read on hook. Device will power up in this state.
0	1	**Low-Power Scan.** Except for off-hook detection, all circuits are shut down to conserve power. Pin PT is positive with respect to pin PR. On-hook transmission is disabled.

Table 3. Supervision Coding

NSTAT	TSD
0 = off-hook or ring trip. 1 = on-hook and no ring trip.	0 = Normal device operation. 1 = Device is in thermal shutdown.

Absolute Maximum Ratings (at T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
5 V Power Supply	V_{CC}	—	—	7.0	V
Battery (talking) Supply	V_{BAT}	—	—	–75	V
Logic Input Voltage	—	–0.5	—	7.0	V
Analog Input Voltage	—	–7.0	—	7.0	V
Maximum Junction Temperature	T_J	150	—	—	°C
Storage Temperature Range	T_{stg}	–40	—	125	°C
Relative Humidity Range	R_H	5	—	95	%
Ground Potential Difference (BGND to AGND)	—	—	±3	—	V
PT or PR Fault Voltage (dc)	V_{PT}, V_{PR}	V_{BAT} – 5	—	3	V
PT or PR Fault Voltage (10 x 1000 µs)	V_{PT}, V_{PR}	V_{BAT} – 15	—	15	V
Current into Ring Trip Inputs	I_{RTSP}, I_{RTSN}	—	±240	—	µA

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. Some of the known examples of conditions that cause such potentials during powerup are the following:

1. An inductor connected to tip and ring can force an overvoltage on V_{BAT} through the protection devices if the V_{BAT} connection chatters.
2. Inductance in the V_{BAT} lead could resonate with the V_{BAT} filter capacitor to cause a destructive overvoltage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature	–40	—	85	°C
V_{CC} Supply Voltage	4.75	5.0	5.25	V
V_{BAT} Supply Voltage	–24	–48	–70	V

Electrical Characteristics

Minimum and maximum values are testing requirements in the temperature range of 25 °C to 85 °C and battery range of –24 V to –70 V. These minimum and maximum values are guaranteed to –40 °C based on component simulations and design verification of samples, but devices are not tested to –40 °C in production. The test circuit shown in Figure 4 is used, unless otherwise noted. Positive currents flow into the device.

Typical values are characteristics of the device design at 25 °C based on engineering evaluations and are not part of the test requirements. Supply values used for typical characterization are V_{CC} = 5.0 V, V_{BAT} = –48 V, unless otherwise noted.

Table 4. Power Supply

Parameter	Min	Typ	Max	Unit
Power Supply—Powerup, No Loop Current:				
I_{CC}	—	4.6	5.6	mA
I_{BAT} (V_{BAT} = –48 V)	—	–2.4	–2.7	mA
Power Dissipation (V_{BAT} = –48 V)	—	138	158	mW
Power Supply—Scan, No Loop Current:				
I_{CC}	—	2.8	3.8	mA
I_{BAT} (V_{BAT} = –48 V)	—	–0.8	–1.0	mA
Power Dissipation (V_{BAT} = –48 V)	—	52	67	mW
Power Supply—Disconnect, No Loop Current:				
I_{CC}	—	1.6	—	mA
I_{BAT} (V_{BAT} = –48 V)	—	–0.12	—	mA
Power Dissipation (V_{BAT} = –48 V)	—	14	—	mW
Power Supply Rejection 500 Hz to 3 kHz (See Figure 5 and Figure 6)[1]:				
V_{CC}	30	—	—	dB
V_{BAT}	40	—	—	dB
Thermal Protection Shutdown (T_{jc})[3]	150	165	—	°C
Thermal Resistance, Junction to Ambient (θ_{JA})[2, 3]:				
Natural Convection 2S2P Board	—	30	—	°C/W
Natural Convection 2S0P Board	—	43	—	°C/W
Wind Tunnel 100 Linear Feet per Minute (LFPM) 2S2P Board	—	27	—	°C/W
Wind Tunnel 100 Linear Feet per Minute (LFPM) 2S0P Board	—	36	—	°C/W

1. This parameter is not tested in production. It is guaranteed by design and device characterization.
2. Careful thermal design as a function of maximum battery, loop length, maximum ambient temperature package thermal resistance, airflow, PCB board layers, and other related parameters must ensure that thermal shutdown temperature is not exceeded under normal use conditions.
3. Airflow, PCB board layers, and other factors can greatly affect this parameter.

Electrical Characteristics (continued)

Table 5. 2-Wire Port

Parameter	Min	Typ	Max	Unit
Tip or Ring Drive Current = dc + Longitudinal + Signal Currents	80	—	—	mA
Signal Current	15	—	—	mArms
Longitudinal Current Capability per Wire[1]	8.5	15	—	mArms
dc Loop Current Limit[2]: Allowed Range Including Tolerance[3] Accuracy (R_{LOOP} = 100 Ω, V_{BAT} = –48 V)	 15 —	 — ±5	 45 —	 mA %
Powerup Open Loop Voltage Levels: Common-mode Voltage Differential Voltage V_{BAT} = –48 V[4] (Gain = 2) Differential Voltage V_{BAT} = –48 V[4] (Gain = 7.86)	 — |V_{BAT} + 7.5| |V_{BAT} + 8.0|	 V_{BAT}/2 |V_{BAT} + 6.5| |V_{BAT} + 6.5|	 — |V_{BAT} + 5.9| |V_{BAT} + 5.9|	 V V V
Disconnect State: Leakage	 —	 10	 150	 µA
dc Feed Resistance (for I_{LOOP} below regulation level) (does not include protection resistor)	—	80	100	Ω
Loop Resistance Range (–3.17 dBm overload into 900 Ω; not including protection): I_{LOOP} = 20 mA at V_{BAT} = –48 V	 1800	 —	 —	 Ω
Longitudinal to Metallic Balance—*IEEE*® Std. 455 (See Figure 7)[5]: 200 Hz to 3400 Hz	 58	 61	 —	 dB
Metallic to Longitudinal Balance (open loop): 200 Hz to 4 kHz	 40	 —	 —	 dB
RFI Rejection (See Figure 8)[3], 0.5 Vrms, 50 Ω Source, 30% AM Mod 1 kHz: 500 kHz to 100 MHz	— —	— –55	— –45	— dBV

1. The longitudinal current is independent of dc loop current.
2. Current-limit I_{LIM} is programmed by a resistor, R_{PROG}, from pin I_{PROG} to DCOUT. I_{LIM} is specified at the loop resistance where current limiting begins (see Figure 13).
3. This parameter is not tested in production. It is guaranteed by design and device characterization.
4. Specification is reduced to |V_{BAT1} + 10.5 V| minimum when V_{BAT1} = –70 V at 85 °C.
5. Longitudinal balance of circuit card will depend on loop series protection resistor matching and magnitude. More information is available in the Applications section of this document.

Electrical Characteristics (continued)

Table 6. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
Differential PT/PR Current Sense (DCOUT):				
Gain (PT/PR to DCOUT)	121	125	129	V/A
Offset Voltage at I_{LOOP} = 0	–100	—	100	mV
Loop Closure Detector Threshold (R_{LCTH} = 22.1 kΩ)[1]:				
On- to Off-hook Threshold (scan mode)	8.8	—	13.6	mA
Off- to On-hook Threshold (active mode)	6.0	—	10.2	mA
Ring Trip Comparator:				
Input Offset Voltage[2]	—	±10	—	mV
Internal Voltage Source	–9.1	–8.6	–8.1	V
Current at Input RTSP[3]	I_N – 0.5	I_N	I_N + 0.6	µA
RCVN, RCVP:				
Input Bias Current	—	–0.2	–1	µA
Input Resistance	—	1	—	MΩ

1. Loop closure threshold is programmed by resistor R_{LCTH} from pin LCTH to pin DCOUT. The programming equation or relationship between off-hook threshold and resistor value is different for active mode versus scan mode (see Applications section for more details).
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. I_N is the sourcing current at RTSN. Guaranteed if I_N is within 5 µA to 30 µA.

Electrical Characteristics (continued)

Table 7. ac Feed Characteristics

Parameter	Min	Typ	Max	Unit
ac Termination Impedance[1]	150	—	1300	Ω
Longitudinal Impedance at PT/PR[2]	—	0	—	Ω
Total Harmonic Distortion—200 Hz to 4 kHz[2]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain, f = 1 kHz (PT/PR to VITR) (current limit)	–391	–403	–415	V/A
L9218A, Open Loop:				
Receive + Gain, f = 1 kHz (RCVP to PT/PR)[3]	7.62	7.86	8.09	—
Receive – Gain, f = 1 kHz (RCVN to PT/PR)[3]	–7.62	–7.86	–8.09	—
L9218G, Open Loop:				
Receive + Gain, f = 1 kHz (RCVP to PT/PR)[4]	1.94	2.00	2.06	—
Receive – Gain, f = 1 kHz (RCVN to PT/PR)[4]	–1.94	–2.00	–2.06	—
Gain vs. Frequency (transmit and receive) (600 Ω termination; reference 1 kHz[2]):				
200 Hz to 300 Hz	–1.00	0.0	0.05	dB
300 Hz to 3.4 kHz	–0.3	0.0	0.05	dB
3.4 kHz to 16 kHz	–3.0	–0.1	0.3	dB
16 kHz to 266 kHz	—	—	2.5	dB
Gain vs. Level (transmit and receive)(reference 0 dBV[2]):				
–55 dB to +3 dB	–0.05	0	0.05	dB
2-Wire Idle-channel Noise (600 Ω termination):				
Psophometric[2]	—	–87	–77	dBmp
C-message	—	2	12	dBrnC
3 kHz Flat[2]	—	10	20	dBrn
Transmit Idle-channel Noise:				
Psophometric[2]	—	–82	–77	dBmp
C-message	—	7	12	dBrnC
3 kHz Flat[2]	—	15	20	dBrn

1. With a first-generation codec, this parameter is set by external components. Any complex impedance R1 + R2 || C between 150 Ω and 1300 Ω can be synthesized. With a third-generation codec, this parameter is set by a codec or by a combination of a codec and an external network.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Use this gain option with a first-generation or third-generation codec.
4. Use this gain option with an Agere third-generation codec.

Electrical Characteristics (continued)

Table 8. Logic Inputs and Outputs

All outputs are open collectors with internal, 30 kΩ pull-down resistor. Input pins have internal pull-down or some way to power up in disconnect state.

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level (permissible range)	V_{IL}	–0.5	0.4	0.7	V
High Level (permissible range)	V_{IH}	2.0	2.4	V_{CC}	V
Input Currents:					
Low Level (V_{CC} = 5.25 V, V_I = 0.4 V)	I_{IL}	0	+4	+10	µA
High Level (V_{CC} = 5.25 V, V_I = 2.4 V)	I_{IH}	+10	+24	+50	µA
Output Voltages (open collector with internal pull-up resistor):					
Low Level (V_{CC} = 4.75 V, I_{OL} = 200 µA)	V_{OL}	0	0.2	0.4	V
High Level (V_{CC} = 4.75 V, I_{OH} = –20 µA)	V_{OH}	2.4	—	V_{CC}	V

Ring Trip Requirements

- Ringing signal:
  - — Voltage, minimum 35 Vrms, maximum 100 Vrms.
  - — Frequency, 17 Hz to 33 Hz.
  - — Crest factor, 1.2 to 1.6.
- Ring trip:
  - — ≤100 ms (typical).
- Pretrip:
  - — The circuits in Figure 3 will not cause ring trip.

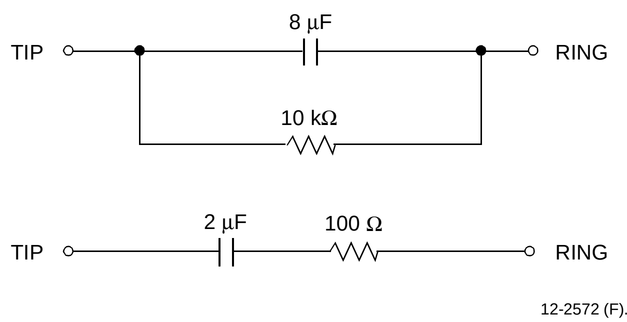


Figure 3. Ring Trip Circuits

Test Configurations

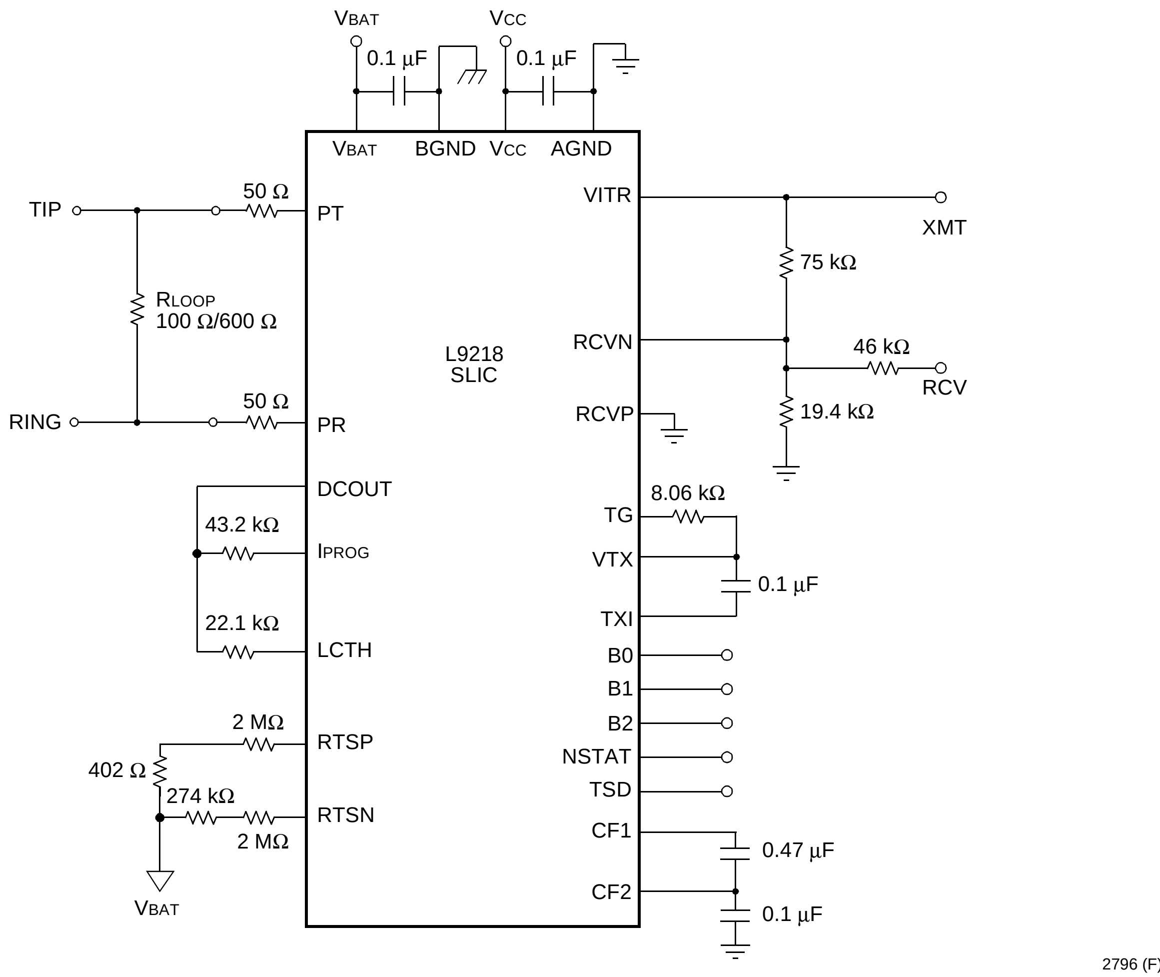


Figure 4. L9218 Basic Test Circuit

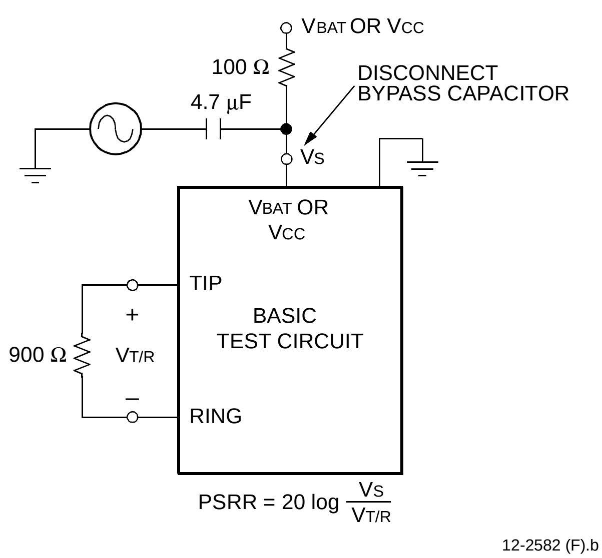


Figure 5. Metallic PSRR

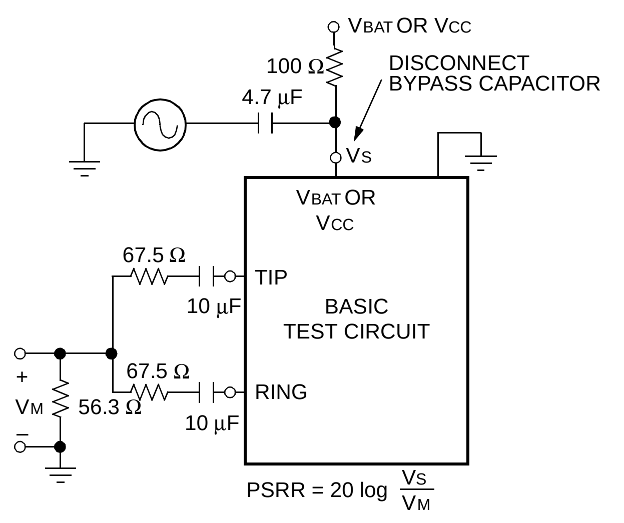


Figure 6. Longitudinal PSRR

Test Configurations (continued)

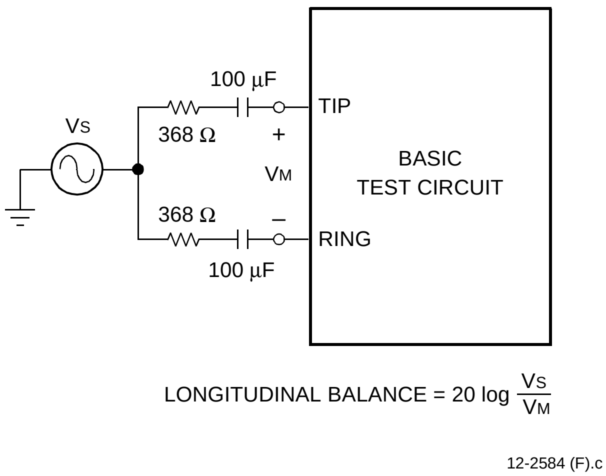
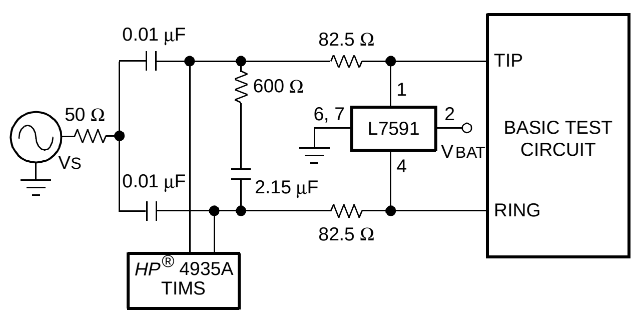


Figure 7. Longitudinal Balance



VS = 0.5 Vrms 30% AM 1 kHz modulation,
f = 500 kHz—1 MHz
device in powerup mode, 600 Ω termination.

Figure 8. RFI Rejection

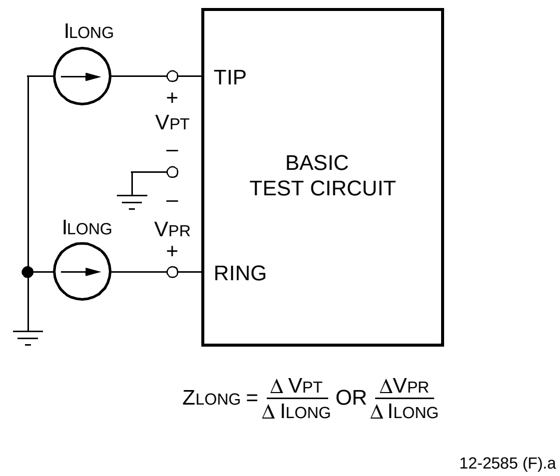


Figure 9. Longitudinal Impedance

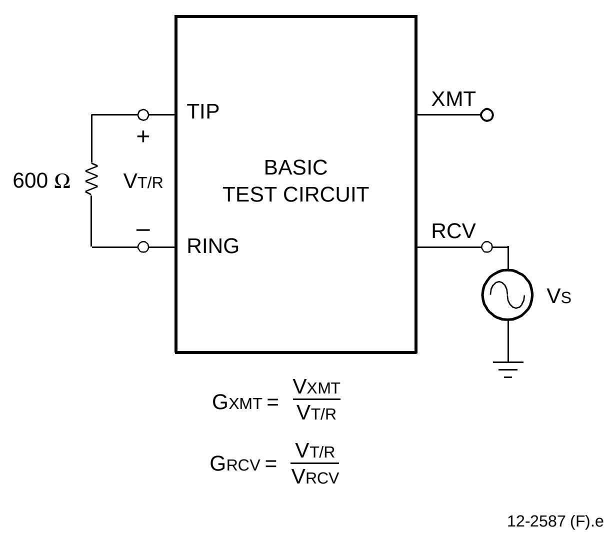


Figure 10. ac Gains

Applications

A basic loop start reference circuit, using bused ringing with the L9218 SLIC and the T7504 first-generation codec, is shown in Figure 11. This circuit is designed for a 200 Ω + 680 Ω || 0.1 µF complex termination impedance and transhybrid. Transmit gain is set at 0 dBm and receive gain is set at –7 dBm.

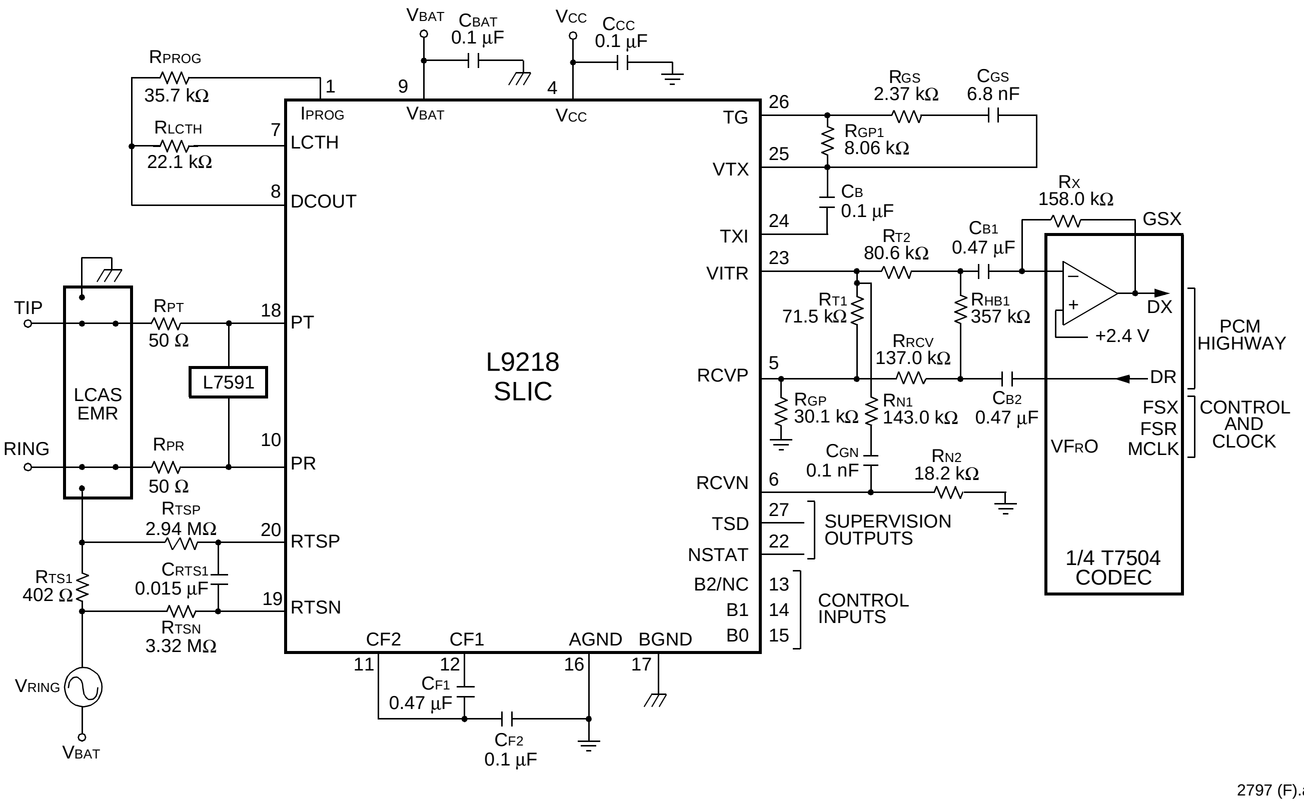


Figure 11. Basic Loop Start Application Circuit Using T7504-Type Codec

Table 9 shows the design parameters of the application circuit shown in Figure 11. Components that are adjusted to program these values are also shown.

Table 9. 200 Ω + 680 Ω || 0.1 µF First-Generation Codec Design Parameters

Design Parameter	Parameter Value	Components Adjusted
Loop Closure Threshold	10 mA	R_{LCTH}
dc Loop Current Limit	20 mA	R_{PROG}
2-wire Signal Overload Level	3.14 dBm	—
ac Termination Impedance	200 Ω + 680 Ω || 0.1 µF	R_{T1}, R_{GP}, R_{RCV}, R_{GP1}, R_{GS}, C_{GS}
Hybrid Balance Line Impedance	200 Ω + 680 Ω || 0.1 µF	R_{HB1}
Transmit Gain	0 dBm	R_{T2}, R_X, R_{N1}, R_{N2}, C_N
Receive Gain	–7 dBm	R_{RCV}, R_{GP}, R_{T1}

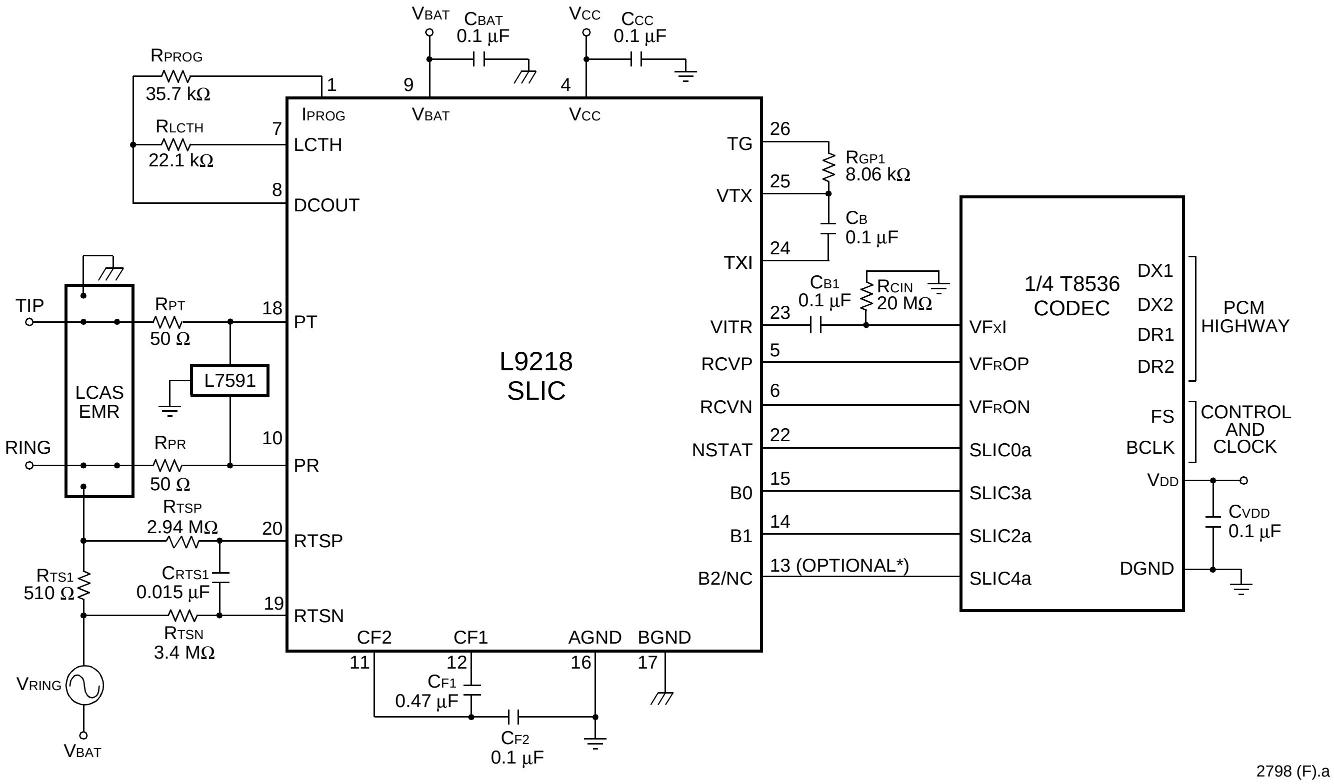
Applications (continued)

Table 10. Parts List for Loop Start Application Circuit Using T7504-Type Codec

Name	Value	Function
Integrated Circuits		
SLIC	L9218	Subscriber loop interface circuit (SLIC).
Protector	Agere L7591	Secondary protection.
Ringing Relay	Agere L7581/2/3 or EMR	Switches ringing signals.
Codec	T7504	First-generation codec.
Overvoltage Protection		
R_{PT}	50 Ω, Fusible	Protection resistor.
R_{PR}	50 Ω, Fusible	Protection resistor.
Power Supply		
C_{BAT1}	0.1 µF, 20%, 100 V	V_{BAT} filter capacitor.
C_{CC}	0.1 µF, 20%, 10 V	V_{CC} filter capacitor.
C_{F1}	0.47 µF, 20%, 100 V	With C_{F2}, improves idle-channel noise.
C_{F2}	0.1 µF, 20%, 100 V	With C_{F1}, improves idle-channel noise.
dc Profile		
R_{PROG}	35.7 kΩ, 1%, 1/16 W	Sets dc loop current limit.
ac Characteristics		
C_{B1}	0.47 µF, 20%, 10 V	ac/dc separation capacitor.
C_{B2}	0.47 µF, 20%, 10 V	ac/dc separation capacitor.
R_{T1}	71.5 kΩ, 1%, 1/16 W	With R_{GP} and R_{RCV}, sets ac termination impedance.
R_{RCV}	137 kΩ, 1%, 1/16 W	With R_{GP} and R_{T1}, sets receive gain.
R_{GP}	30.1 kΩ, 1%, 1/16 W	With R_{T1} and R_{RCV}, sets ac termination impedance and receive gain.
R_{T2}	80.6 kΩ, 1%, 1/16 W	With R_X, sets transmit gain in codec.
R_X	158 kΩ, 1%, 1/16 W	With R_{T2}, sets transmit gain in codec.
R_{HB1}	357 kΩ, 1%, 1/16 W	Sets hybrid balance.
C_{GS}	6.8 nF, 10%, 10 V	With R_{GS}, provides gain shaping for termination impedance matching.
R_{GS}	2.37 kΩ, 1%, 1/16 W	With C_{GS}, provides gain shaping for termination impedance matching.
R_{GP1}	8.06 kΩ, 1%, 1/16 W	Sets transmit gain of SLIC.
C_N	0.1 nF, 20%, 10 V	With R_{N1} and R_{N2} high frequency compensation.
R_{N1}	143 kΩ, 1%, 1/16 W	With C_N and R_{N2} high frequency compensation.
R_{N2}	18.2 kΩ, 1%, 1/16 W	With R_{N1} and C_N high frequency compensation.
Supervision		
R_{LCTH}	22.1 kΩ, 1%, 1/16 W	Sets loop closure (off-hook) threshold.
R_{TS1}	402 Ω, 5%, 2 W	Ringing source series resistor.
C_{RTS1}	0.015 µF, 20%, 10 V	With R_{TSN}, R_{TSP}, forms filter pole.
R_{TSN}	3.32 MΩ, 1%, 1/16 W	With R_{TSP}, sets threshold.
R_{TSP}	2.94 MΩ, 1%, 1/16 W	With C_{RTS1}, R_{TSN}, sets threshold.

Applications (continued)

A basic loop start reference circuit, using bused ringing with the L9218 SLIC and the T8536 third-generation codec, is shown in Figure 12.



* Optional nonfunctional connection for exact footprint match with L9219.

Figure 12. Basic Loop Start Application Circuit Using T8536-Type Codec

Applications (continued)

Table 11. Parts List for Loop Start Application Circuit Using T8536-Type Codec

Name	Value	Function
Integrated Circuits		
SLIC	L9218	Subscriber loop interface circuit (SLIC).
Protector	Agere L7591	Secondary protection.
Ringing Relay	Agere L7581/2/3 or EMR	Switches ringing signals.
Codec	T8536	Third-generation codec.
Overvoltage Protection		
R_{PT}	50 Ω, Fusible	Protection resistor.
R_{PR}	50 Ω, Fusible	Protection resistor.
Power Supply		
C_{BAT1}	0.1 µF, 20%, 100 V	V_{BAT} filter capacitor.
C_{CC}	0.1 µF, 20%, 10 V	V_{CC} filter capacitor.
C_{F1}	0.47 µF, 20%, 100 V	With C_{F2}, improves idle-channel noise.
C_{F2}	0.1 µF, 20%, 100 V	With C_{F1}, improves idle-channel noise.
dc Profile		
R_{PROG}	35.7 kΩ, 1%, 1/16 W	Sets dc loop current limit.
ac Characteristics		
C_{B3}	0.1 µF, 20%, 10 V	ac/dc separation capacitor.
R_{GP1}	8.06 kΩ, 1%, 1/16 W	Sets transmit gain of SLIC.
R_{CIN}	20 MΩ, 5%, 1/16 W	dc bias.
Supervision		
R_{LCTH}	22.1 kΩ, 1%, 1/16 W	Sets loop closure (off-hook) threshold.
R_{TS1}	510 Ω, 5%, 2 W	Ringing source series resistor.
C_{RTS1}	0.015 µF, 20%, 10 V	With R_{TSN} and R_{TSP}, forms second 2 Hz filter pole.
R_{TSN}	3.4 MΩ, 1%, 1/16 W	With R_{TSP}, sets threshold.
R_{TSP}	2.94 MΩ, 1%, 1/16 W	With R_{TSN}, sets threshold.

Applications (continued)

dc Applications

Battery Feed

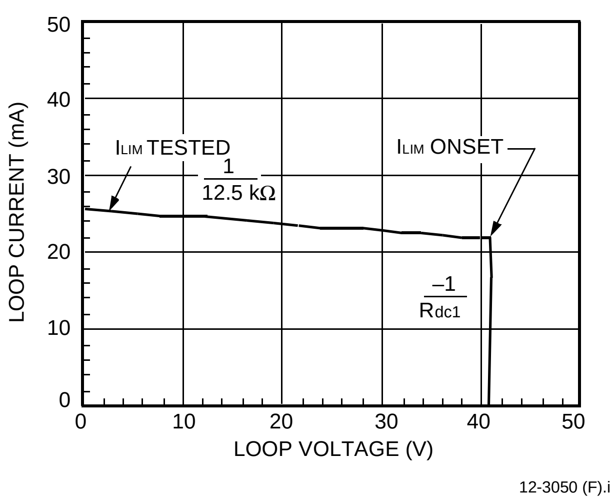
The dc feed characteristic can be described by:

$$V_{T/R} = \frac{(|V_{BAT}| - V_{OH}) \times R_L}{R_L + 2R_P + R_{dc}}$$

$$I_L = \frac{|V_{BAT}| - V_{OH}}{R_L + 2R_P + R_{dc}}$$

where:
I_L = dc loop current.
$V_{T/R}$ = dc loop voltage.
$|V_{BAT}|$ = battery voltage magnitude.
V_{OH} = overhead voltage. This is the difference between the battery voltage and the open loop tip/ring voltage.
R_L = loop resistance, not including protection resistors.
R_P = protection resistor value.
R_{dc} = SLIC internal dc feed resistance.

The design begins by drawing the desired dc template. An example is shown in Figure 13.



Notes:
V_{BAT} = –48 V.
I_{LIM} = 22 mA.
R_{dc1} = 115 Ω.

Figure 13. Loop Current vs. Loop Voltage

Starting from the on-hook condition and going through to a short circuit, the curve passes through the following two regions:

Region 1: On-hook and low-loop currents. The slope corresponds to the dc resistance of the SLIC, R_{dc1} (70 Ω typical). The open circuit voltage is the battery voltage minus the overhead voltage of the device, V_{OH} (6.5 V typical). These values are suitable for most applications but can be adjusted if needed.

Region 2: Current limit. The dc current is limited to a starting value determined by external resistor R_{PROG}, an internal current source, and the gain from tip/ring to pin DCOUT.

Current Limit

With the B0/B1 logic inputs set to 11 (low current limit), current limit with a 100 Ω load is given by the following equation:

$0.637\ R_{PROG}$ (kΩ) + 2 mA= I_{LIM} x (mA)

The relationship between low current limit (B0 = 1, B1 = 1) and high current limit (B0 = 1, B1 = 0) is

$$\frac{I_{LIMIT}(Low)}{I_{LIMIT}(High)} = 0.7$$

Overhead Voltage

In order to drive an on-hook ac signal, the SLIC must set up the tip and ring voltage to a value less than the battery voltage. The amount that the open loop voltage is decreased relative to the battery is referred to as the overhead voltage, expressed as the following equation:

$$V_{OH} = |V_{BAT}| - (V_{PT} - V_{PR})$$

Without this buffer voltage, amplifier saturation will occur and the signal will be clipped. The L9218 is automatically set at the factory to allow undistorted on-hook transmission of a 3.14 dBm signal into a 900 Ω loop impedance.

Applications (continued)

dc Applications (continued)

Loop Range

The equation below can be rearranged to provide the loop range for a required loop current:

$$R_L = \frac{|V_{BAT}| - V_{OH}}{I_L} - 2R_P - R_{DC}$$

Off-Hook Detection

The loop closure comparator has built-in longitudinal rejection, eliminating the need for an external 60 Hz filter. The loop closure detection threshold is set by resistor R_{LCTH}. The supervision output bit NSTAT is high in an on-hook condition. The off-hook comparator goes low during an off-hook condition:

I_{TR} (mA) = 0.4167 R_{LCTH} (kΩ) – 1.9 mA ACTIVE off-hook to on-hook

I_{TR} (mA) = 0.4167 R_{LCTH} (kΩ) + 2.7 mA SCAN on-hook to off-hook

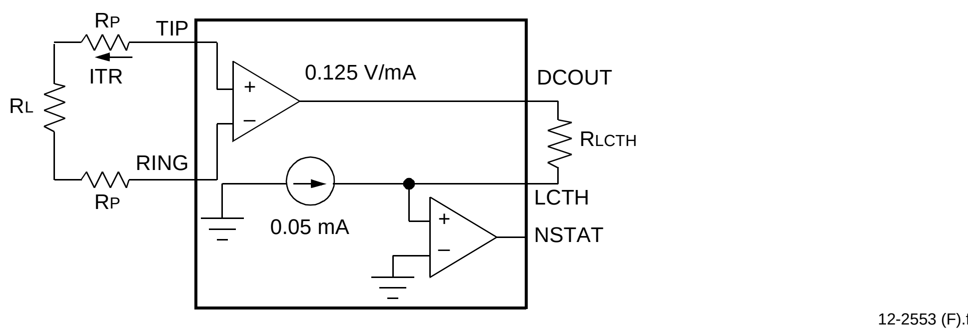


Figure 14. Off-Hook Detection Circuit

Applications (continued)

dc Applications (continued)

Ring Trip Detection

The ring trip circuit is a comparator that has a special input section optimized for this application. The equivalent circuit is shown in Figure 15, along with its use in an application using unbalanced, battery-backed ringing.

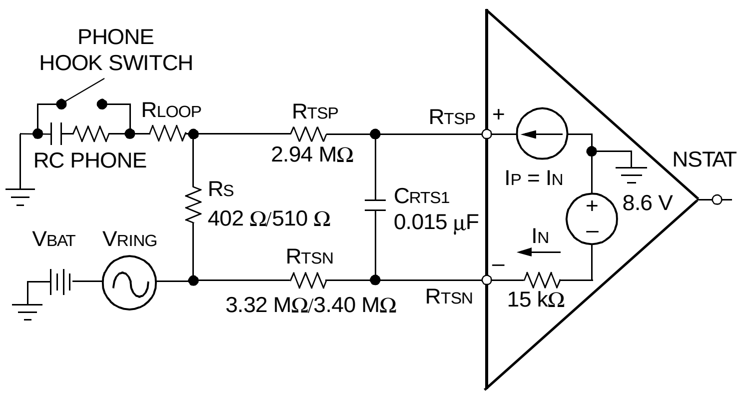


Figure 15. Ring Trip Equivalent Circuit and Equivalent Application

Ring trip detection threshold is given by the following equation:

$$I_{TH}\,(\text{mA}) = \frac{[RTSN(M\Omega) + 0.015 - RTSP(M\Omega)] \times [|V_{BAT}| - 8.6] \times 1000}{[RTSN(M\Omega) + 0.015] \times R_S}$$

Longitudinal Balance

The SLIC is graded to certain longitudinal balance specifications. The numbers are guaranteed by testing (Figure 5 and Figure 8). However, for specific applications, the longitudinal balance may also be determined by termination impedance, protection resistance, and especially by the mismatch between protection resistors at tip and ring. This can be illustrated by the following equation:

$$LB = 20 \times \log \frac{(368 + RP) \times (368 + ZT - RP)}{368 \times (2 \times [ZT - 2 \times RP] \times \Delta + \varepsilon)}$$

where:

LB: longitudinal balance.
RP: protection resistor value in Ω.
ZT: magnitude of the termination impedance in Ω.
ε: protection resistor mismatch in Ω.
Δ: SLIC internal tip/ring sensing mismatch.

The Δ can be calculated using the above equation with these exceptions: ε = 0, ZT = 600 Ω, RP = 100 Ω, and the longitudinal balance specification on a specific code.

Now with Δ available, the equation will predict the actual longitudinal balance for RP, ZT, and ε.

Be aware that ZT may vary with frequency for complex impedance applications.

Applications (continued)

ac Design

Codec Types

At this point in the design, the codec needs to be selected. The interface network between the SLIC and codec can then be designed. There are four key ac design parameters. Termination impedance is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. Transmit gain is measured from the 2-wire port to the PCM highway, while receive gain is done from the PCM highway to the transmit port. Finally, the hybrid balance network cancels the unwanted amount of the receive signal that appears at the transmit port.

Below is a brief codec feature summary.

First-Generation Codecs. These perform the basic filtering, A/D (transmit), D/A (receive), and µ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, 5 V only or ±5 V operation, and µ-law/A-law selectability. These are available in single and quad designs. This type of codec requires continuous time analog filtering via external resistor/capacitor networks to set the ac design parameters. An example of this type of codec is the Agere T7504 quad 5 V only codec.

This type of codec tends to be the most economical in terms of piece part price, but tends to require more external components than a third-generation codec. Furthermore, ac parameters are fixed by the external R/C network, so software control of ac parameters is difficult.

Third-Generation Codecs. This class of devices includes all ac parameters set digitally under microprocessor control. Depending on the device, it may or may not have data control latches. Additional functionality sometimes offered includes tone plant generation and reception, TTX generation, test algorithms, and echo cancellation. Again, this type of codec may be 5 V only or ±5 V operation, single quad or 16-channel, and µ-law/A-law or 16-bit linear coding selectable. Examples of this type of codec are the Agere T8535/6 (5 V only, quad, standard features), T8533/4 (5 V only, quad with echo-cancellation), and the T8531/36 (5 V only 16-channel with self-test).

ac Interface Network

The ac interface network between the L9218 and the codec will vary depending on the codec selected. With a first-generation codec, the interface between the L9218 and codec actually sets the ac parameters. With a third-generation codec, all ac parameters are set digitally, internal to the codec; thus, the interface between the L9218 and this type of codec is designed to avoid overload at the codec input in the transmit direction, and to optimize signal-to-noise ratio (S/N) in the receive direction.

Receive Interface

Because the design requirements are very different with a first- or third-generation codec, the L9218 is offered with two different receive gains. Each receive gain was chosen to optimize, in terms of external components required, the ac interface between the L9218 and the codec.

With a first-generation codec, the termination impedance is set by providing gain shaping through a feedback network from the SLIC VITR output to the SLIC RCVN/RCVP inputs. The L9218 provides a transconductance from T/R to VITR in the transmit direction and a single-ended to differential gain in the receive direction from either RCVN or RCVP to T/R. Assuming a short from VITR to RCVN or RCVP, the maximum impedance that is seen looking into the SLIC is the product of the SLIC transconductance times the SLIC receive gain, plus the protection resistors. The various specified termination impedance can range over the voice band as low as 300 Ω up to over 1000 Ω. Thus, if the SLIC gains are too low, it will be impossible to synthesize the higher termination impedances. Furthermore, the termination that is achieved will be far less than what is calculated by assuming a short for SLIC output to SLIC input. In the receive direction, in order to control echo, the gain is typically a loss, which requires a loss network at the SLIC RCVN/RCVP inputs, which will reduce the amount of gain that is available for termination impedance. For this reason, a high-gain SLIC is required with a first-generation codec.

Applications (continued)

ac Design (continued)

Receive Interface (continued)

With a third-generation codec, the line card designer has different concerns. To design the ac interface, the designer must first decide upon all termination impedance, hybrid balances, and transmission-level points (TLP) requirements that the line card must meet. In the transmit direction, the only concern is that the SLIC does not provide a signal that is too hot and overloads the codec input. Thus, for the highest TLP that is being designed to, given the SLIC gain, the designer, as a function of voice band frequency, must ensure that the codec is not overloaded. With a given TLP and a given SLIC gain (if the signal will cause a codec overload), the designer must insert some sort of loss, typically a resistor divider, between the SLIC output and codec input.

In the receive direction, the issue is to optimize S/N. Again, the designer must consider all the considered TLPs. The idea is, for all desired TLPs, to run the codec at or as close as possible to its maximum output signal, to optimize the S/N. Remember noise floor is constant, so the hotter the signal from the codec, the better the S/N. The problem is, if the codec is feeding a high-gain SLIC, either an external resistor divider is needed to knock the gain down to meet the TLP requirements, or the codec is not operating near maximum signal levels, thus compromising the S/N.

It appears the solution is to have a SLIC with a low gain, especially in the receive direction. This will allow the codec to operate near its maximum output signal (to optimize S/N), without an external resistor divider (to minimize cost).

Note also that some third-generation codecs require the designer to provide an inherent resistive termination via external networks. The codec will then provide gain shaping, as a function of frequency to meet the return loss requirements. Further stability issues may add external components or excessive ground plane requirements to the design.

To meet the unique requirements of both types of codecs, the L9218 offers two receive gain choices. These receive gains are mask-programmable at the factory and are offered as two different code variations. For interface with a first-generation codec, the L9218A is offered with a receive gain of 7.86. For interface with a third-generation codec, the L9218G is offered with a receive gain of 2. In either case, the transconductance in the transmit direction, or the transmit gain is 403 Ω.

Example 1: Real Termination (First-Generation Codec)

ac equivalent circuits for real termination using a T7504 codec is shown in Figure 15.

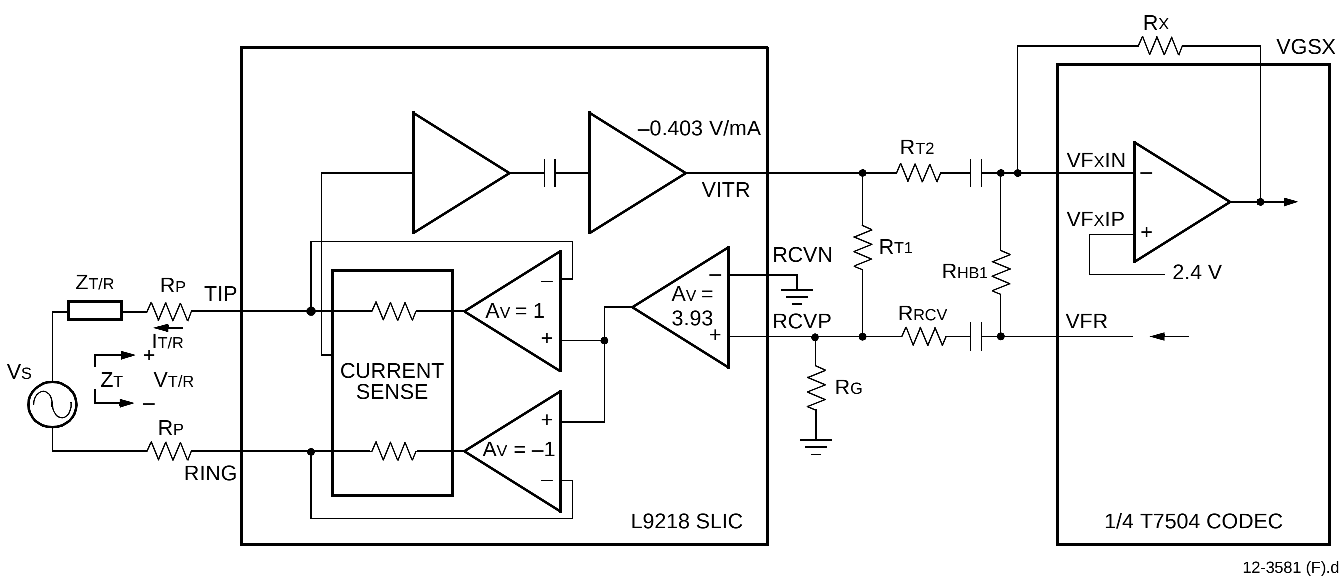


Figure 16. ac Equivalent Circuit

Applications (continued)

ac Design (continued)

Example 1: Real Termination (First-Generation Codec) (continued)

The following design equations refer to the circuit in Figure 16. Use these to synthesize real termination impedance.

Termination Impedance:

$$Z_T = \frac{V_{T/R}}{-I_{T/R}}$$

$$Z_T = 2R_P + \frac{3168}{1 + \frac{R_{T3}}{R_{GP}} + \frac{R_{T3}}{R_{RCV}}}$$

Receive Gain:

$$g_{rcv} = \frac{V_{T/R}}{V_{fr}}$$

$$g_{rcv} = \frac{7.86}{\left(1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GP}}\right)\left(1 + \frac{Z_T}{Z_{T/R}}\right)}$$

Transmit Gain:

$$g_{tx} = \frac{V_{GSX}}{V_{T/R}}$$

$$g_{tx} = \frac{R_X}{R_{T6}} \text{ x } \frac{403}{Z_T}$$

Hybrid Balance:

$$h_{bal} = 20\log\frac{V_{GSX}}{V_{T/R}}$$

To optimize the hybrid balance, the sum of the currents at the VFX input of the codec op amp should be set to 0. The following expressions assume the test network is the same as the termination impedance:

$$R_{HB} = \frac{R_X}{g_{tx} \times g_{rcv}}$$

$$h_{bal} = 20\log\left(\frac{R_X}{R_{HB}} - g_{tx} \times g_{rcv}\right)$$

Applications (continued)

ac Design (continued)

Example 2: Complex Termination (First-Generation Codec)

Below are design equations for complex termination (see Figure 17 and Figure 18).

$Z_T = R_{T1} + R_{T2} \parallel C_T$

$$R_{T1} = 2R_P + \frac{7.86}{201.2} \bullet \left(\frac{1}{1 + \frac{R_{T3}}{R_{GP}} + \frac{R_{T3}}{R_{RCV}}} - \frac{1}{1 + \frac{R_{N1}}{R_{N2}}} \right) R_{TGP} \parallel R_{TGS}$$

$$R_{T2} = \frac{7.86}{201.2} \bullet \left(\frac{R_{TGP}/R_{TGS}}{1 + \frac{R_{T3}}{R_{GP}} + \frac{R_{T3}}{R_{RCV}}} + \frac{1}{1 + \frac{R_{N1}}{R_{N2}}} \right) R_{TGP} \parallel R_{TGS}$$

$$\frac{1}{C_T} = \frac{7.86}{201.2}\left(\frac{1}{C_{N1}} \frac{R_{N2}}{(R_{N1} + R_{N2})^2} R_{TGP} \parallel R_{TGS} + \frac{1}{C_{TG}} \bullet \left(\frac{R_{TGP}}{R_{TGP} + R_{TGS}} \right)^2 \bullet \left(\frac{1}{1 + \frac{R_{T3}}{R_{GP}} + \frac{R_{T3}}{R_{RCV}}} - \frac{1}{1 + \frac{R_{N1}}{R_{N2}}} \right) \right)$$

$$g_{tx} = \frac{R_X}{R_{T6}} \frac{1}{201.2} \frac{Z_{TG}}{Z_T}$$

$$g_{rcv} = \frac{7.86}{1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GP}}} \times \frac{1}{1 + \frac{Z_T}{Z_{T/R}}}$$

$$h_{bal} = 20\log \left(\frac{R_X}{R_{HB}} - g_{tx} \times g_{rcv} \right)$$

where:

$Z_{T/R} = R_1 + R_2 \parallel C$

$Z_{TG} = R_{TGP} \parallel (R_{TGS} + C_G)$

$R_{TGP} = 8.06\ k\Omega$

$$R_{TGS} = \frac{R_1}{R_2} R_{TGP}$$

$$C_G = \frac{R_2^2}{R_{TGP}(R_1 + R_2)} \times C$$

and

$$C_N R_{N2} = \frac{2R_P}{3168} C_G R_{TGP}$$

$$R_{N1} = R_{N2} \frac{(3168)}{2R_P}\left(\frac{R_{TGS}}{R_{TGP}} \right) - 1$$

The equations above do not include the blocking capacitors.

Applications (continued)

ac Design (continued)

Example 2: Complex Termination (First-Generation Codec) (continued)

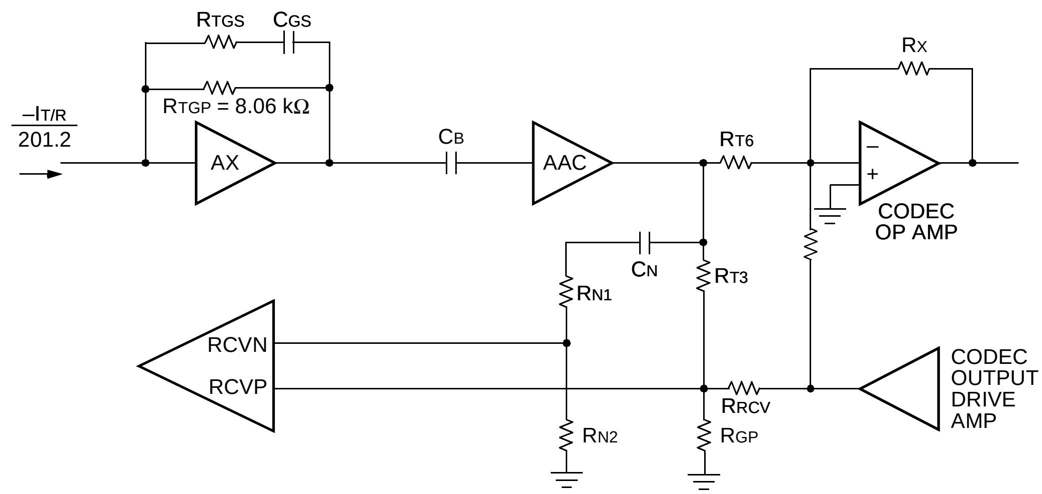


Figure 17. Interface Circuit Using First-Generation Codec (±5 V Battery)

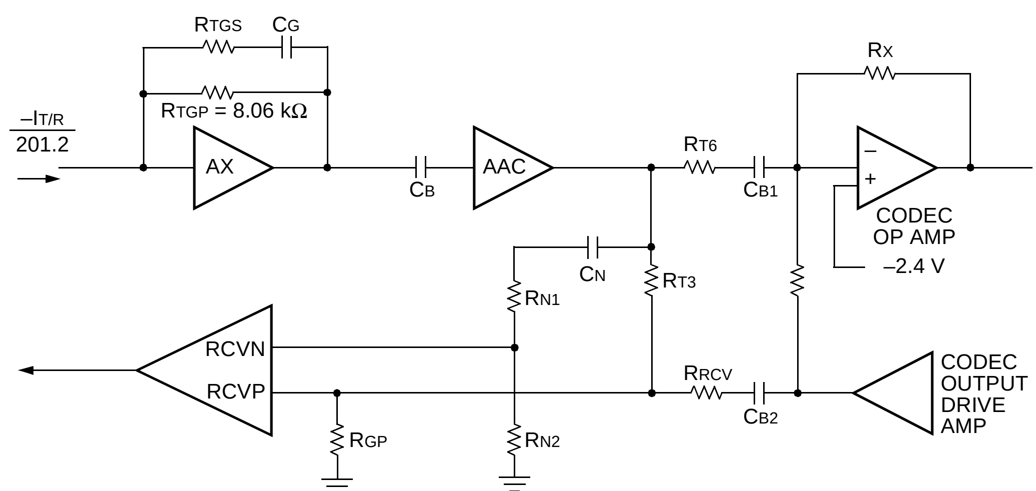


Figure 18. Interface Circuit Using First-Generation Codec (5 V Only Codec)

Applications (continued)

Power Derating

Operating temperature range, maximum current limit, maximum battery voltage, minimum dc loop, and protection resistor values will influence the overall thermal performance. This section shows the relevant design equations and considerations in evaluating the SLIC thermal performance.

Consider the L9218 SLIC in a 28-pin PLCC package. The still-air thermal resistance on a 2-layer board is typically 43 °C/W.

The SLIC will enter the thermal shutdown state at a minimum of 150 °C. The thermal shutdown design should ensure that the SLIC temperature does not reach 150 °C under normal operating conditions.

Assume a maximum ambient operating temperature of 85 °C, a maximum current limit of 25 mA (including tolerance), and a maximum battery of –52 V. Furthermore, assume a (worst-case) minimum dc loop of 200 Ω, and that 50 Ω protection resistors are used at both tip and ring.

1. $T_{TSD} - T_{AMBIENT(max)}$ = allowed thermal rise.

   150 °C – 85 °C = 65 °C

2. Allowed thermal rise = package thermal impedance • SLIC power dissipation.

   65 °C = 43 °C/W • SLIC power dissipation

   SLIC power dissipation (P_{DISS}) = 1.51 W

Thus, if the total power dissipated in the SLIC is less than 1.51 W, it will not enter the thermal shutdown state. Total SLIC power is calculated as:

Total P_{DISS} = maximum battery • maximum current limit (including effects of accuracy) + SLIC quiescent power

For the L9218, SLIC quiescent power (P_Q) is maximum at 0.158 W. Thus,

Total P_{DISS} = (–52 V • [25 mA • 1.05]) + 0.158 W

Total P_{DISS} = 1.365 W + 0.158 W

Total P_{DISS} = 1.523 W

The power dissipated in the SLIC is the total power dissipation minus the power that is dissipated in the loop.

SLIC P_{DISS} = total power – loop power

Loop power = $(I_{LIM})^2$ • (R_{dcLOOP} min + $2R_P$)

Loop power = $(25\text{ mA} \bullet 1.05)^2$ • (200 Ω + 100 Ω)

Loop power = 0.207 W

SLIC power = 1.523 W – 0.207 W = 1.28

SLIC power = 1.28 W < 1.51 W

Thus, in this example, the thermal design ensures that the SLIC will not enter the thermal shutdown state.

Pin-for-Pin Compatibility with L9217/L9219

The L9218 is an exact pin-for-pin replacement for the L9217/19. The one minor exception is L9217/19 has three logic control inputs: B0, B1, and B2. The L9218 has only two logic control inputs, B0 and B1. B2 in the L9217/19 is pin 13. Pin 13 in L9218 is NC, so a connection between the controller and pin 13 will not affect L9218 operation. This allows an exact footprint match with L9217/19.

PCB Layout Information

Make the leads to BGND and V_{BAT} as wide as possible for thermal and electrical reasons. Also, maximize the amount of PCB copper in the area of (and specifically on) the leads connected to this device for the lowest operating temperature.

When powering the device, make certain that no external potential creates a voltage on any pin of the device that exceeds the device ratings. In this application, some of the conditions that cause such potentials during powerup are the following:

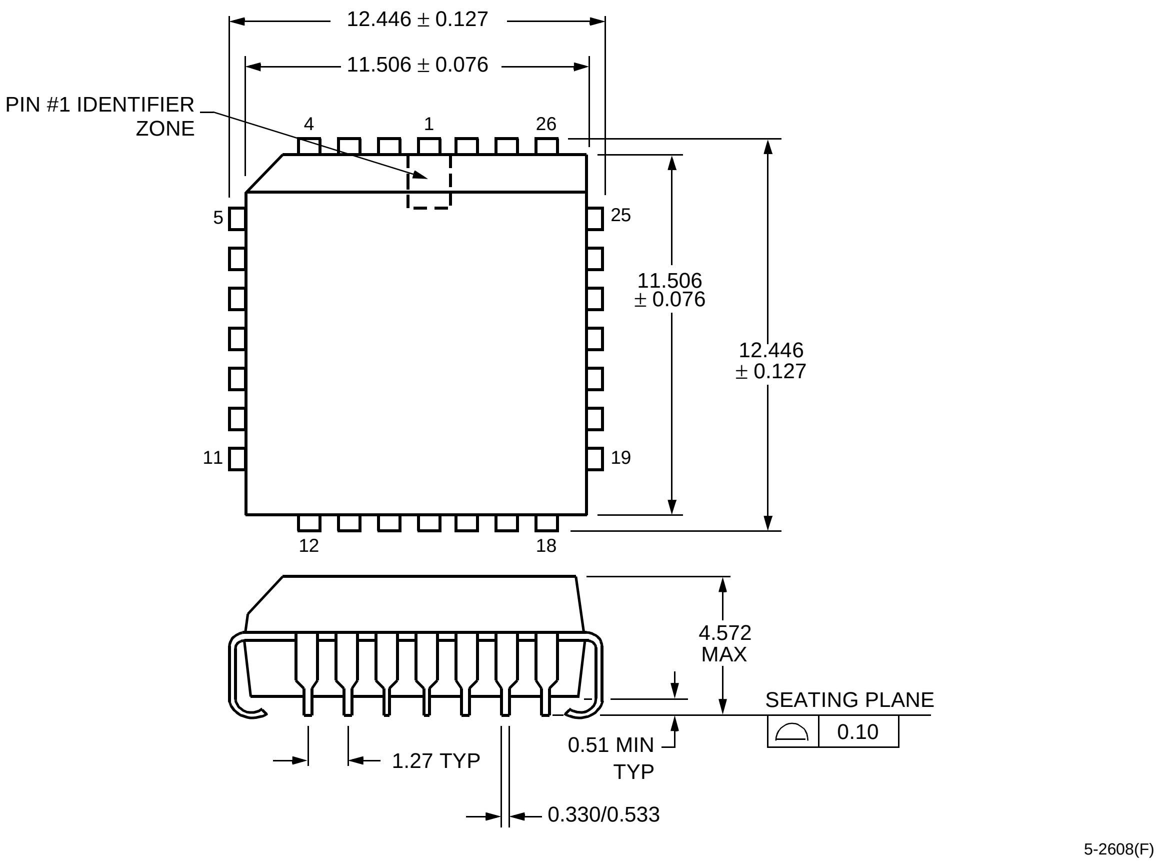
1. An inductor connected to PT and PR (this can force an overvoltage on V_{BAT} through the protection devices if the V_{BAT} connection chatters).
2. Inductance in the V_{BAT} lead (this could resonate with the V_{BAT} filter capacitor to cause a destructive overvoltage).

This device is normally used on a circuit card that is subjected to hot plug-in, meaning the card is plugged into a biased backplane connector. In order to prevent damage to the IC, all ground connections must be applied before, and removed after, all other connections.

Outline Diagram

28-Pin PLCC

Dimensions are in millimeters.



Ordering Information

Device	Package	Comcode
LUCL9218AAR-D	28-Pin PLCC (Dry Bag) Gain of 12	108558271
LUCL9218AAR-DT	28-Pin PLCC (Tape and Reel, Dry Bag) Gain of 12	108558289
LUCL9218GAR-D	28-Pin PLCC (Dry Bag) Gain of 2	108558156
LUCL9218GAR-DT	28-Pin PLCC (Tape and Reel, Dry Bag) Gain of 2	108558164

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