

### Description

The NEC μPD4265 is a 65,536-word by 1-bit dynamic CMOS Random Access Memory (RAM) designed to operate from a single +5 V power supply. The negative voltage substrate bias is generated internally providing automatic and transparent operation. The unique construction of the μPD4265 allows for an extremely low standby power device that incorporates three user-selected, self-refresh standby modes. The device can accomplish RAS-only refresh. Also, by utilizing the pin 1 refresh function, it can perform automatic pulsed refresh or hidden auto pulsed refresh which makes use of the internal refresh address generator.

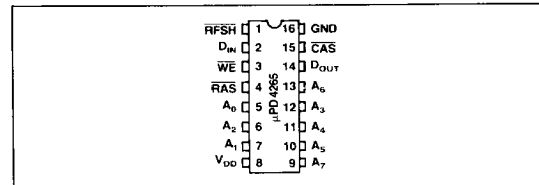
### Features

- 65,536-word x 1-bit organization
- High memory density: 16-pin plastic DIP
- Single +5V ± 10% power supply
- Control on pin 1 for automatic and self refresh
- Multiplexed address inputs
- Fully TTL-compatible including clocks
- Three-state output
- Read, write, RMW, RAS-only refresh, page mode, latched pulse, pulse and self-refresh capabilities
- CAS-controlled output allows hidden refresh
- 2 performance ranges:

Device	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	Power
μPD4265C-20	200ns	100ns	335ns	193mW
μPD4265C-25	250ns	125ns	410ns	165mW

- Cycle time: R/W, 335ns min
- Low power dissipation
  - 35mA max (operating)
  - 1.0mA max (standby,  $\overline{RAS} = \overline{CAS} = V_{IH}$ )
  - 0.5mA max (standby,  $\overline{RAS} = \overline{CAS} = V_{DD}$ )
  - 200μA max (self-refresh 1, T<sub>A</sub> = 0°C to +70°C)
  - 100μA max (self-refresh 2, T<sub>A</sub> = 0°C to +45°C)
  - 50μA max (self-refresh 3, T<sub>A</sub> = 0°C to +25°C)  
(According to Figure 1.)
- 128 refresh cycles

### Pin Configuration



### Pin Identification

No.	Pin Symbol	Function
1	RFSH	Refresh
2	D <sub>IN</sub>	Data-in
3	WE	Write Enable
4	RAS	Row Address Strobe
5-7, 9-13	A <sub>0</sub> - A <sub>7</sub>	Address Inputs
5-7, 10-13	A <sub>0</sub> - A <sub>8</sub>	Refresh Addresses
8	V <sub>DD</sub>	+5V Power Supply
14	D <sub>OUT</sub>	Data-out
15	CAS	Column Address Strobe
16	GND	Ground

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### Absolute Maximum Ratings\*

Voltage on any Pin Relative to Ground, V <sub>IO</sub>	-1.0V to +7.0V
Operating Temperature, T <sub>OPT</sub> (Ambient)	0°C to +70°C
Storage Temperature, T <sub>STG</sub> (Ambient)	-55°C to +125°C
Short-circuit Output Current, I <sub>OS</sub>	50mA
Power Dissipation, P <sub>D</sub>	1W

\*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Capacitance

T<sub>A</sub> = 25°C; f = 1MHz

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Address, Data-in	C <sub>11</sub>			5	pF	
RAS, CAS, WE, RFSH	C <sub>12</sub>			8	pF	
Output	C <sub>0</sub>			7	pF	

**DC Characteristics**

T<sub>A</sub> = 0°C to +70°C; V<sub>DD</sub> = 5V ± 10%

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Supply Voltage	V <sub>DD</sub>	4.5	5.0	5.5	V	All Voltages Referenced to Ground
High-level Input Voltage	V <sub>IH</sub>	2.4		5.5	V	
Low-level Input Voltage	V <sub>IL</sub>	-1.0		0.8	V	
V <sub>DD</sub> Supply Current Standby	I <sub>DD2</sub>			1.0	mA	RAS = CAS = V <sub>IH</sub>
Standby (Output-enable)	I <sub>DD5</sub>			1.0	mA	RAS = V <sub>IH</sub>
Standby	I <sub>DD6</sub>			0.5	mA	RAS = CAS = V <sub>DD</sub>
Self-refresh 1 (T <sub>A</sub> = 0°C to +70°C)	I <sub>DD8</sub>			200	μA	RAS = CAS = V <sub>IH</sub> ; WE = V <sub>IH</sub>
Self-refresh 2 (T <sub>A</sub> = 0°C to +45°C)	I <sub>DD9</sub>			100	μA	RAS = CAS = V <sub>IH</sub> ; WE = V <sub>IL</sub>
Self-refresh 3	I <sub>DD10</sub>			①		CAS = GND; RAS = V <sub>IH</sub> ; WE = V <sub>DD</sub> /GND
Input Leakage Current	I <sub>IL</sub>	-10		10	μA	
Output Leakage Current	I <sub>OL</sub>	-10		10	μA	
Output Low Voltage	V <sub>OL</sub>	0		0.4	V	I <sub>OL</sub> = 4.2mA
Output High Voltage	V <sub>OH</sub>	2.4		V <sub>DD</sub>	V	I <sub>OH</sub> = -5mA

Note: ① According to Figure 1.

**AC Characteristics**

T<sub>A</sub> = 0°C to +70°C; V<sub>DD</sub> = 5V ± 10%

Read, Write, RMW, RAS-only Refresh Cycles

Parameter	Symbol	Limits		Unit	Test Conditions	
		4265-20	4265-25			
V <sub>DD</sub> Operating Current	I <sub>DD1</sub>		35	30	mA	
V <sub>DD</sub> RAS-only Refresh Current	I <sub>DD3</sub>		30	25	mA	
V <sub>DD</sub> Page Current	I <sub>DD4</sub>		20	17	mA	
Random Read or Write Cycle Time	t <sub>RC</sub>	335	410		ns	
Read, Write Cycle Time	t <sub>RWC</sub>	370	465		ns	
Access Time from RAS	t <sub>RAC</sub>	200	250		ns	
Access Time from CAS	t <sub>CAC</sub>	100	125		ns	
Output Buffer Turn-off Delay	t <sub>OFF</sub>	0	50	0	60	ns
Transition Time (Rise and Fall)	t <sub>T</sub>	3	50	3	60	ns
RAS Precharge Time	t <sub>RP</sub>	120	150		ns	
RAS Pulse Width	t <sub>RAS</sub>	200	10000	250	10000	ns
RAS Hold Time	t <sub>RSH</sub>	100	125		ns	
CAS Pulse Width	t <sub>CAS</sub>	100	10000	125	10000	ns
CAS Hold Time	t <sub>CSH</sub>	200	250		ns	
RAS to CAS Delay Time	t <sub>RCD</sub>	30	100	35	125	ns
CAS to RAS Precharge Time	t <sub>CRP</sub>	0	0	0	ns	
CAS Precharge Time, (Nonpage Cycles)	t <sub>CPN</sub>	30	35		ns	
RAS Precharge CAS Hold Time	t <sub>RPC</sub>	0	0		ns	
Row Address Set-up Time	t <sub>ASR</sub>	0	0		ns	
Row Address Hold Time	t <sub>RAH</sub>	20	25		ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	0		ns	
Column Address Hold Time	t <sub>CAH</sub>	55	65		ns	
Column Address Hold Time Referenced to RAS	t <sub>AR</sub>	155	190		ns	
Read Command Set-up Time	t <sub>RCS</sub>	0	0		ns	
Read Command Hold Time Referenced to RAS	t <sub>RRH</sub>	25	30		ns	
Read Command Hold Time Referenced to CAS	t <sub>RCH</sub>	0	0		ns	
Write Command Hold Time	t <sub>WCH</sub>	55	65		ns	

**AC Characteristics (Cont.)**

T<sub>A</sub> = 0°C to +70°C; V<sub>DD</sub> = 5V ± 10%

Read, Write, RMW, RAS-only Refresh Cycles

Parameter	Symbol	Limits				Unit	Test Conditions
		4265-20		4265-25			
Write Command Hold Time Referenced to RAS	t <sub>WCR</sub>	155		190		ns	
Write Command Pulse Width	t <sub>WP</sub>	55		65		ns	
Write Command to RAS Lead Time	t <sub>RWL</sub>	55		65		ns	
Write Command to CAS Lead Time	t <sub>CWL</sub>	55		65		ns	
Data-in Set-up Time	t <sub>DS</sub>	0		0		ns	
Data-in Hold Time	t <sub>DH</sub>	55		65		ns	
Data-in Hold Time Referenced to RAS	t <sub>DHR</sub>	155		190		ns	
Refresh Period	t <sub>REF</sub>		2		2	ns	
WE Command Set-up Time	t <sub>WCS</sub>	-10		-10		ns	
CAS to WE Delay	t <sub>CWD</sub>	80		100		ns	
RAS to WE Delay	t <sub>RWD</sub>	180		235		ns	

**Page Mode Cycle**

Parameter	Symbol	Limits				Unit	Test Conditions
		4265-20		4265-25			
Read or Write Cycle Time	t <sub>PC</sub>	190		260		ns	
Read Modify Write Cycle Time	t <sub>CPM</sub>	230		280		ns	
CAS Precharge Time	t <sub>CP</sub>	80		100		ns	
RAS Pulse Width	t <sub>CPM</sub>	200	10000	250	10000	ns	
CAS Pulse Width	t <sub>CAS</sub>	100	10000	125	10000	ns	

**Pulse Refresh Cycle (Latched Pulse Refresh)**

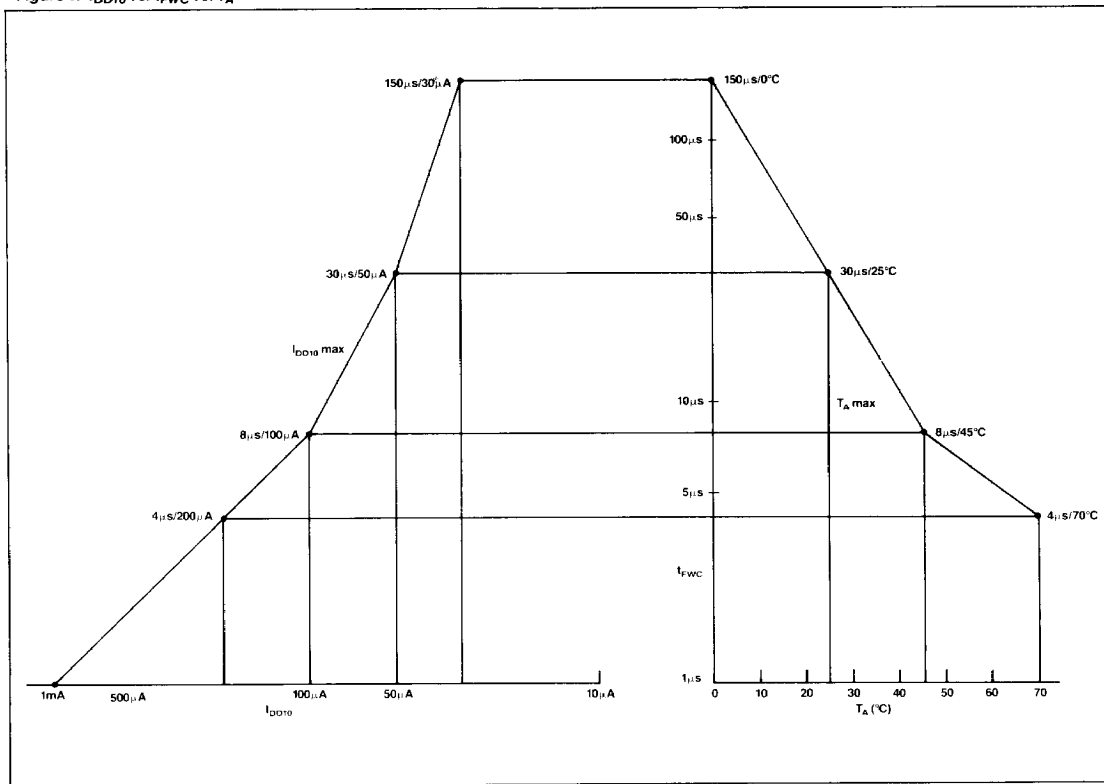
Parameter	Symbol	Limits				Unit	Test Conditions
		4265-20		4265-25			
V <sub>DD</sub> Pulse Refresh Current	I <sub>DD7</sub>		25		20	mA	
Pulse Refresh Cycle Time	t <sub>RC</sub>	335		410		ns	
RAS to RFSH Delay	t <sub>RFD</sub>	120		150		ns	
RFSH Pulse Width	t <sub>RFS</sub>	80	1000	80	1000	ns	
RFSH Precharge Time	t <sub>RFP</sub>	120		120		ns	
RFSH to RAS Delay	t <sub>RSR</sub>	30		30		ns	
RFSH before RAS Set-up Time	t <sub>RBR</sub>	365		445		ns	
RAS to RFSH Delay (Latched Pulse)	t <sub>RFD</sub>	80		80		ns	
RAS to RFSH Set-up (Latched Pulse)	t <sub>RFS</sub>	455		560		ns	

**Self-refresh Cycle**

Parameter	Symbol	Limits				Unit	Test Conditions
		4265-20		4265-25			
RAS to RFSH Delay	t <sub>RFD</sub>	120		150		ns	
RFSH Pulse Width	t <sub>RFS</sub>	8000		8000		ns	
RFSH to RAS Delay	t <sub>RSR</sub>	365		445		ns	
RAS Hold Time	t <sub>RH</sub>	8000		8000		ns	
RAS to RFSH Set-up Time	t <sub>RFS</sub>	0		0		ns	
RFSH to CAS Delay	t <sub>FCD</sub>	0	1000	0	1000	ns	
RFSH to WE Delay	t <sub>FWD</sub>	0	1000	0	1000	ns	
RFSH to CAS Set-up Time	t <sub>FCS</sub>	0		0		ns	
RFSH to WE Set-up Time	t <sub>FWS</sub>	0		0		ns	
CAS to WE Set-up Time	t <sub>FWCS</sub>	0		0		ns	
WE Pulse Width	t <sub>FWP</sub>	1		1		μs	
WE Pulse Cycle Time	t <sub>FWC</sub>		①		①	μs	

Note: ① According to Figure 1.

Figure 1.  $I_{DDIO}$  vs.  $t_{FWC}$  vs.  $T_A$

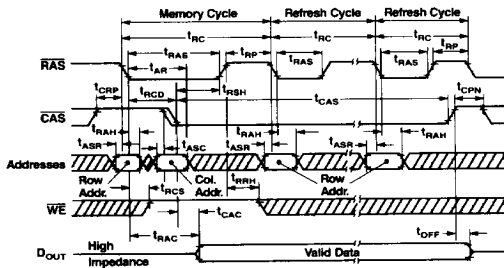


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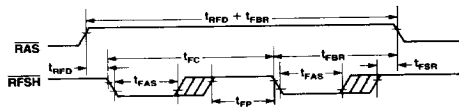


## Timing Waveforms (Cont.)

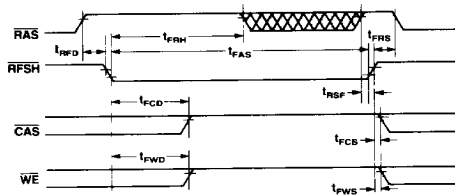
**Hidden Refresh Cycle**



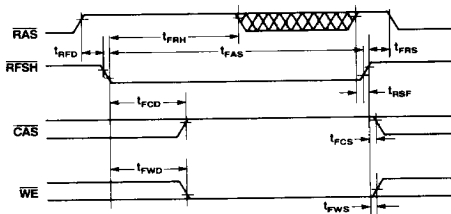
**Pulse Refresh Cycle**



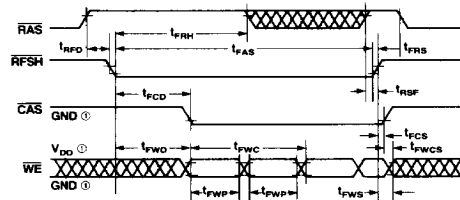
**Self-refresh Cycle 1**



**Self-refresh Cycle 2**

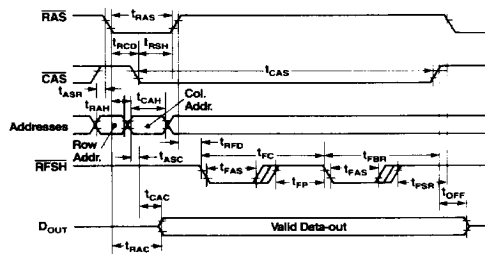


**Self-refresh Cycle 3**



Note: ① Needs CMOS level.

**Hidden Automatic Pulse Refresh Cycle**



**Latched Pulse Refresh Cycle**

