

TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 9 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2089C-35
TMM2089C-45
TMM2089C-55

PRELIMINARY

DESCRIPTION

The TMM2089C is a 73,728 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 9 bits and operates from a single 5-volt supply. The TMM2089C is features an automatic stand-by mode when deselected by $\overline{CS1}$ signal. Thus the TMM2089C

is suitable for use in cache memory and high speed storage. The TMM2089C has nine I/O terminals, therefore it is most suitable for MEMORY SYSTEM with Parity bit. The TMM2089C is offered in a 28 pin standard ceramic dual in-line package with 0.3 inch width for high density assembly.

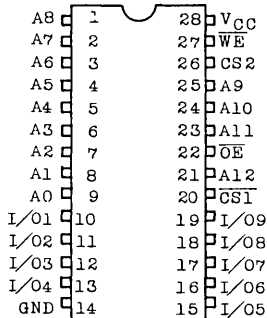
FEATURES

- Access Time and Current

Part Number	Parameter	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2089C-35		35ns	135mA	15mA
TMM2089C-45		45ns	135mA	15mA
TMM2089C-55		55ns	135mA	15mA

- Single 5V Power Supply
- Fully static Operation
- Power Down Feature : ($\overline{CS1}$)
- Output Buffer Control : (\overline{OE})
- Three State Outputs

PIN CONNECTION (TOP VIEW)

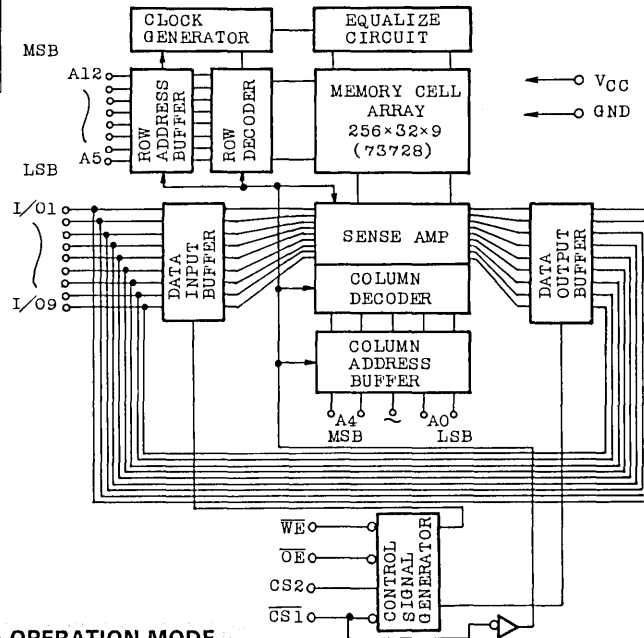


PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
$\overline{CS1}, \overline{CS2}$	Chip Select Inputs
\overline{WE}	Write Enable Input
I/O1 ~ I/O9	Data Input/Output
\overline{OE}	Output Enable Input
Vcc	Power (+5V)
GND	Ground

- All Inputs and Outputs: (Directly TTL Compatible)
- Inputs Protected: (All inputs have protection against static charge.)

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CS1}$	$\overline{CS2}$	\overline{OE}	\overline{WE}	I/O1 ~ 9	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

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MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	Power Supply Voltage	-3.5~7.0	V
V _{IN} , V _{OUT}	Input Output Voltage	-3.5~7.0	V
T _{opr.}	Operating Temperature	0~70	°C
T _{stg.}	Storage Temperature	-55~150	°C
T _{holder}	Soldering Temperature · Time	260·10	°C·sec
P _D	Power Dissipation (Ta=70°C)	1.0	W

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V _{IH}	Input High Voltage	2.0	—	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-3.0	—	0.8	V
V _{CC}	V _{CC} Power Supply Voltage	4.50	5.00	5.50	V

* Pulse width : 10ns, DC : -0.5V (Min.)

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} =0V~5.5V	-1.0	1.0	μA
I _{OH}	Output High Current	V _{OH} =2.4V	-4.0	—	mA
I _{OL}	Output Low Current	V _{OL} =0.4V	8.0	—	mA
I _{LO}	Output Leakage Current	CS1=V _{IH} or CS2=V _{IL} or WE=V _{IL} or OE=V _{IH} , V _{OUT} =0V~5.5V	-1.0	1.0	μA
I _{SBP}	Peak Power-on Current	CS1=V _{CC} , CS2=0V, I _{OUT} =0mA	—	30	mA
I _{SB}	Standby Current	CS1=V _{IH} , I _{OUT} =0mA	—	15	mA
I _{CC}	Operating Current	CS1=V _{IL} , I _{OUT} =0mA	—	135	mA

CAPACITANCE * (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} =0V	8	pF
C _{OUT}	Output Capacitance	V _{IN} =0V	10	pF

* Note : This parameter is periodically sampled and is not 100% tested.

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A. C. CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2089C-35		TMM2089C-45		TMM2089C-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t _{ACC}	Address Access Time	—	35	—	45	—	55	
t _{CO1}	$\overline{CS1}$ Access Time	—	35	—	45	—	45	
t _{CO2}	CS2 Access Time	—	25	—	25	—	30	
t _{OE}	\overline{OE} Access Time	—	20	—	20	—	25	
t _{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	
t _{CLZ}	Output Enable Time from $\overline{CS1}$ or CS2	0	—	5	—	5	—	
t _{CHZ}	Output Disable Time from $\overline{CS1}$ or CS2	—	20	—	20	—	20	
t _{OLZ}	Output Enable Time from \overline{OE}	0	—	0	—	0	—	
t _{OHZ}	Output Disable Time from \overline{OE}	—	10	—	10	—	15	
t _{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t _{PD}	Chip Deselection to Power Down Time	—	30	—	30	—	30	

WRITE CYCLE

SYMBOL	PARAMETER	TMM2089C-35		TMM2089C-45		TMM2089C-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t _{CW}	Chip Selection to End of Write	30	—	40	—	50	—	
t _{AS}	Address Set Up Time	0	—	0	—	0	—	
t _{WP}	Write Pulse Width	25	—	35	—	45	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{DS}	Data Set UP Time	15	—	20	—	20	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	
t _{WLZ}	Output Enable Time from \overline{WE}	0	—	0	—	0	—	
t _{WHZ}	Output Disable Time from \overline{WE}	—	10	—	10	—	15	

A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig. 1

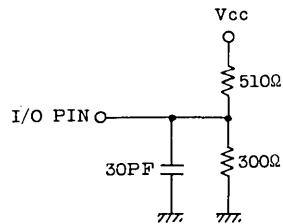
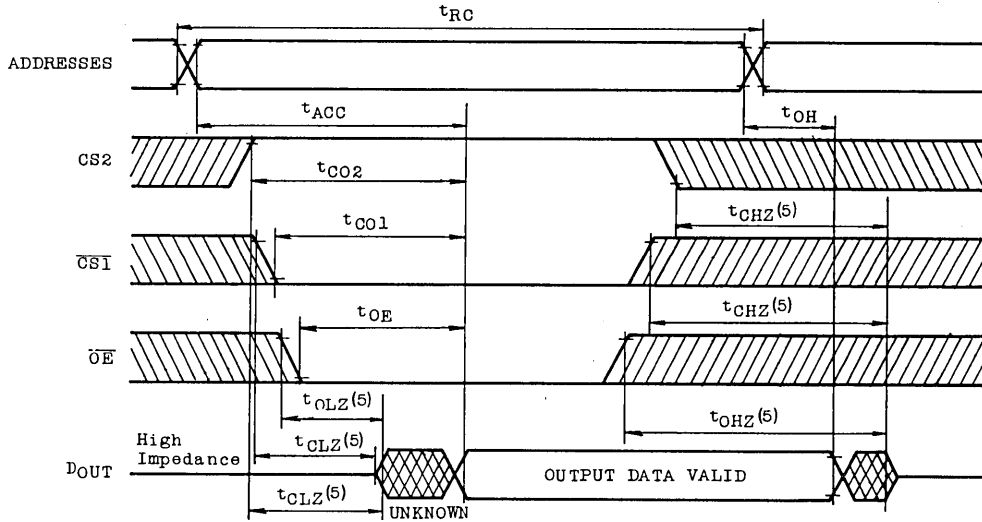


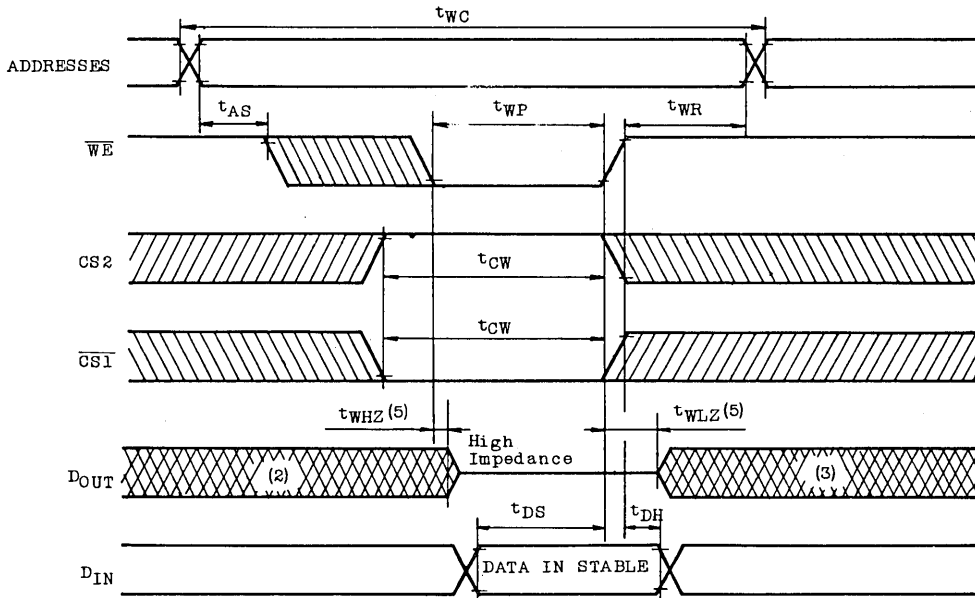
Fig.1 Output Load

TIMING WAVEFORMS

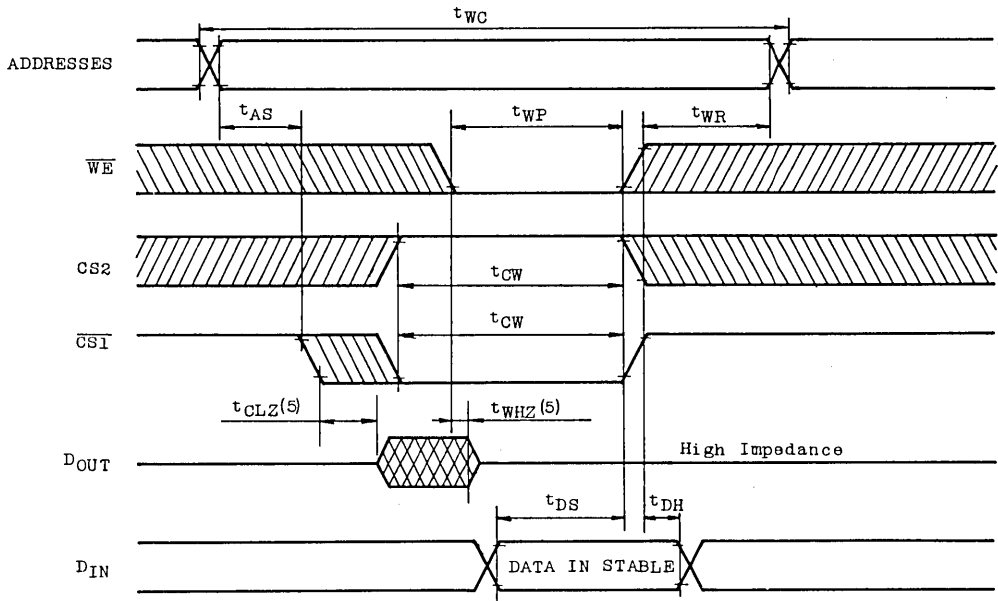
● READ CYCLE (1)



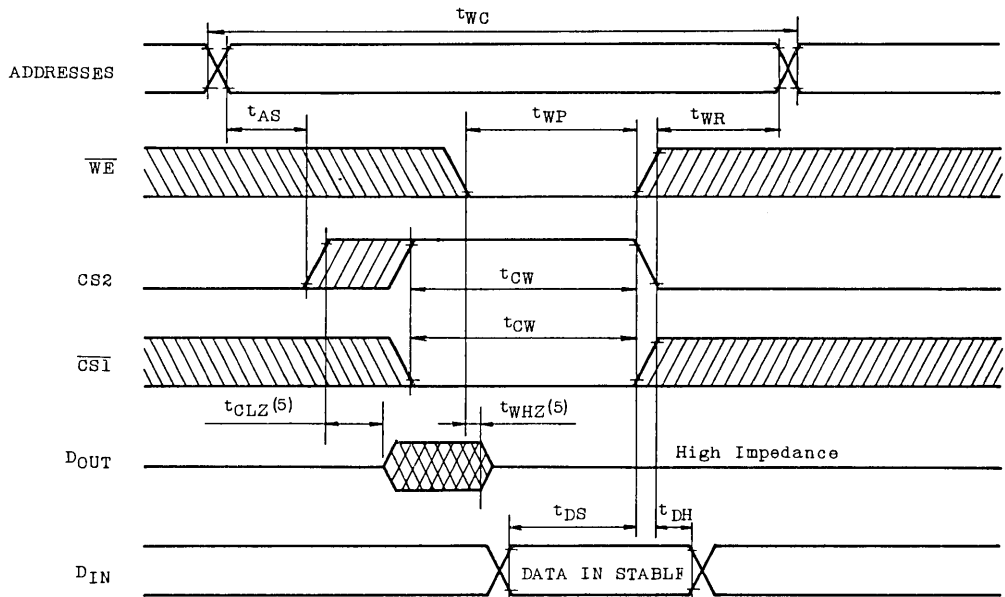
● WRITE CYCLE 1 (4) (\overline{WE} Controlled Write)



● WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



● WRITE CYCLE 3 (4) ($\overline{CS2}$ Controlled Write)

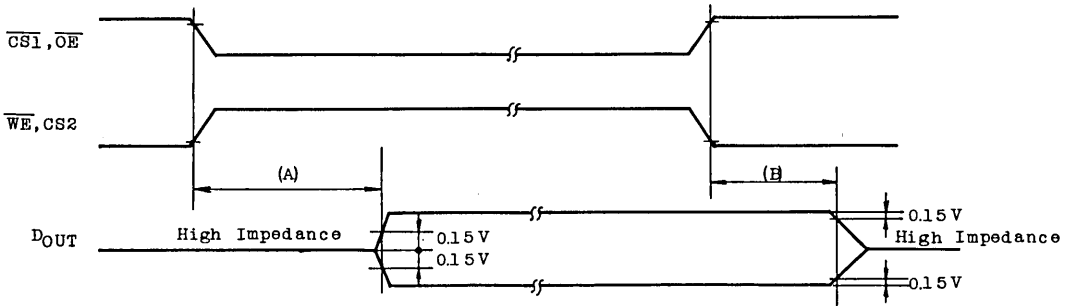


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NOTE :

1. \overline{WE} is High for Read Cycle.
2. Assuming that $\overline{CS1}$ Low transition or $\overline{CS2}$ High transition occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS1}$ High transition or $\overline{CS2}$ Low transition occurs coincident with or prior to \overline{WE} High transition, Outputs remain in a high impedance state.
4. Assuming that \overline{OE} is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load in Fig. 1.

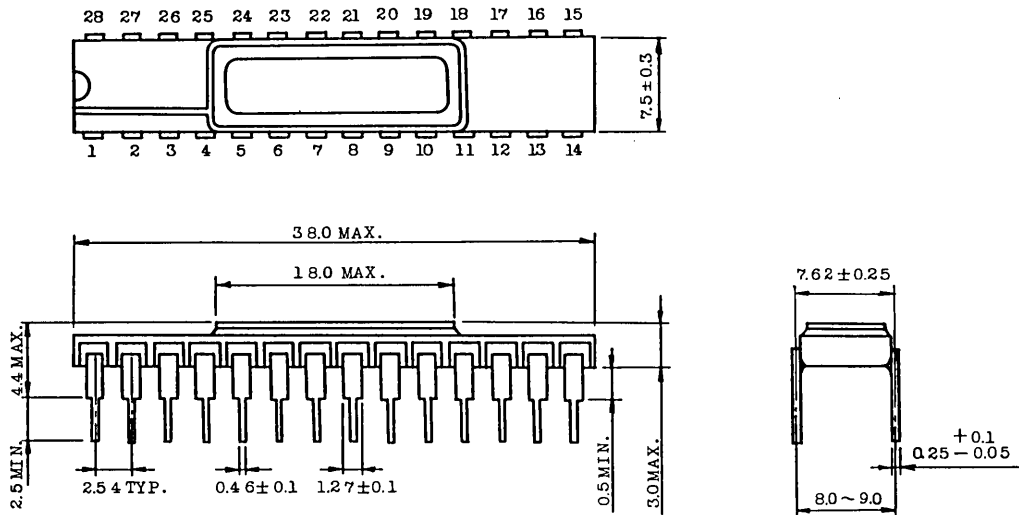
(A) $t_{CLZ}, t_{OLZ}, t_{WLZ}$Output Enable Time
 (B) $t_{CHZ}, t_{OHZ}, t_{WHZ}$Output Disable Time



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OUTLINE DRAWINGS

Unit: mm



Note : Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.28 leads.