262,144 WORD ×4 BIT DYNAMIC RAM

SILICON GATE CMOS

TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

DESCRIPTION

The TC514256P/J/Z is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514256 P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514256P/J/Z to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

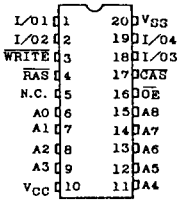
- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514256P/J/Z-85	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	30ns	35ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

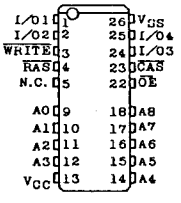
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power
  413mW MAX. Operating (TC514256P/J/Z-85)
  358mW MAX. Operating (TC514256P/J/Z-10)
  303mW MAX. Operating (TC514256P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP : TC514256P
  Plastic SOJ : TC514256J
  Plastic ZIP : TC514256Z

PIN CONNECTION (TOP VIEW)

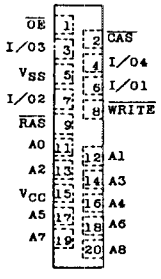
Plastic DIP



Plastic SOJ



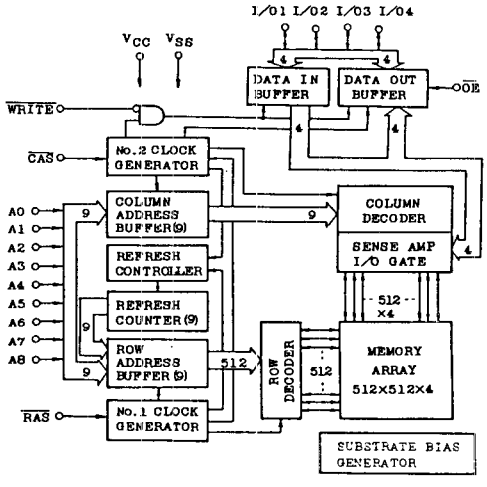
Plastic ZIP



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/01 ~ I/04	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1 ~ 7	V	1
Output Voltage	V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514256P/J/Z-85	–	75	mA	3, 4
		TC514256P/J/Z-10	–	65		
		TC514256P/J/Z-12	–	55		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN.)	TC514256P/J/Z-85	–	75	mA	3
		TC514256P/J/Z-10	–	65		
		TC514256P/J/Z-12	–	55		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL} , $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514256P/J/Z-85	–	55	mA	3, 4
		TC514256P/J/Z-10	–	45		
		TC514256P/J/Z-12	–	35		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE RAS REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before RAS Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514256P/J/Z-85	–	75	mA	3
		TC514256P/J/Z-10	–	65		
		TC514256P/J/Z-12	–	55		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ V_{CC})		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level VOLTAGE (I_{OUT} = −5mA)		2.4	–	V	
I_{OL}	OUTPUT LEVEL Output "L" Level VOLTAGE (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514256P/J/Z-85		TC514256P/J/Z-10		TC514256P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	–	190	–	220	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	225	–	255	–	295	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	55	–	70	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	110	–	115	–	140	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	85	–	100	–	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	30	–	30	–	35	ns	8, 13
t_{AA}	Access Time from Column Address	–	45	–	50	–	60	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	50	–	65	ns	8, 14
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	–	5	–	5	–	ns	5
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	–	80	–	90	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	–	30	–	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	–	100	–	120	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	30	10,000	35	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	70	25	85	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	–	15	–	20	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	15	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	20	–	25	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	50	–	60	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	20	–	20	–	25	–	ns	
t_{WCR}	Write Command Hold Time referenced to RAS	65	–	75	–	90	–	ns	
t_{WP}	Write Command Pulse Width	20	–	20	–	25	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	11
t_{DH}	Data Hold Time	20	–	20	–	25	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514256P/J/Z-85		TC514256P/J/Z-10		TC514256P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	65	–	65	–	75	–	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	120	–	135	–	160	–	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	80	–	85	–	100	–	ns	12
t_{CSR}	CAS Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	–	50	–	60	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to OE	20	–	20	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	–	25	–	30	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	25	0	25	0	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	30	–	ns	

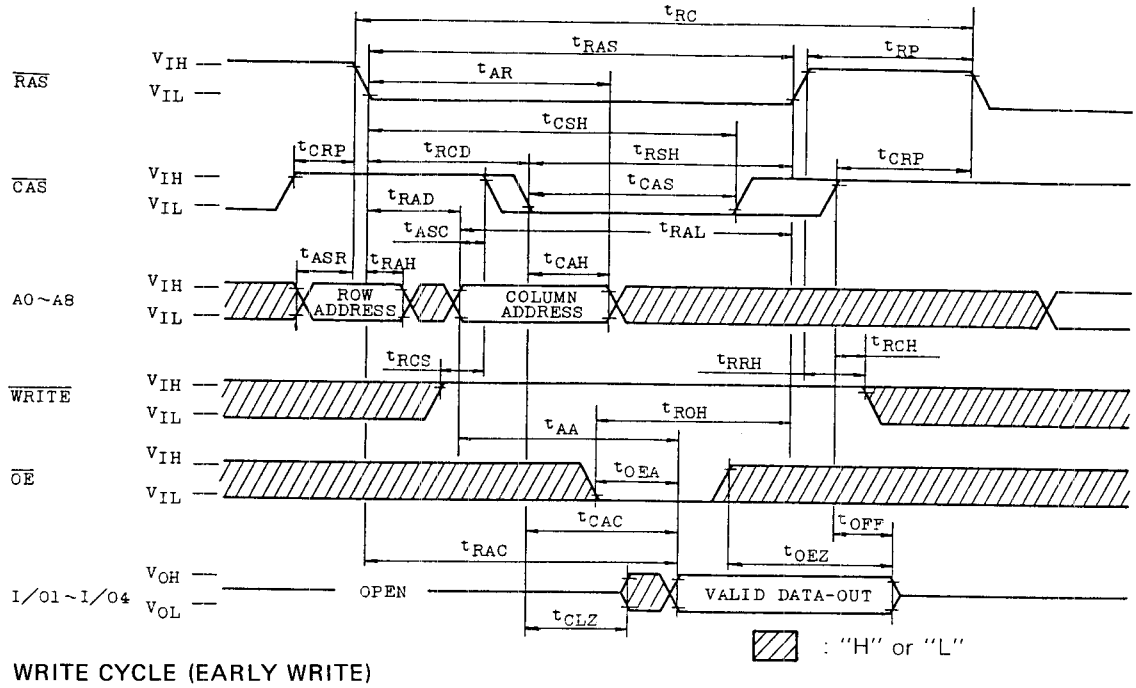
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1 MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{11}	Input Capacitance ($A_0 - A_8$)	–	5	pF
C_{12}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_0	Output Capacitance ($I/O_1 - I/O_4$)	–	7	pF

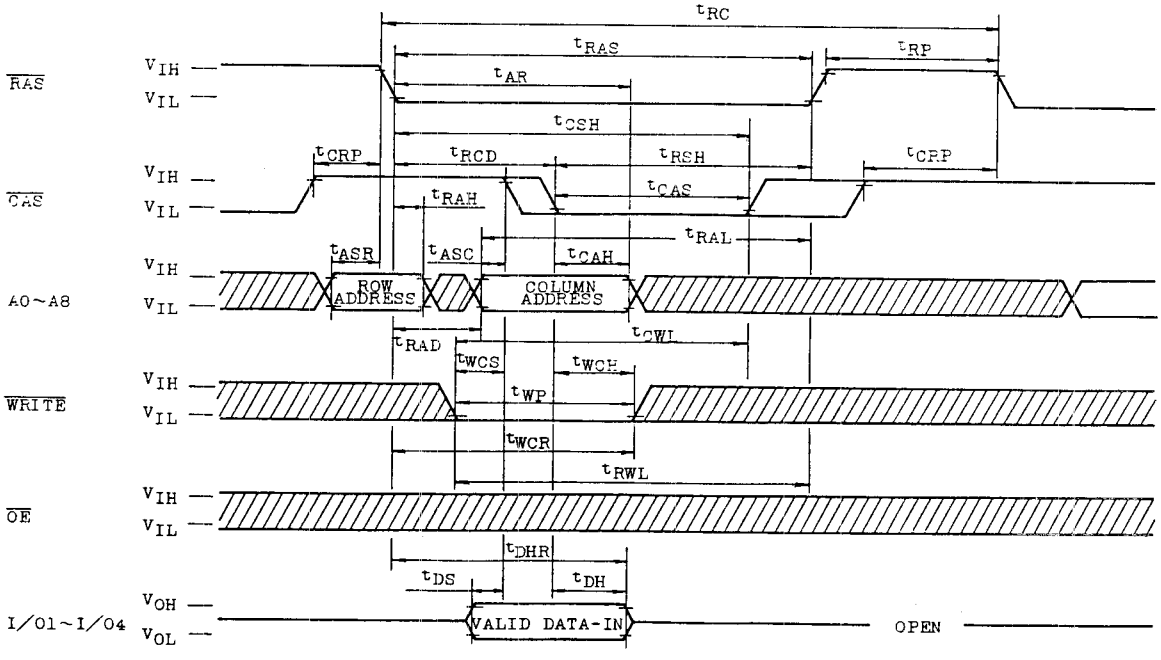
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

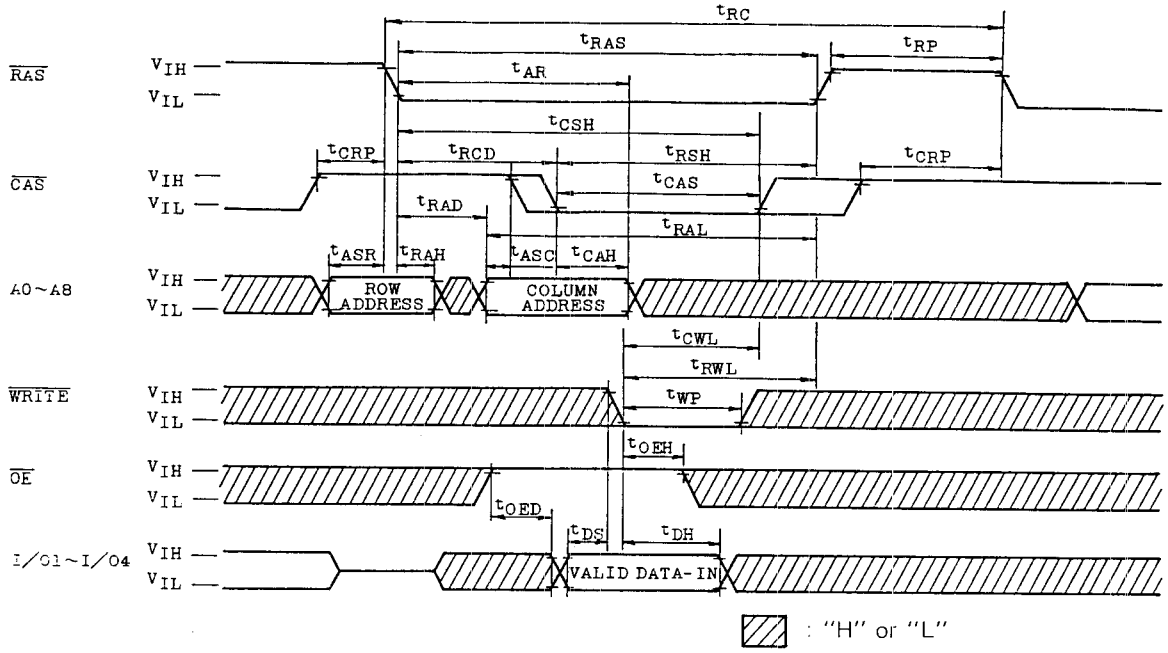
- READ CYCLE



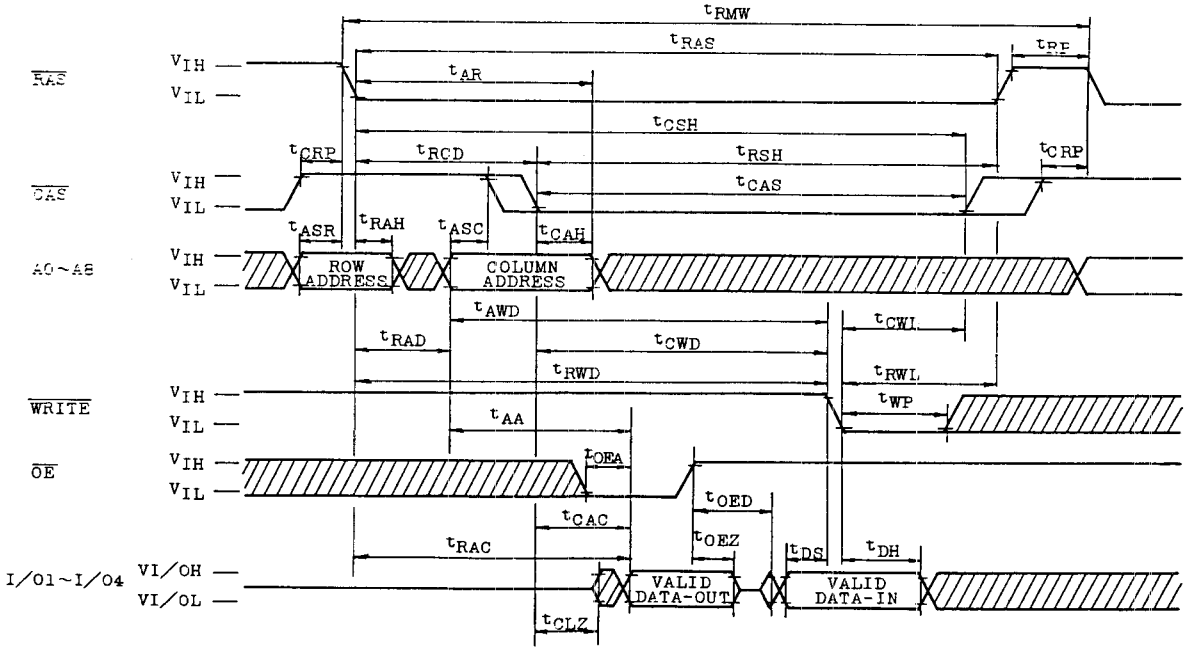
- WRITE CYCLE (EARLY WRITE)



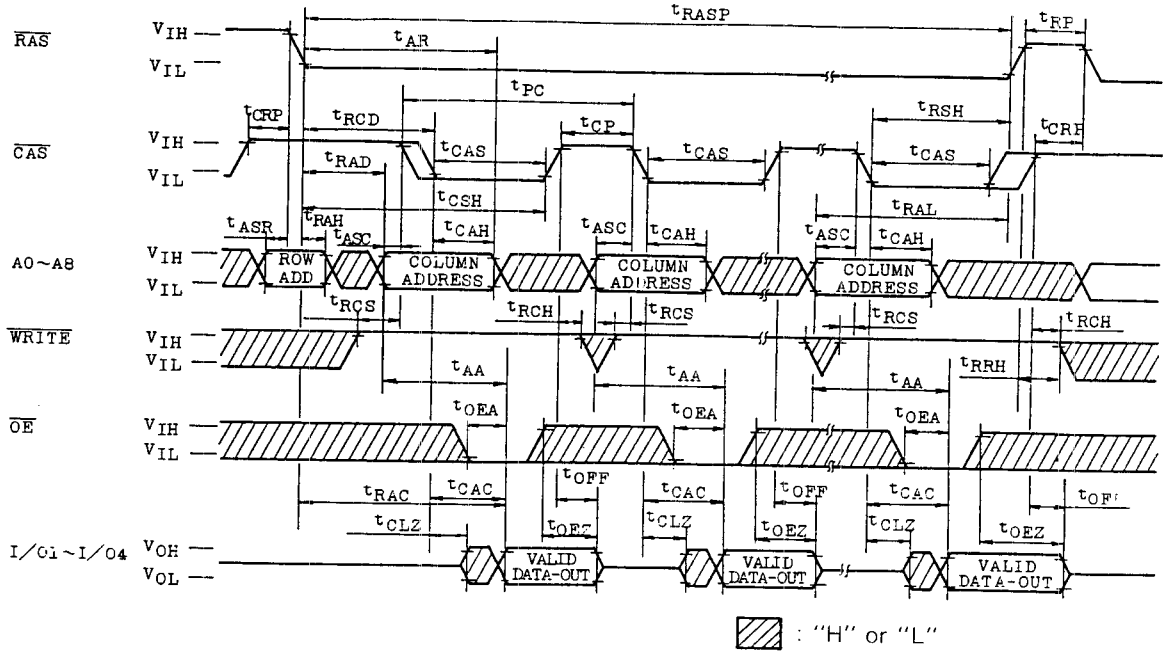
- WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



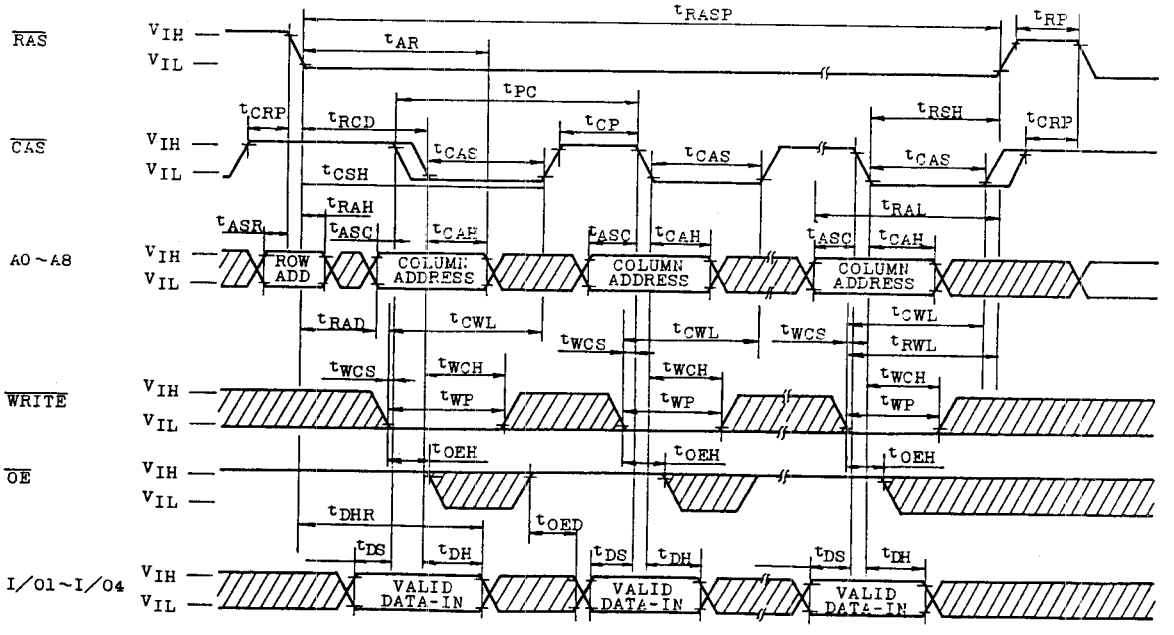
- READ-MODIFY-WRITE CYCLE



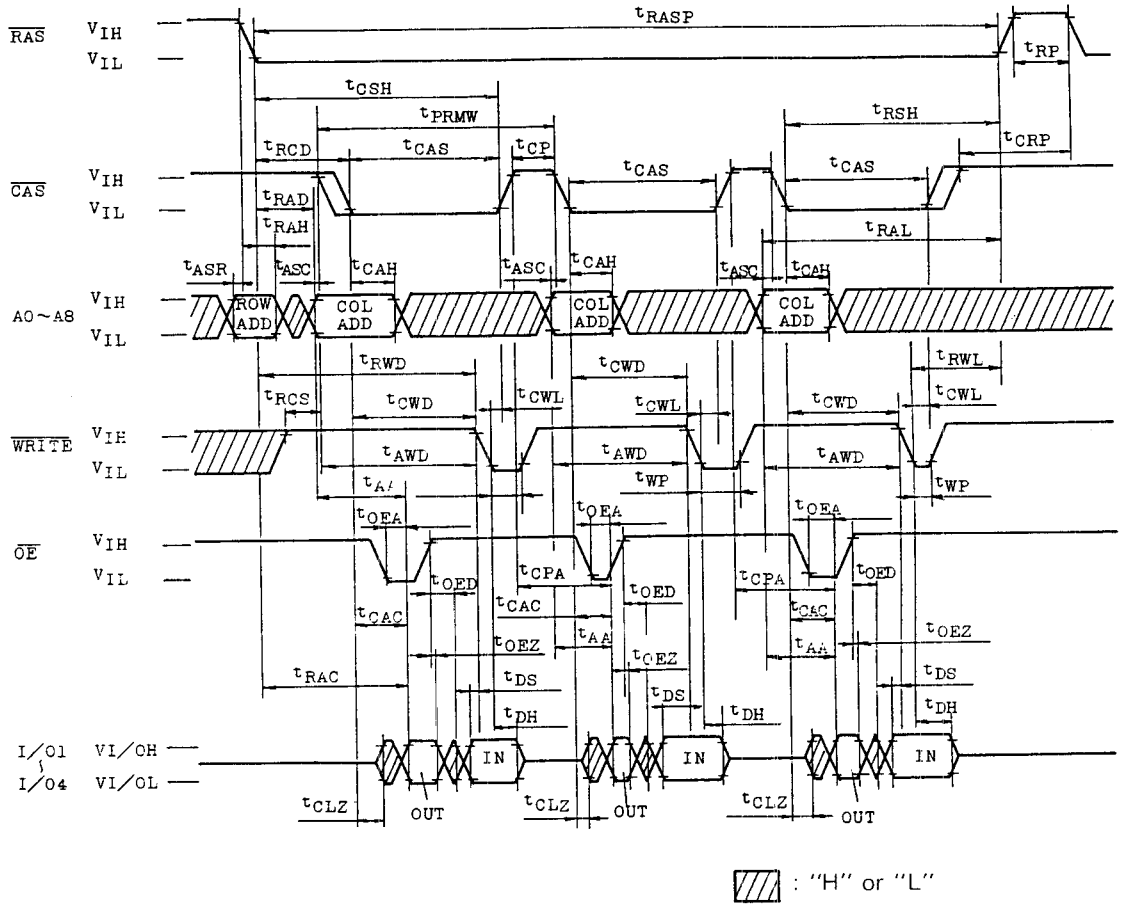
- FAST PAGE MODE READ CYCLE



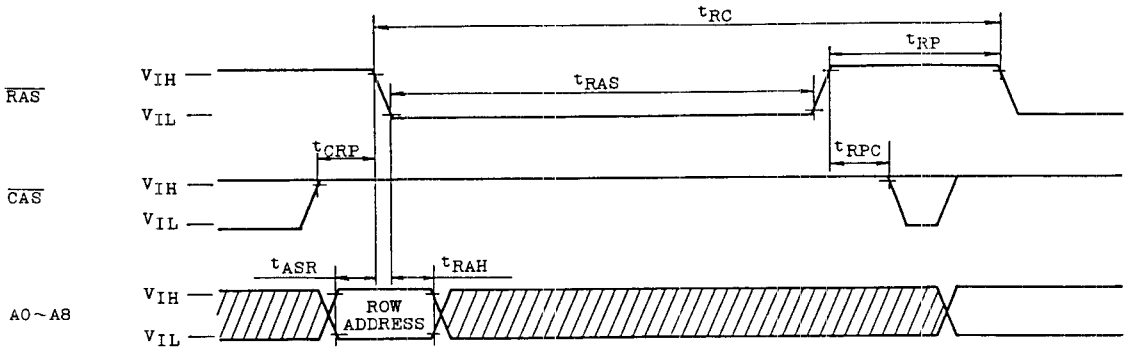
- FAST PAGE MODE WRITE CYCLE



- FAST PAGE MODE READ-MODIFY-WRITE CYCLE



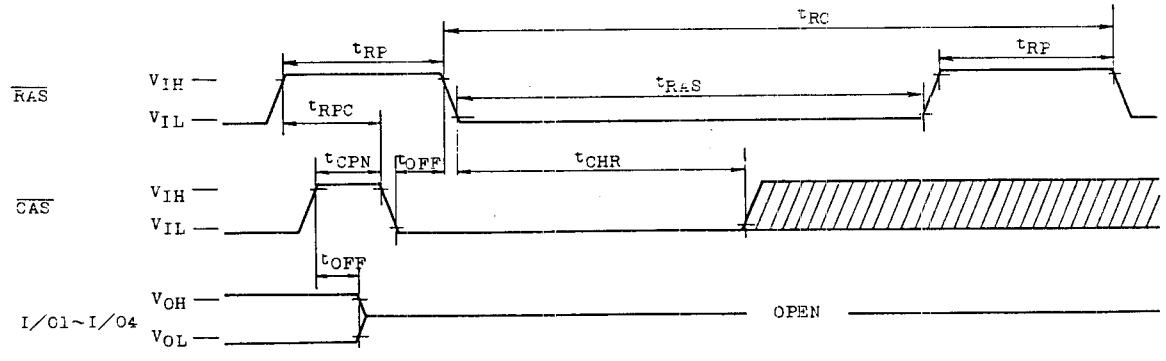
- $\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: WRITE, OE = Don't care

▨ : "H" or "L"

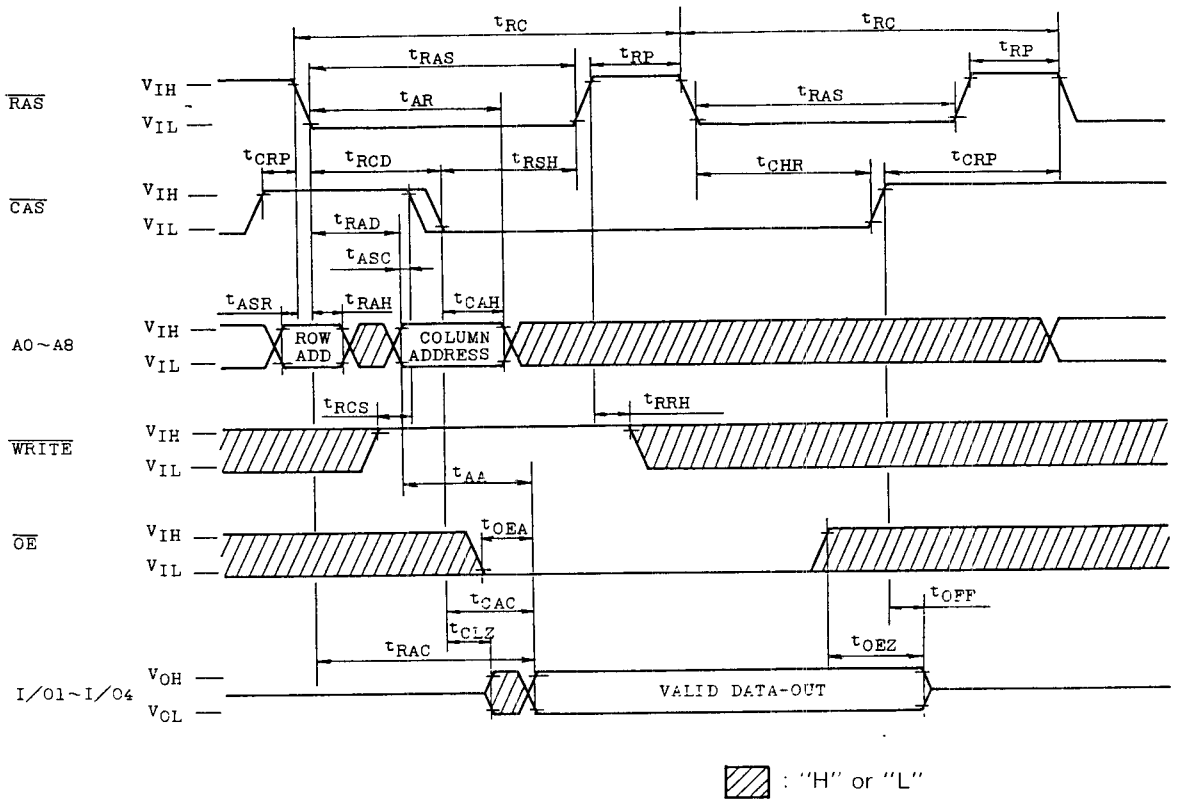
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



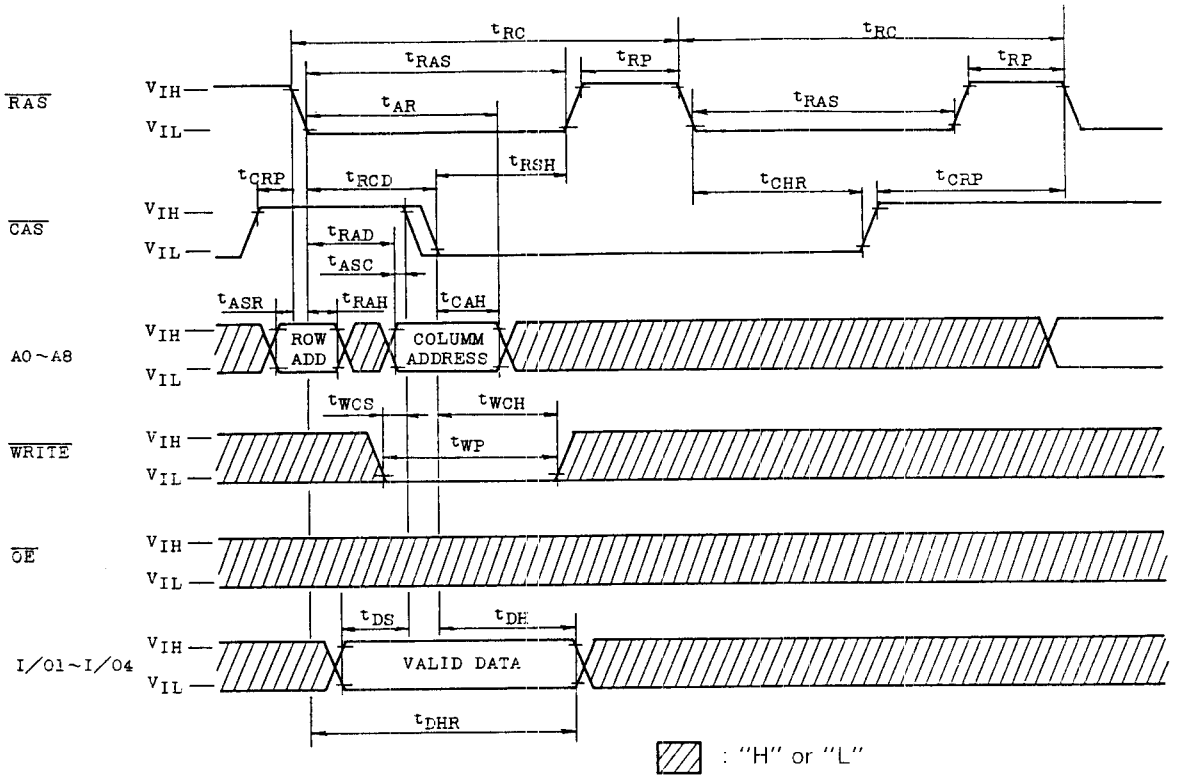
NOTE: WRITE, OE, A0 ~ A8 = "H" or "L"

▨ : "H" or "L"

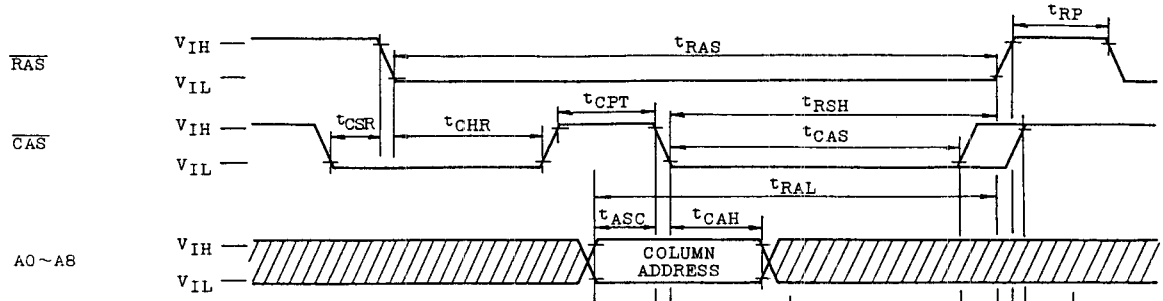
● HIDDEN REFRESH CYCLE (READ)



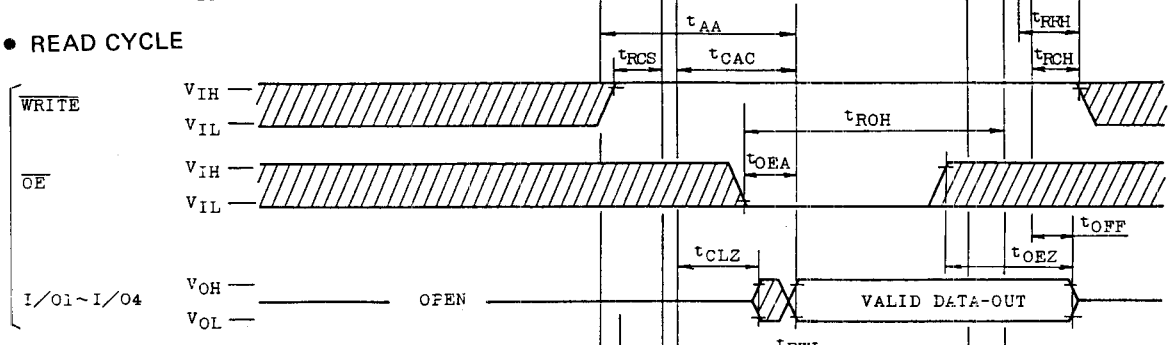
- HIDDEN REFRESH CYCLE (WRITE)



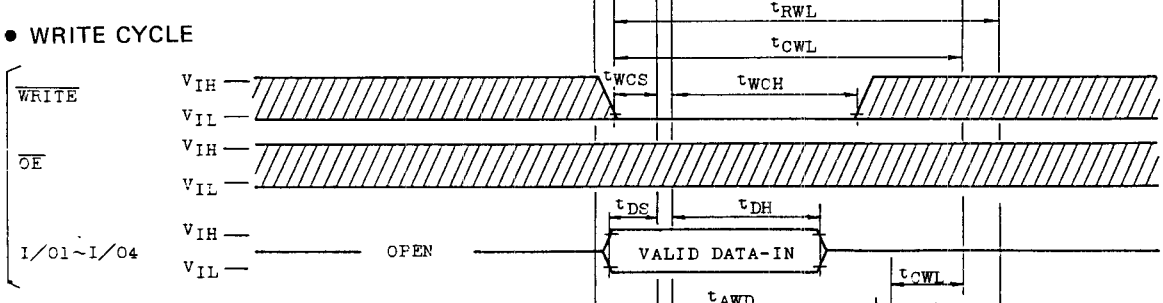
• $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



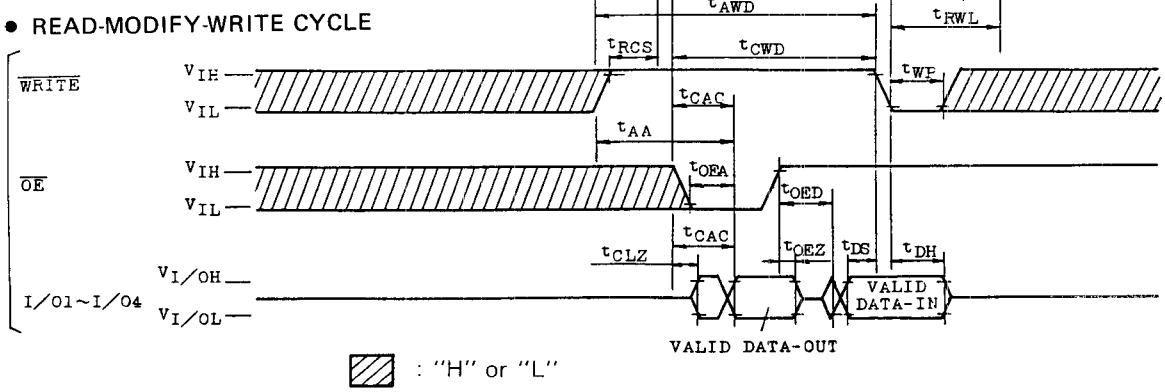
• READ CYCLE



• WRITE CYCLE



• READ-MODIFY-WRITE CYCLE

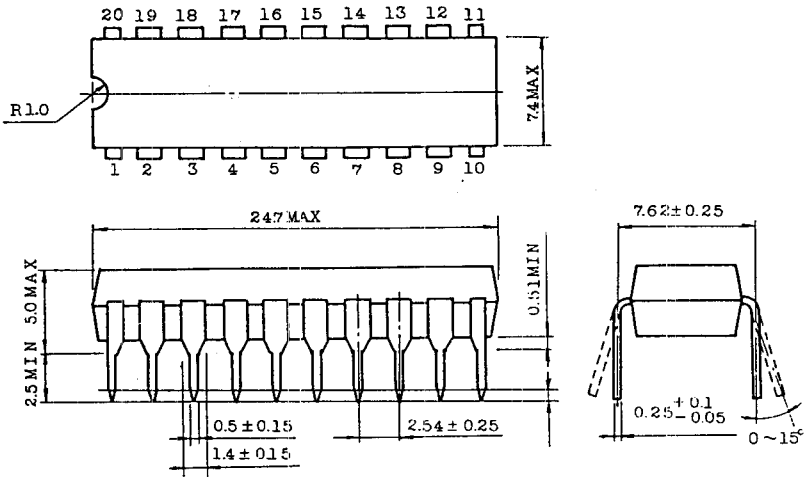


: "H" or "L"

OUTLINE DRAWINGS

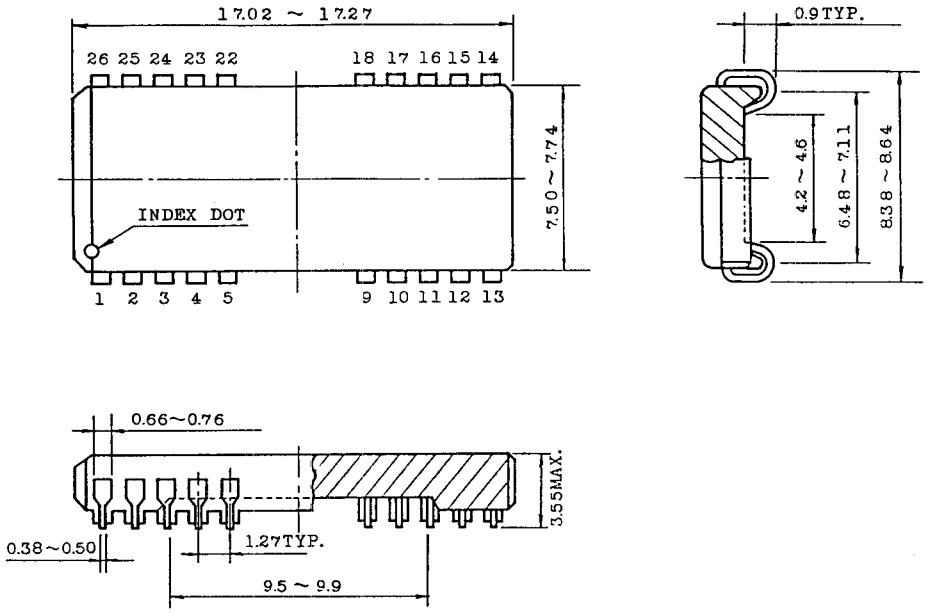
- Plastic DIP

Unit in mm



NOTE: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 20 leads.
All dimensions are in millimeters.

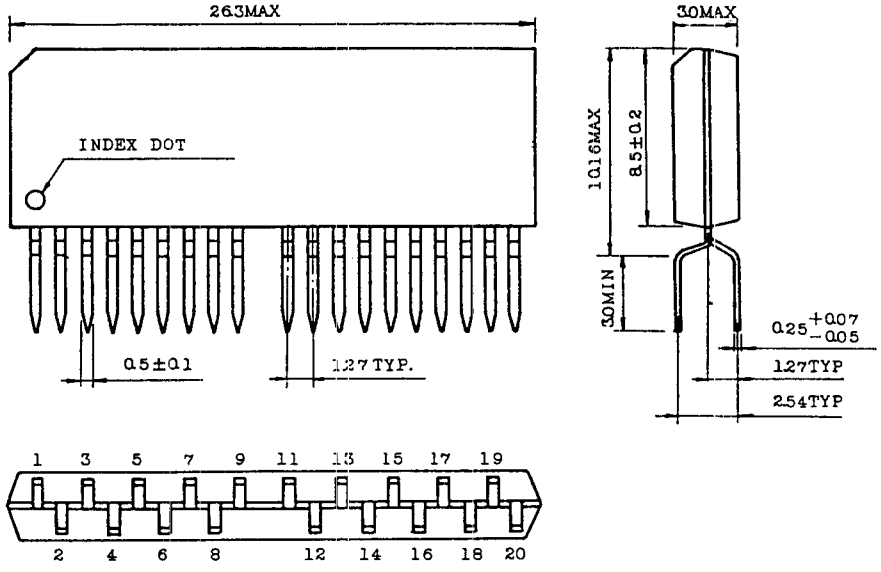
- Plastic SOJ



NOTE: Each lead pitch 1.27mm.
All dimensions are in millimeters.

- **Plastic ZIP**

Unit in mm

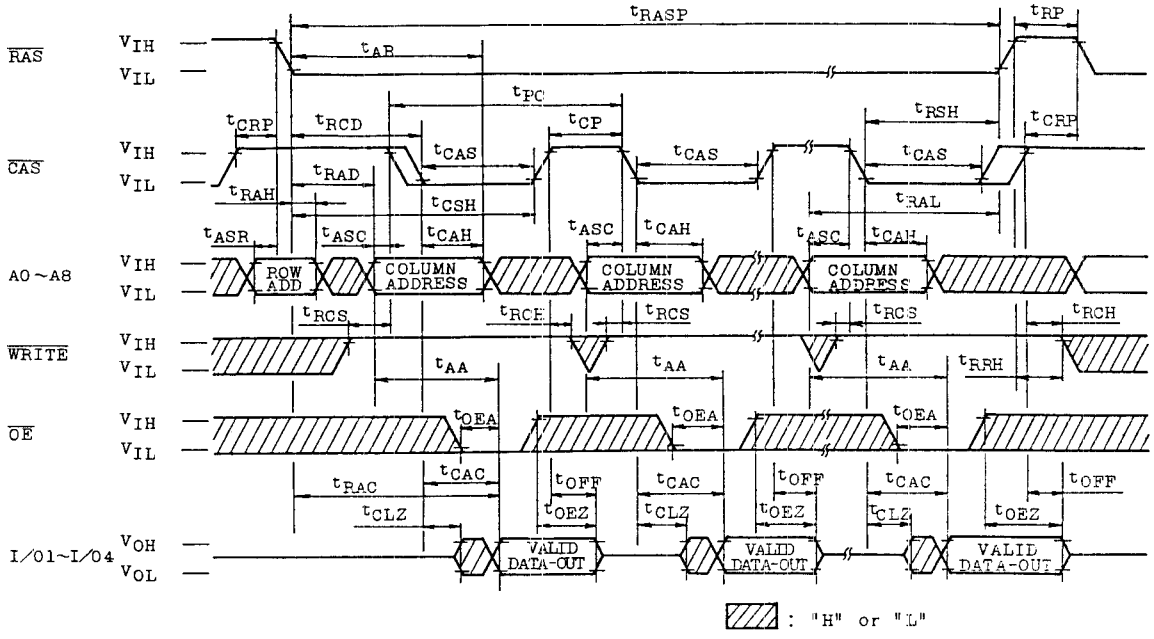


NOTE: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltages are referenced to V_{SS} .
3. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} , I_{CC7} depend on cycle rate.
4. I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. t_{RAS}(max.) = 1μs is only applied to refresh of battery-back up. t_{RAS}(max.) = 10μs is applied to functional operating.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume t_T = 5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

- FAST PAGE MODE READ CYCLE



- FAST PAGE MODE WRITE CYCLE