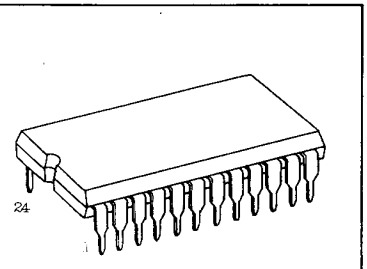
TC4036BP 4 WORD × 8 BIT STATIC RAM (BINARY ADDRESSING)
TC4039BP 4 WORD × 8 BIT STATIC RAM (DIRECT WORD-LINE ADDRESSING)

TC4036BP/TC4039BP are static RAM of 4 × 8 bits and since eight data input/output lines are mutually independently provided for one word, wide variety of applications are expected for scratch pad memories, channel preset memories of digital frequency synthesizer systems, etc.

TC4036BP Each word is binarily selected by two lines of address inputs A_0 and A_1.

TC4039BP Each word is directly selected by mutually independent four lines of address inputs WORD 1 through WORD 4.



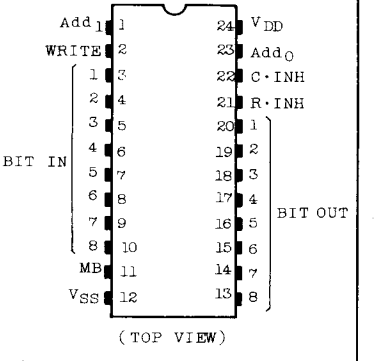
DIP 24 (6D24A-P)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

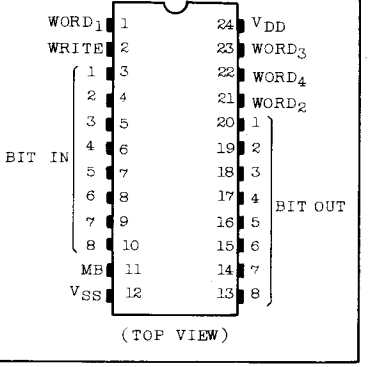
PIN ASSIGNMENT

TC4036BP



(TOP VIEW)

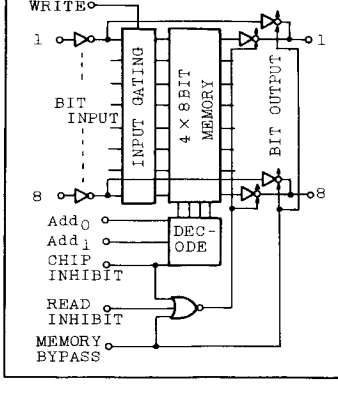
TC4039BP



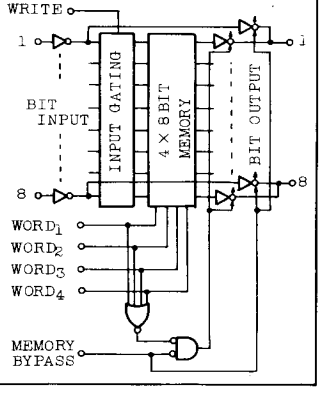
(TOP VIEW)

BLOCK DIAGRAM

TC4036BP



TC4039BP



FUNCTION TABLE

TC4036BP

WRITE	READ INHIBIT	MEMORY BYPASS	CHIP INHIBIT	OPERATIONAL MODEL
*	*	L	H	Each bit output has high impedance generating floating condition. Writing into the memory is not performed.
*	*	H	H	Bit input data is directly output to the corresponding bit output. The memory retains the content of bit input data written in previous write mode.
L	*	H	L	
H	*	H	L	Bit input data is directly output to the corresponding bit output. But input data is written into the word memory designated by address inputs A_0 and A_1.
L	L	L	L	Memory data is read from the word designated by address inputs A_0 and A_1. Writing into the memory is not performed.
L	H	L	L	Each bit output has high impedance generating floating condition. Writing into the memory is not performed.
H	L	L	L	As well as each bit input data is written into the word memory designated by address inputs A_0 and A_1, the input data is read out.
H	H	L	L	Each bit output has high impedance generating floating condition. Each bit input data is written into the word memory designated by address inputs A_0 and A_1.

TC4039BP

WRITE	MEMORY BYPASS	WORD1 ~ WORD4	OPERATIONAL MODE
*	L	all L	Each bit output has high impedance generating floating condition. The memory retains the content of bit input data written in previous write mode.
*	H	all L	Bit input data is directly output to the corresponding bit output. The memory retains the content of bit input data written in previous write mode.
L	H	△△	
H	H	△△	Bit input data is directly output to the corresponding bit output. Each bit input data is written into the memory designated by the word input.
L	L	△△	Memory data designated by the word input is read out. Writing into the memory is not performed.
H	L	△△	As well as each bit input data is written into the memory designated by the word input, the input data is read out.

* Don't care △△ Only one WORD input has "H" level.

ADDRESS TRUTH TABLE

TC4036BP

Add_1	Add_0	ADDRESSED WORD
L	L	WORD 1
L	H	WORD 2
H	L	WORD 3
H	H	WORD 4

TC4039BP

WORD 1	WORD 2	WORD 3	WORD 4	ADDRESSED WORD
H	L	L	L	WORD 1
L	H	L	L	WORD 2
L	L	H	L	WORD 3
L	L	L	H	WORD 4
L	L	L	L	NONE
OTHER STATES				*

※ Inhibit mode

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V, 13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V, 13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\| < 1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
3-State Output Leakage Current	"H" Level	I_{DH}	V_{OUT}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{OUT}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	5	-	0.005	5	-	150	μA
				10	-	10	-	0.010	10	-	300	
				15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

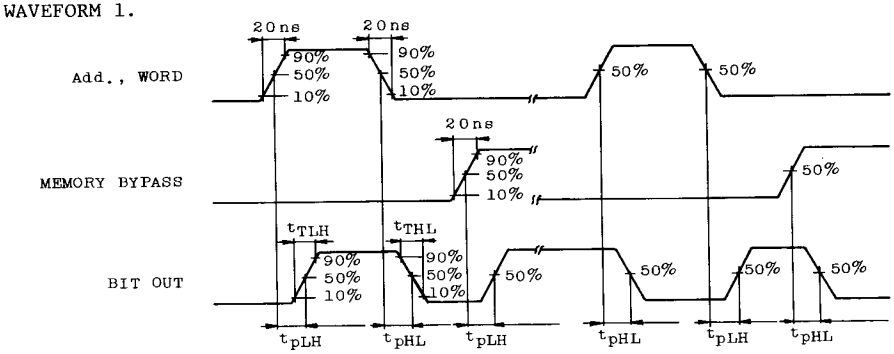
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

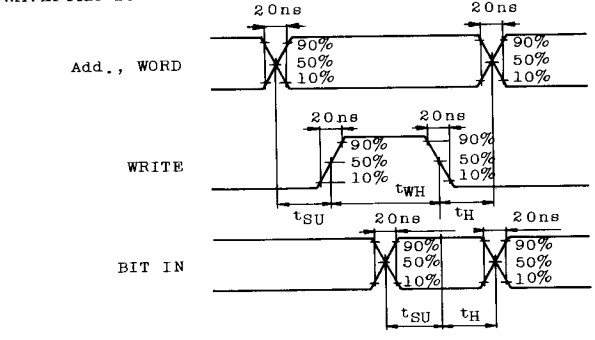
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (R·INH - BIT OUT) (TC4036BP)	t_{pZL} t_{pZH}	R_L=1kΩ	5	-	200	750	ns
			10	-	90	350	
			15	-	70	300	
Propagation Delay Time (C·INH - BIT OUT) (TC4036BP)	t_{pZL} t_{pZH}	R_L=1kΩ	5	-	250	750	ns
			10	-	120	350	
			15	-	90	300	
Propagation Delay Time (M·B - BIT OUT)	t_{pLH} t_{pHL}		5	-	210	750	ns
			10	-	100	350	
			15	-	80	300	
Propagation Delay Time (Add.WORD - BIT OUT)	t_{pLH} t_{pHL}		5	-	260	750	ns
			10	-	110	350	
			15	-	80	300	
Min. Set-up Time (Add. WORD - WRITE)	t_{SU}		5	-	45	200	ns
			10	-	25	110	
			15	-	20	60	
Min. Hold Time (Add. WORD - WRITE)	t_H		5	-	-60	100	ns
			10	-	-35	70	
			15	-	-25	40	
Min. Pulse Width (WRITE)	t_{WH}		5	-	60	150	ns
			10	-	20	60	
			15	-	15	50	
Min. Set-up Time (BIT IN - WRITE)	t_{SU}		5	-	-20	100	ns
			10	-	-15	50	
			15	-	-10	40	
Min. Hold Time (BIT IN - WRITE)	t_H		5	-	40	200	ns
			10	-	25	90	
			15	-	20	60	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1.



WAVEFORM 2.



WAVEFORM 3. (TC4036BP)