

R1LV1616R Series

16Mb Advanced LPSRAM (1M wordx16bit / 2M wordx8bit)

REJ03C0101-0400Z

Rev.4.00

2007.09.12

Description

The R1LV1616R Series is a family of low voltage 16-Mbit static RAMs organized as 1048576-words by 16-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies.

The R1LV1616R Series is suitable for memory applications where a simple interfacing , battery operating and battery backup are the important design objectives.

The R1LV1616R Series is packaged in a 52pin micro thin small outline mount device[μTSOP / 10.79mm x 10.49mm with the pin-pitch of 0.4mm], a 48pin thin small outline mount device[TSOP / 12mm x 20mm with the pin-pitch of 0.5mm] or a 48balls fine pitch ball grid array [f-BGA / 7.5mmx8.5mm with the ball-pitch of 0.75mm and 6x8 array] . It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

Features

- Single 2.7-3.6V power supply
- Small stand-by current:2μA (3.0V, typ.)
- Data retention supply voltage =2.0V
- No clocks, No refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion by CS1#, CS2, LB# and UB#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention on the I/O bus
- Process technology: 0.15um CMOS

Ordering Information

Type No.	Access time	Package
R1LV1616RSD-5S%	55 ns (Note0)	350-mil 52-pin plastic μ - TSOP(II) (normal-bend type) (52PTG)
R1LV1616RSD-7S%	70 ns	
R1LV1616RSD-8S%	85 ns	
R1LV1616RBG-5S%	55 ns (Note0)	7.5mmx8.5mm f-BGA 0.75mm pitch 48ball
R1LV1616RBG-7S%	70 ns	
R1LV1616RBG-8S%	85 ns	
R1LV1616RSA-5S%	55 ns (Note0)	12mm x 20mm plastic TSOP(I) (normal-bend type) (48P3R)
R1LV1616RSA-7S%	70 ns	
R1LV1616RSA-8S%	85 ns	

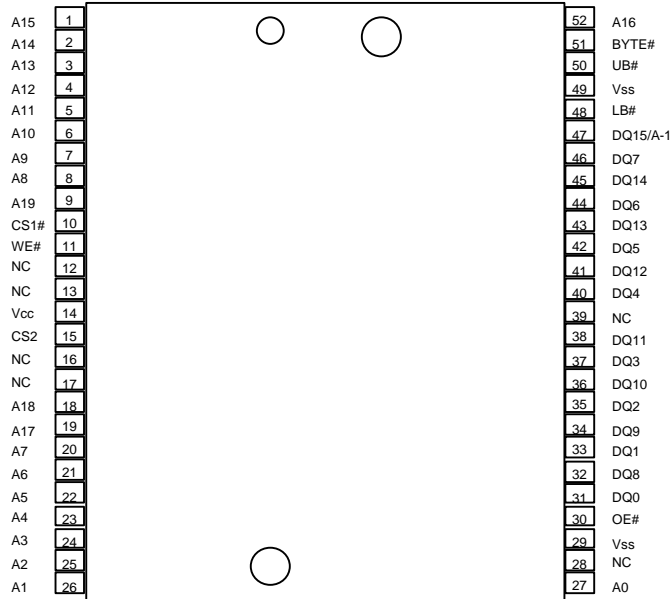
Note0. 55ns parts can be supported under the condition of the input timing limitation toward SRAM on customer's system. Please contact our sales office in your region, in case of the inquiry for 55ns parts.

% - Temperature version; see table below

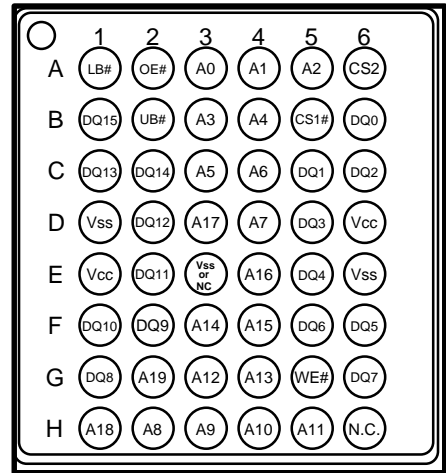
%	Temperature Range
R	0 ~ +70 °C
I	-40 ~ +85 °C

Pin Arrangement

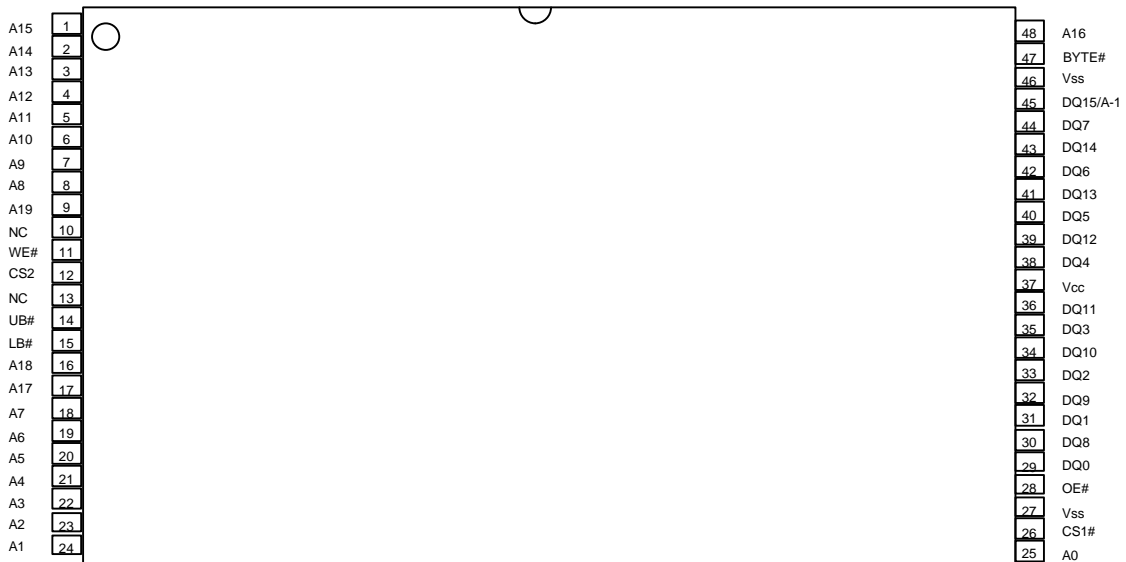
52-pin μ T SOP



48-pin fBGA

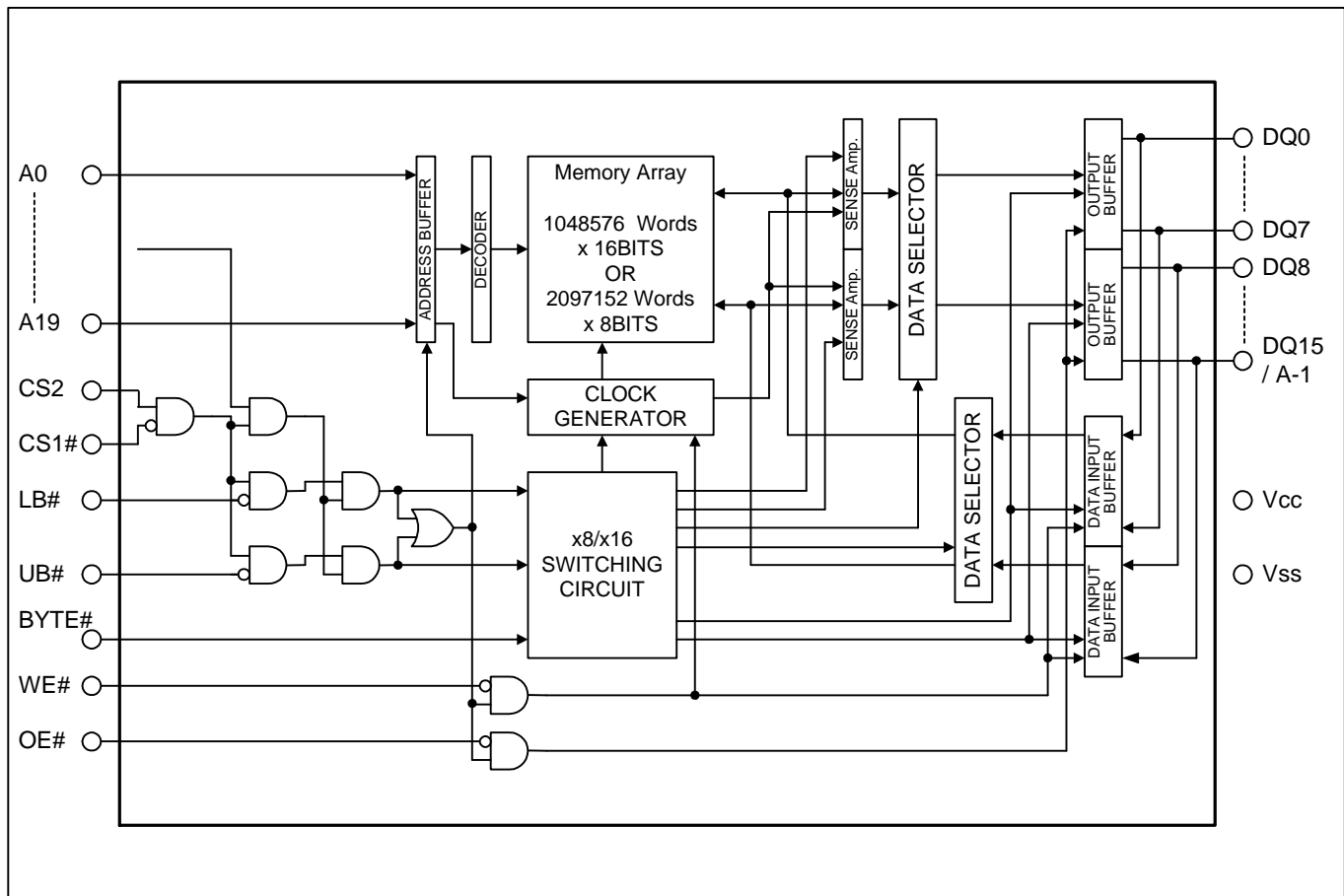


48-pin TSOP



Pin Description	
Pin name	Function
A0 to A19	Address input
DQ 0 to DQ15	Data input/output
CS1# & CS2	Chip select
WE#	Write enable
OE#	Output enable
LB#	Lower byte select
UB#	Upper byte select
Vcc	Power supply
Vss	Ground
BYTE#	Byte (x8 mode) enable input
NC	Non connection

Block Diagram



Note. BYTE# pin supported by only TSOP and uTSOP types.

Operating Table

CS1#	CS2	BYTE#	LB#	UB#	WE#	OE#	DQ0-7	DQ8-14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand by
L	H	H	L	H	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	L	H	H	L	Dout	High-Z	High-Z	Read from lower byte
L	H	X	X	X	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	H	L	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	H	L	H	L	High-Z	Dout	Dout	Read from upper byte
L	H	H	L	L	L	X	Din	Din	Din	Write
L	H	H	L	L	H	L	Dout	Dout	Dout	Read
L	H	L	L	L	L	X	Din	High-Z	A-1	Write
L	H	L	L	L	H	L	Dout	High-Z	A-1	Read

Note 1. H:VIH L:VIL X: VIH or VIL

2. BYTE# pin supported by only TSOP and uTSOP types. When apply BYTE#="L", please assign LB#=UB#="L".

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	
Power supply voltage relative to Vss	Vcc	-0.5 to +4.6	V	
Terminal voltage on any pin relation toVss	V _T	-0.5* ¹ to Vcc+0.3* ²	V	
Power dissipation	P _T	0.7	W	
Operation temperature	T _{opr}	R ver.	0 to +70	°C
		I ver.	-40 to +85	°C
Storage temperature	T _{stg}	-65 to +150	°C	
Storage temperature range under bias	T _{bias}	R ver.	0 to +70	°C
		I ver.	-40 to +85	°C

Note 1. -2.0V in case of AC (Pulse width ≤ 30ns)

2. Maximum voltage is +4.6V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note	
Supply voltage	V _{CC}	2.7	3.0	3.6	V		
	V _{SS}	0	0	0	V		
Input high voltage	V _{IH}	2.4	-	V _{CC} +0.2	V		
Input low voltage	V _{IL}	-0.2	-	0.4	V	1	
Ambient temperature range	R ver.	T _a	0	-	+70	°C	2
	I ver.		-40	-	+85	°C	2

Note 1. -2.0V in case of AC (Pulse width ≤ 30ns)

2. Ambient temperature range depends on R/I-version. Please see table on page 2.

DC Characteristics

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test conditions*2	
Input leakage current	I _{LI}	-	-	1	μA	V _{in} =V _{SS} to V _{CC}	
Output leakage current	I _{LO}	-	-	1	μA	CS1# =V _{IH} or CS2=V _{IL} or OE# = V _{IH} or WE# =V _{IL} or LB# =UB# =V _{IH} , V _{I/O} =V _{SS} to V _{CC}	
Average operating current	I _{CC1}	-	25	40	mA	Min. cycle, duty =100% I _{I/O} = 0 mA, CS1# =V _{IL} , CS2=V _{IH} Others = V _{IH} / V _{IL}	
	I _{CC2}	-	2	5	mA	Cycle time = 1 μs, I _{I/O} = 0 mA, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V V _{IH} ≥ V _{CC} -0.2V, V _{IL} ≤ 0.2V, duty=100%	
Standby current	I _{SB}	-	0.1	0.3	mA	CS2=V _{IL}	
Standby current	I _{SB1}	-	2	6	μA	~+25°C	V _{in} ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS2 ≥ V _{CC} -0.2V, CS1# ≥ V _{CC} -0.2V or (3) LB# =UB# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V, CS1# ≤ 0.2V Average value
		-	4	12	μA	~+40°C	
		-	-	25	μA	~+70°C	
		-	-	40	μA	~+85°C	
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -1mA	
Output Low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA	

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (T_a = 25°C), and not 100% tested.

2. BYTE# pin supported by only TSOP and uTSOP types.

BYTE# ≥ V_{CC}-0.2V or BYTE# ≤ 0.2V

Capacitance

(Ta = +25°C, f = 1MHz)

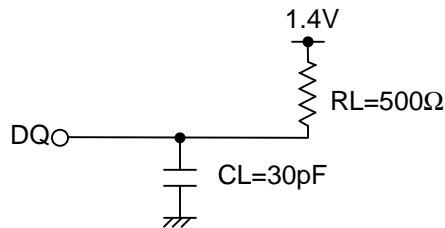
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	-	-	10	pF	V in = 0V	1
Input / output capacitance	C I/O	-	-	10	pF	V I/O = 0V	1

Note 1: This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc=2.7~3.6V, Ta = 0~+70°C / -40~+85°C *)

- Input pulse levels: VIL= 0.4V, VIH=2.4V
- Input rise and fall time : 5ns
- Input and output timing reference levels : 1.4V
- Output load : See figures (Including scope and jig)



Note: Temperature range depends on R/I-version. Please see table on page 2.

Read Cycle

Parameter	Symbol	R1LV1616R**- 5S (Note0)		R1LV1616R**- 7S		R1LV1616R**- 8S		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	55	-	70	-	85	-	ns	
Address access time	t_{AA}	-	70	-	70	-	85	ns	
Chip select access time	t_{ACS1}	-	55	-	70	-	85	ns	
	t_{ACS2}	-	55	-	70	-	85	ns	
Output enable to output valid	t_{OE}	-	35	-	35	-	45	ns	
Output hold from address change	t_{OH}	10	-	10	-	10	-	ns	
LB#,UB# access time	t_{BA}	-	55	-	70	-	85	ns	
Chip select to output in low-Z	t_{CLZ}	10	-	10	-	10	-	ns	2,3
LB#,UB# enable to low-Z	t_{BLZ}	5	-	5	-	5	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	5	-	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	0	25	0	30	ns	1,2,3
	t_{CHZ2}	0	20	0	25	0	30	ns	1,2,3
LB#,UB# disable to high-Z	t_{BHZ}	0	20	0	25	0	30	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	0	30	ns	1,2,3

Write Cycle

Parameter	Symbol	R1LV1616R**-5S (Note0)		R1LV1616R**-7S		R1LV1616R**-8S		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	55	-	70	-	85	-	ns	
Address valid to end of write	t_{AW}	50	-	65	-	70	-	ns	
Chip selection to end of write	t_{CW}	55	-	65	-	70	-	ns	5
Write pulse width	t_{WP}	40	-	55	-	60	-	ns	4
LB#,UB# valid to end of write	t_{BW}	50	-	65	-	70	-	ns	
Address setup time	t_{AS}	0	-	0	-	0	-	ns	6
Write recovery time	t_{WR}	0	-	0	-	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	35	-	40	-	ns	
Data hold from write time	t_{DH}	0	-	0	-	0	-	ns	
Output active from end of write	t_{OW}	5	-	5	-	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	0	30	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	0	25	0	30	ns	1,2

Note0. 55ns parts can be supported under the condition of the input timing limitation toward SRAM on customer's system. Please contact our sales office in your region, in case of the inquiry for 55ns parts.

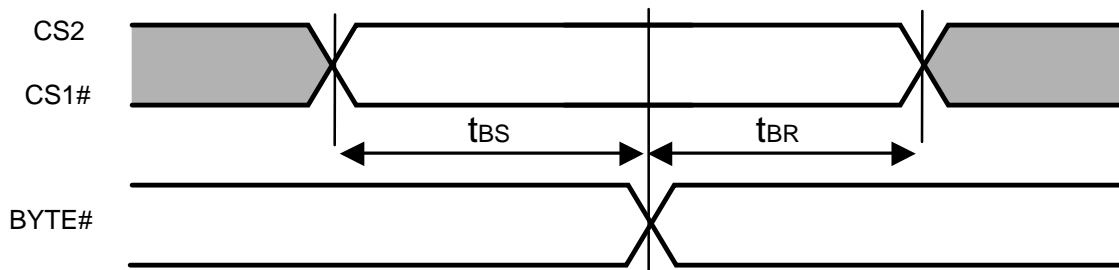
In case of $t_{AA} = 70ns$, $t_{RC} = 70ns$.

1. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. AT any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and form device to device.
4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low . A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS1# going low or CS2 going high to end of write.
6. t_{AS} is measured the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

Byte enable (supported by only 48-pin TSOP and 52-pin μ TSOP)

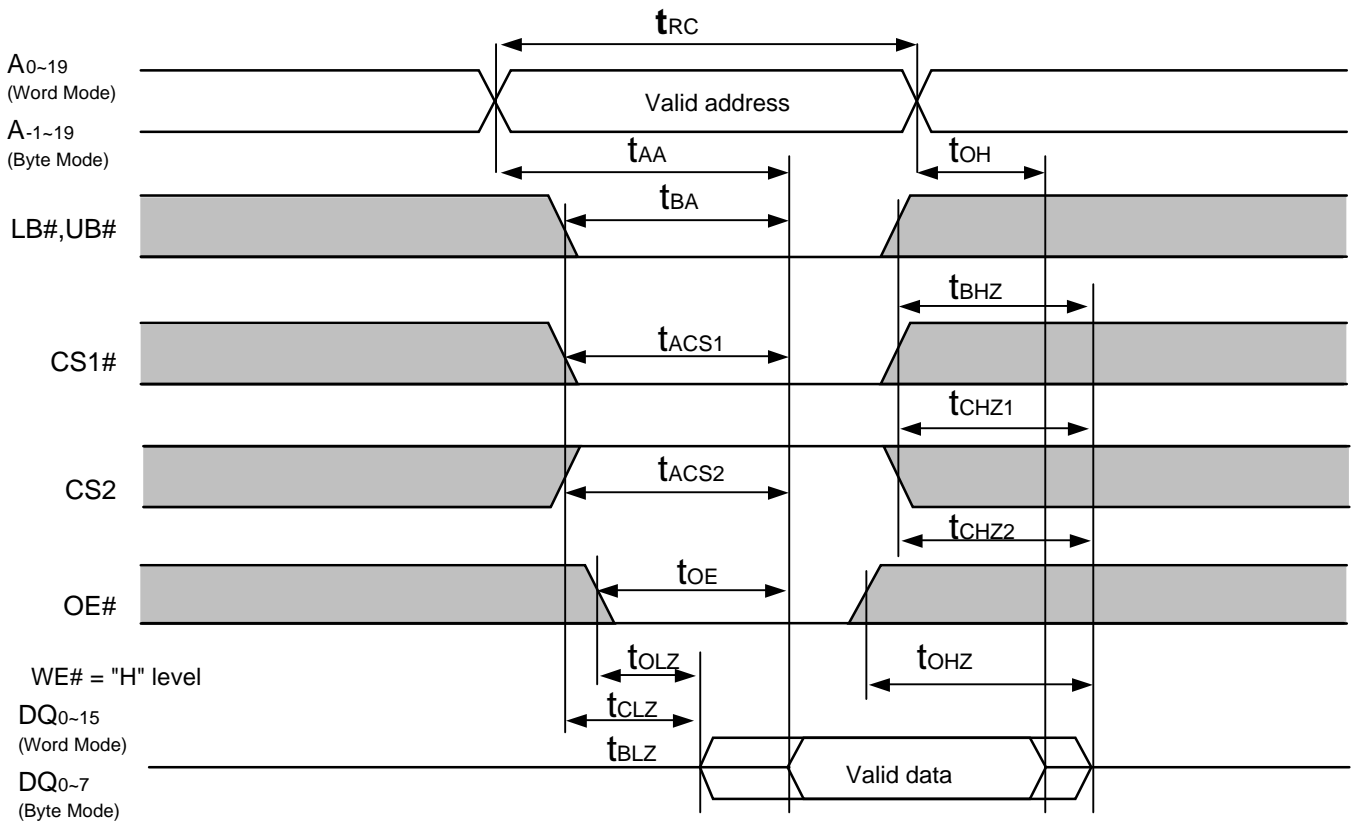
Parameter	Symbol	R1LV1616R**-5S		R1LV1616R**-7S		R1LV1616R**-8S		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Byte setup time	t_{BS}	5	-	5	-	5	-	ms	
Byte recovery time	t_{BR}	5	-	5	-	5	-	ms	

BYTE# Timing Waveform

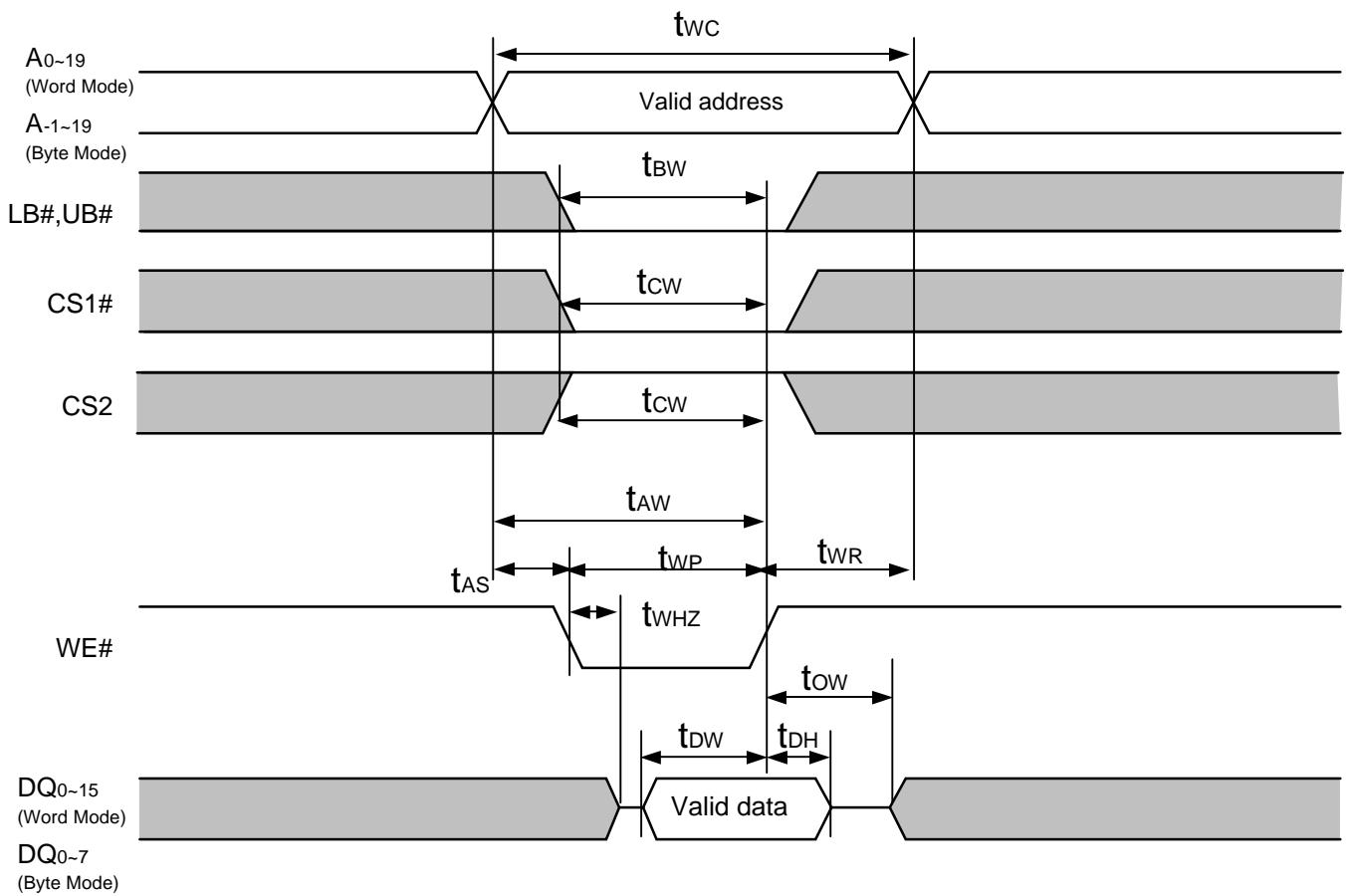


Timing Waveform

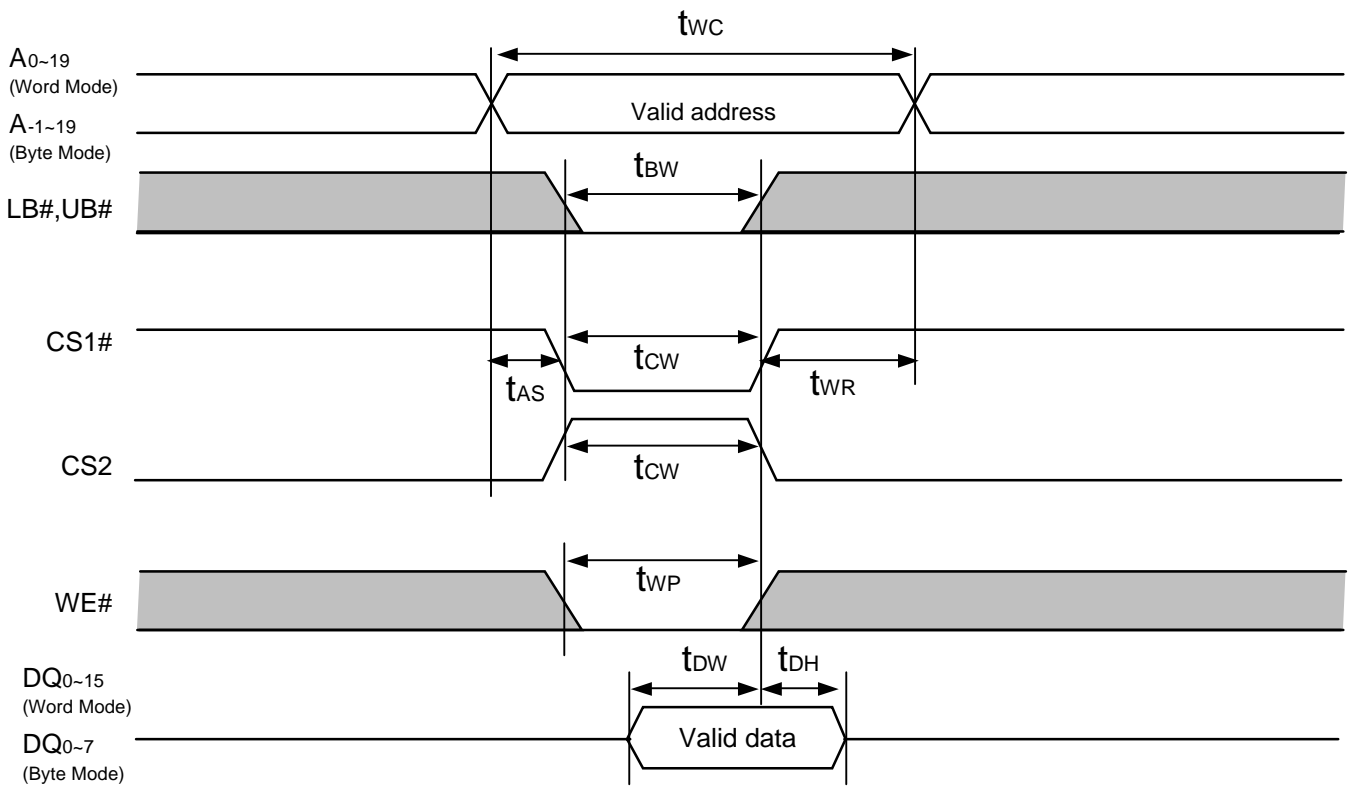
Read Cycle



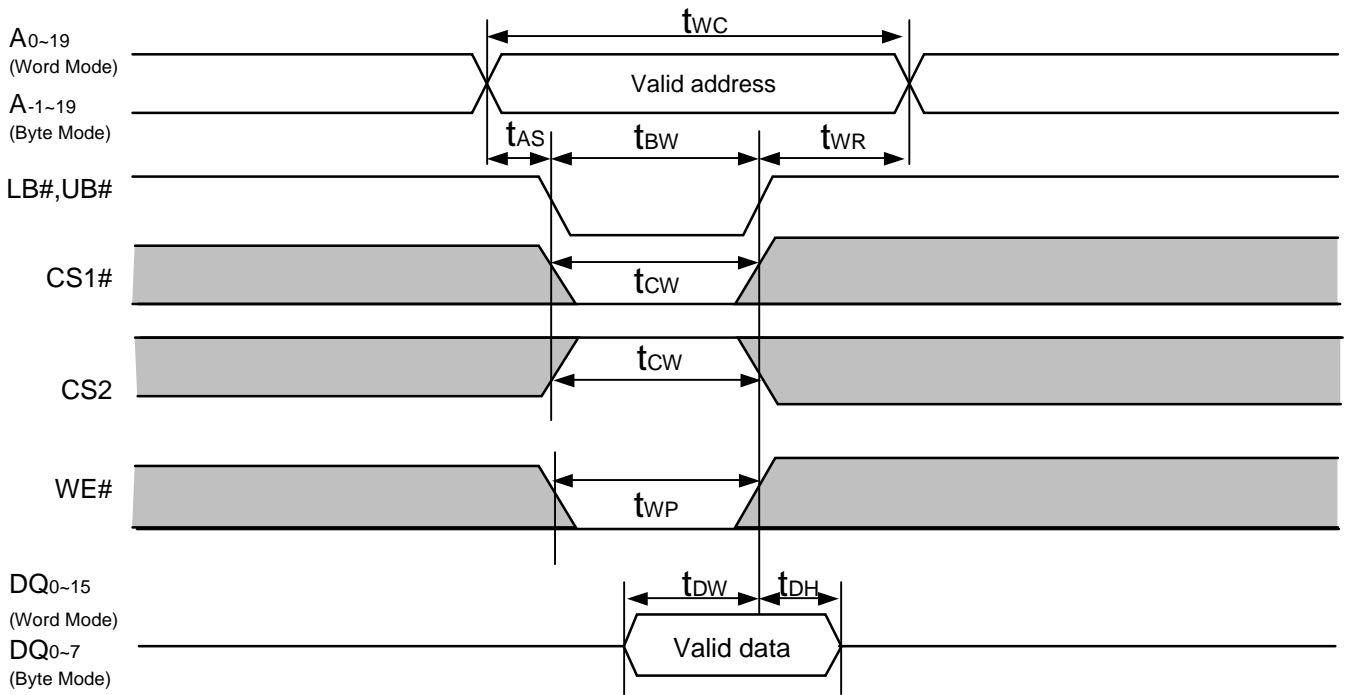
Write Cycle (1) (WE# Clock)



Write Cycle (2) (CS1# ,CS2 Clock, OE#=V_{IH})



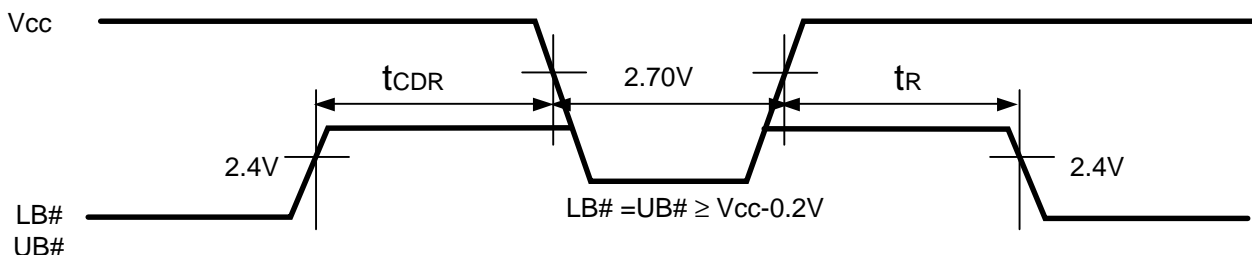
Write Cycle (3) (LB#,UB# Clock, OE#=VIH)



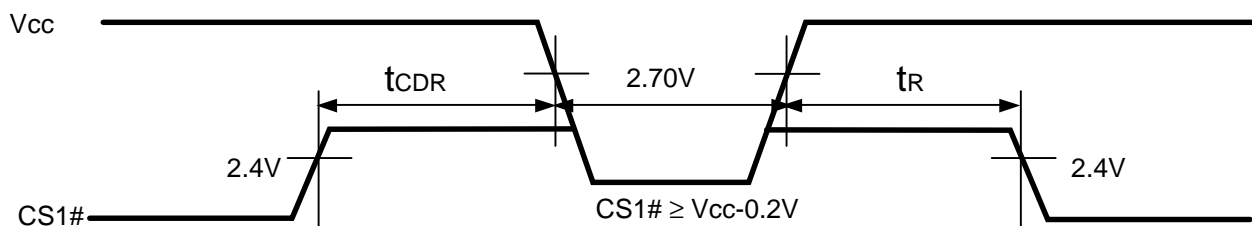
Data Retention Characteristics							
Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test conditions*2,3	
Vcc for data retention	V _{DR}	2.0	-	3.6	V	V _{in} ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS2 ≥ V _{cc} -0.2V, CS1# ≥ V _{cc} -0.2V or (3) LB# =UB# ≥ V _{cc} -0.2V, CS2 ≥ V _{cc} -0.2V, CS1# ≤ 0.2V	
Data retention current	I _{CCDR}	-	2	6	μA	~+25°C	V _{cc} =3.0V, V _{in} ≥0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS2 ≥ V _{cc} -0.2V, CS1# ≥ V _{cc} -0.2V or (3) LB# =UB# ≥ V _{cc} -0.2V, CS2 ≥ V _{cc} -0.2V, CS1# ≤ 0.2V Average value
		-	4	12	μA	~+40°C	
		-	-	25	μA	~+70°C	
		-	-	40	μA	~+85°C	
Chip deselect to data retention time	t _{CDR}	0	-	-	ns	See retention waveform	
Operation recovery time	t _R	5	-	-	ms		

Note 1. Typical parameter of I_{CCDR} indicates the value for the center of distribution at V_{cc}=3.0V and not 100% tested.
 2. BYTE# pin supported only by TSOP and uTSOP types. BYTE# ≥ V_{cc}-0.2V or BYTE# ≤ 0.2V
 3. Also CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{cc}-0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state.

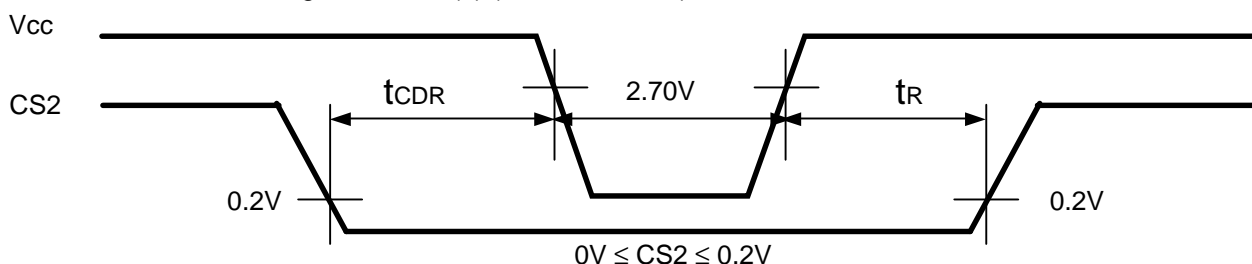
Data Retention timing Waveform (1) (LB#,UB# Controlled)



Data Retention timing Waveform (2) (CS1# Controlled)



Data Retention timing Waveform (3) (CS2 Controlled)



Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
 - (1) artificial life support devices or systems
 - (2) surgical implantations
 - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
 - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510