MOTOROLA

MCM6664

PRELIMINARY DATA SHEET

MOS

(N-CHANNEL)

65.536-BIT DYNAMIC RANDOM ACCESS MEMORY

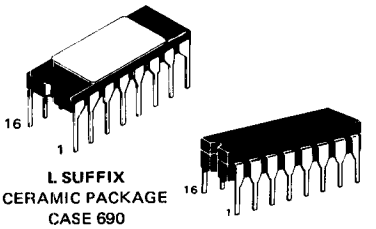
65.536 x 1 BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM6664 is a 65.536-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 65.536 one-bit words and fabricated using Motorola's highly reliable N-channel technology, this device optimizes speed, power and density tradeoffs.

By multiplexing row and column address inputs, the MCM6664 requires only eight address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

The MCM6664 incorporates a one-transistor cell design and dynamic storage techniques, which allows 128 cycle refresh every 2 milliseconds providing compatibility with industry standard 16K RAM.

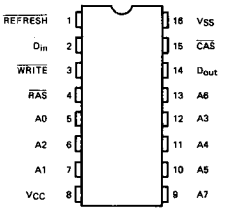
- Single 5 Volt Power Supply
- Automatic Refresh, Self Refresh and RAS-Only Refresh Capability
- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 65.536 x 1 Organization
- All Inputs are Fully TTL Compatible
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation – (<300 mW)
- Fast Access Time Options: 150 ns – MCM6664L-15, C15
  200 ns – MCM6664L-20, C-20
- Easy Upgrade from 16-Pin, 16K RAM



L SUFFIX
CERAMIC PACKAGE
CASE 690

C SUFFIX
FRIT-SEAL PACKAGE
CASE 620

PIN ASSIGNMENT



PIN NAMES

A0 - A7	Address Inputs
CAS	Column Address Strobe
D_{in}	Data In
D_{out}	Data Out
RAS	Row Address Strobe
WRITE	Read/Write input
REFRESH	Refresh Control
V_{CC}	Power (+5 V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE 1:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliabitliy.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This is advance information and specifications are subject to change without notice.

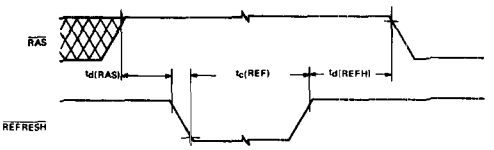
AN IMPROVED REFRESH CONCEPT

To simplify dynamic RAM design, Motorola's MCM6664 uses pin 1 to provide refresh control In addition to the 16K compatible "$\overline{RAS}$-only" refresh mode, two other modes can be used by employing pin 1. "Automatic refresh" is used during normal operation just as "$\overline{RAS}$-only" refresh is used. But Motorola's unique refresh control eliminates the need for supplying $\overline{RAS}$, CAS, row addresses, and address counter, or any critically timed pulse. And during battery backup or power-down, pin 1 places the device in the self-refresh mode with no timing signals required to maintain data in the memory.

SELF REFRESH

Figure 1 shows the simple timing diagram for the MCM6664 in the self-refresh mode. Duting battery backup or other power down period where it is desirable

FIGURE 1 – SELF-REFRESH MODE ($\overline{CAS}$[1], ADDRESS, DATA-IN, AND $\overline{WRITE}$ ARE DON'T CARE)



Parameter	Symbol	Min.	Max.	Unit
Self-refresh cycle time – the entire memory is refreshed every 2 ms	$t_{c(REF)}$	16000	–	ns
Refresh high delay time before a new memory cycle may begin	$t_{d(REFH)}$	250	–	ns
$\overline{RAS}$ high to Refresh low delay ($\overline{RAS}$ precharge time)	$t_{d(RAS)}$	60	–	ns

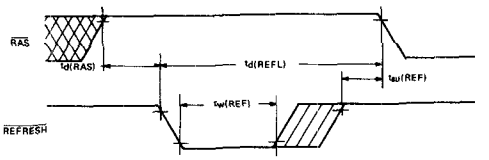
[1] $\overline{CAS}$ controls the output data. If $\overline{CAS}$ remains low the previous output will remain valid. When $\overline{CAS}$ is brought high, the output will assume a high-impedance state.

to maintain the contents of the RAM, $\overline{RAS}$ is brought (or left) HIGH a short time, $t_{d(RAS)}$ before the refresh control is activated (LOW). (This is the regular $\overline{RAS}$ precharge time.) An internal refresh cycle then begins with the MCM6664 providing its own $\overline{RAS}$, row address, and refresh location counter. As long as $\overline{RAS}$ remains HIGH and $\overline{REFRESH}$ remains LOW, the MCM6664 will asynchronously refresh itself. After two milliseconds the internal refresh location counter will have advanced through all the row addresses thus refreshing the entire memory. This activity will continue until a regular memory cycle is desired. Since it is possible that an internal refresh cycle had just started prior to termination of the self-refresh mode ($\overline{REFRESH}$ HIGH), a delay of one cycle time, $t_{d(REFH)}$, is necessary to guarantee valid data in the next cycle ($\overline{RAS}$ going LOW).

AUTOMATIC REFRESH

Automatic refresh, on the MCM6664, is used wherever a "$\overline{RAS}$ only" refresh would be. Motorola's refresh control frees-up the system – sequential row addresses need not be generated. Figure 2 shows that again the refresh

FIGURE 2 – AUTOMATIC REFRESH CYCLE ($\overline{CAS}$[1], ADDRESSES, DATA-IN, AND $\overline{WRITE}$ ARE DON'T CARE)



Parameter	Symbol	Min.	Max.	Unit
Refresh low delay time before beginning of next cycle	$t_{d(REFL)}$	290	–	ns
Refresh low duration time	$t_{w(REF)}$	60	8000	ns
Refresh high setup time before next memory cycle	$t_{su(REF)}$	20	–	ns
$\overline{RAS}$ high to Refresh low delay ($\overline{RAS}$ precharge time)	$t_{d(RAS)}$	60	–	ns

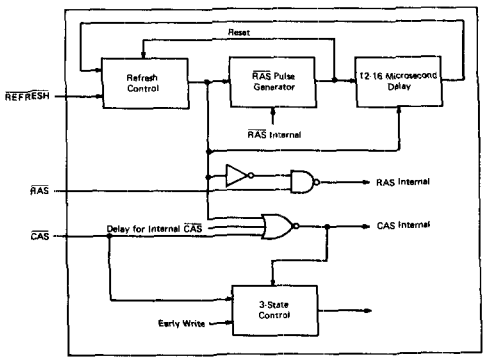
[1] $\overline{CAS}$ controls the output data. If $\overline{CAS}$ remains low the previous output will remain valid. When $\overline{CAS}$ is brought high, the output will assume a high-impedance state.

cycle is begun by bringing $\overline{REFRESH}$ LOW after $\overline{RAS}$ has precharged, $t_{D(RAS)}$. The internal row address counter will present the next set of addresses internally and the internal $\overline{RAS}$ will fire shortly after the cycle begins. $\overline{REFRESH}$ can be inactivated (HIGH) any time after $t_{s(REF)}$. (Obviously it must be activated in at least 8 microseconds or the RAM will enter the self-refresh mode.) One cycle time after the internal RAS has fired, the next memory cycle may begin.

REFRESH FEATURES

To make system implementation of the MCM6664's refresh feature easy, Motorola's design allows $\overline{CAS}$, Data-In, $\overline{Write}$, and the addresses to change without affecting the refresh cycle. One portion of the system memory cas easily be refreshed while regular memory cycles are taking place in another portion. Fail-Safe operation is guaranteed by internal lock-out circuits (figure 3).

FIGURE 3 – SIMPLIFIED TIMING SEQUENCE DIAGRAM



Another feature is Motorola's immediate refresh action after refresh request design, avoiding the one cycle look-ahead problem of other schemes.

Output data can remain valid for use by the CPU while the RAM is being refreshed due to the MCM6664's exclusive $\overline{CAS}$ control. The output is controlled by $\overline{CAS}$ exclusive of any combination of other inputs during refresh (or a regular memory cycle). If $\overline{CAS}$ is left active (LOW) the output data remains valid. As soon as a floating output is desired, $\overline{CAS}$ is brought HIGH (even during the middle of refresh) and the output enters the high-impedance state.

This signal independancy is illustrated in figure 3 and the truth table in figure 4. If $\overline{REFRESH}$ is HIGH and $\overline{RAS}$ goes LOW, internal $\overline{RAS}$ will fire starting the memory cycle. If $\overline{RAS}$ is HIGH and $\overline{REFRESH}$ goes LOW, internal $\overline{RAS}$ will fire starting the refresh cycle. $\overline{REFRESH}$ LOW also inhibits internal CAS from firing preventing the output from trying to go active.

FIGURE 4 – OUTPUT BUFFER TRUTH TABLE

Early Write	CAS	Refresh Control (CAS Internal)		Output Buffer
H	X	X	(X)	H1-Z
X	H	X	(X)	H1-Z
L	L	L	(H)	Maintains Previous Data
L	L	H	(L)	Active

During a refresh cycle the internal $\overline{RAS}$ triggers the $\overline{RAS}$ pulse generator and strobes the internally generated row addresses. A reset signal precharges the Refresh Control and advances the refresh address counter. (For maximum reliability the refresh counter is refreshed after every refresh or regular memory cycle.) If $\overline{REFRESH}$ is held LOW, the Refresh Control will be activated by a signal from the Delay circuitry starting the refresh sequence again. This sequence is repeated asynchronously every 12-16 microseconds thus refreshing the entire memory array within the 2 millisecond specification. Bringing $\overline{REFRESH}$ HIGH aborts the refresh cycle if internal $\overline{RAS}$ has not yet fired. Therefore, a delay of just one cycle time will guarantee that the refresh cycle has ended and that another memory cycle can begin.

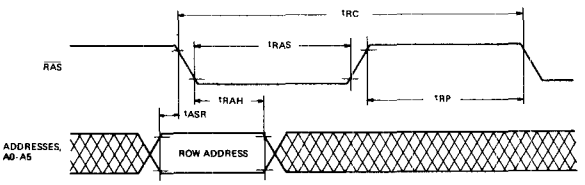
The three-state control will place the output in the high-impedance state during an early write cycle (W low before $\overline{CAS}$ low) to facilitate common I/O operation. But the key to the MCM6664's output flexibility is independent $\overline{CAS}$ control. $\overline{CAS}$ going HIGH brings the output into the high-impedance state regardless of other input conditions or what cycle the memory is in at the time. For instance, if in the middle of a refresh cycle you want to prepare for a read operation and wish to clear the previous output data or you want to prepare for a write operation and are in common I/O system, simply bring $\overline{CAS}$ HIGH and the output floats.

CAS Internal always takes the opposite state of Refresh Control. During a refresh cycle (CAS Internal HIGH) the output maintains the previous data as long as $\overline{CAS}$ is held LOW. When $\overline{CAS}$ is brought HIGH, the data is cleared and the output is returned to a high-impedance state. All inputs LOW indicates a regular memory cycle with the output active level determined by the stored data.

THE REGULAR WAY

"$\overline{RAS}$-only" refresh became the standard for 4K and 16K Dynamic RAMs. Naturally the MCM6664 offers complete compatibility with these industry standards by allowing 128 cycle $\overline{RAS}$-only refresh exactly as it is performed in the 4116. Just as with the 4116, A_0 - A_6 is used during refresh. The new A_7 is not used, thus no modifications to existing refresh circuitry are required for drop-in 64K operation. Again $\overline{CAS}$ may be used as output control – HIGH for high-impedance and reduced power; LOW to maintain previous data at the output.

FIGURE 5 – RAS-ONLY REFRESH CYCLE (DATA-IN AND $\overline{WRITE}$ ARE DON'T CARE, $\overline{CAS}$ IS HIGH)



Parameter	Symbol	Min.	Max.	Unit
Random Read or Write Cycle Time	t_{RC}	250	–	ns
Row Address Strobe Pulse Width	t_{RAS}	150	–	ns
Row Address Strobe Precharge Time	t_{RP}	60	–	ns
Row Address Setup Time	t_{ASR}	0	–	ns
Row Address Hold Time	t_{RAH}	15	–	ns