Preliminary

MB81C71-45, MB81C71-55

65,536-Bit Static Random Access Memory with Separate Data Input, Data Output and Automatic Power Down

Description

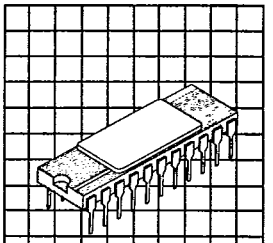
The Fujitsu MB81C71 is a 65,536 word x 1-bit static random access memory fabricated with CMOS technology. It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.

The MB81C71 is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.

All pins are TTL compatible and a single +5 volt power supply is required.

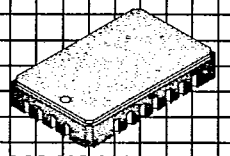
Features

- Organization 65,536 words x 1-bit
- Static operation: no clocks or refresh required
- Fast access time: TAVQV = TELQV = 45 ns max. (MB81C71-45) TAVQV = TELQV = 55 ns max. (MB81C71-55)
- Single +5V supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and outputs
- Three-state output with OR-tie capability
- Chip enable for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- Standard 300 mil. width 22-pin Dual In-Line package
- Standard 22-pad LCC package



Ceramic Package
DIP-22C-A02

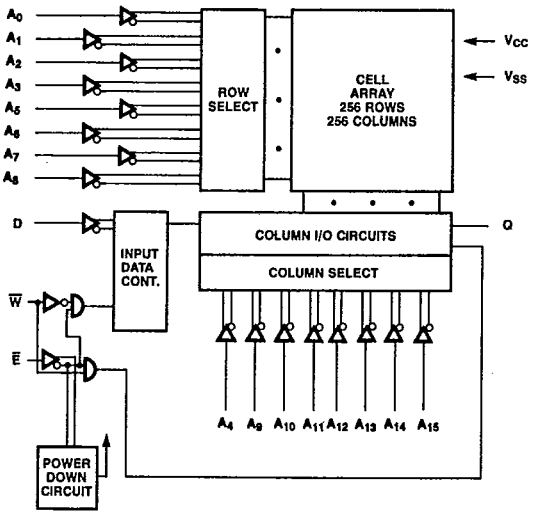
Plastic Package
DIP-22P-M04

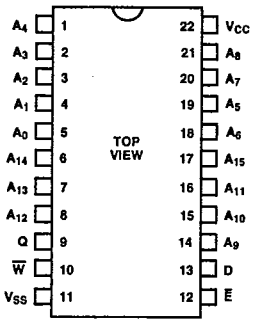


LCC-22C-A01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB81C71 Block Diagram and Pin Assignments





TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	Q	ACTIVE

Absolute Maximum Ratings

(See Note)

Rating	Symbol		Value	Unit
Supply voltage	V_{CC}		−0.5 to +7	V
Input voltage on any pin with reference to V_{SS}	V_{IN}		−3.5* to +7	V
Output voltage on any pin with reference to V_{SS}	V_{OUT}		−0.5 to +7	V
Output current	I_{OUT}		±50	mA
Power dissipation	P_D		1.0	W
Temperature under bias	T_{BIAS}		−10 to +85	°C
Storage temperature	T_{STG}	Ceramic	−65 to +150	°C
		Plastic	−45 to +125	

*DC: min. = −0.5V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.5*		0.8	V
Input high voltage	V_{IH}	2.2		6.0	V
Ambient temperature	T_A	0		70	°C

Note: *−3.0V min. for pulse width less than 20 ns.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}		5	pF
$\overline{E}$ capacitance (V_{IN} = 0V)	$C_{\overline{E}}$		8	pF
Output capacitance (V_{OUT} = 0V)	C_{OUT}		8	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Input leakage current	V_{IN} = 0V to V_{CC} V_{CC} = max.	I_{LI}	−10		10	μA
Output leakage current	$\overline{E}$ = V_{IH}, V_{OUT} = 0V to 4.5 V_{CC} = max.	I_{LO}	−50		50	μA
Operating power supply current	$\overline{E}$ = V_{IL}, V_{CC} = max. I_{OUT} = 0 mA, cycle = min.	I_{CC}			80	mA
Standby current	V_{CC} = min. to max. $\overline{E}$ = V_{CC} −0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} −0.2V	I_{SB1}			15	mA
	V_{CC} = min. to max. $\overline{E}$ = V_{IH}	I_{SB2}			25	
Output low voltage	I_{OL} = 16 mA	V_{OL}			0.45	V
Output high voltage	I_{OH} = −4 mA	V_{OH}	2.4			V
Peak power on current	V_{CC} = 0 to V_{CC} min. $\overline{E}$ = lower of V_{CC} or V_{IH} min.	I_{PO}			30	mA

AC Characteristics

(Recommended operating conditions unless otherwise noted.)

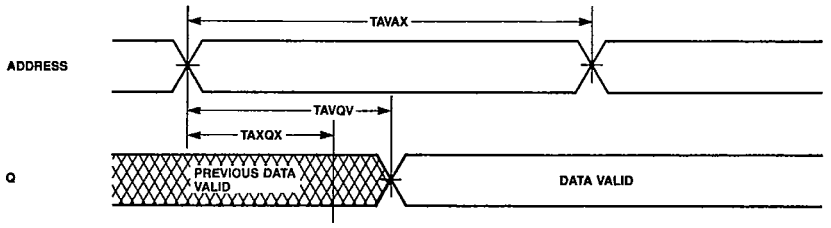
Read Cycle

Parameter	Symbol	MB81C71-45 Min	MB81C71-45 Max	MB81C71-55 Min	MB81C71-55 Max	Unit
Read cycle time*1	TAVAX	45		55		ns
Address access time	TAVQV		45		55	ns
Chip enable access time*2	TELQV		45		55	ns
Output hold from address change	TAXQX	5		5		ns
Chip enable to output in low-Z*3,4	TELQX	5		5		ns
Chip enable to output in high-Z*3,4	TEHQZ	0	25	0	30	ns
Chip enable to power up time	TELIH	0		0		ns
Chip enable to power down	TEHIL		35		40	ns

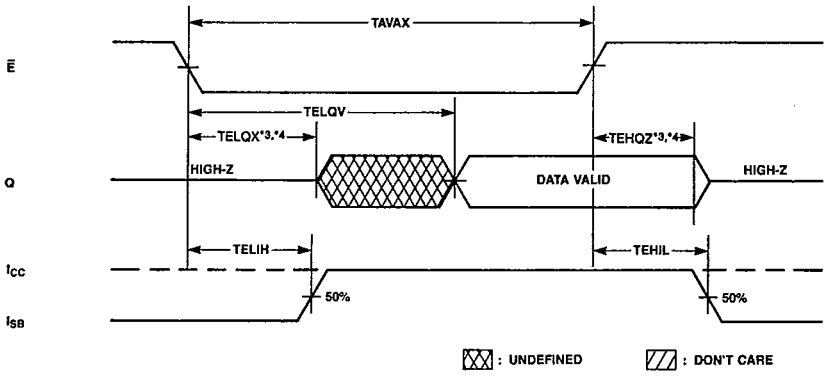
Notes: *1 All read cycles are determined from the last valid address transitioning to the first address transitioning of next cycle.
*2 Chip enable for a finite time is less than TAVAX prior to selection.
*3 Transition is measured at the point of ±500 mV from steady state voltage.
*4 This parameter is measured with the loading specified in Figure 1.

Read Cycle Timing Diagrams

Read Cycle: Address Controlled*1 *2



Read Cycle: $\overline{E}$ Controlled*2



NOTES: *1 $\overline{E}$ IS LOW.
*2 $\overline{W}$ IS HIGH TO READ CYCLES.
*3 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.
*4 THIS PARAMETER IS MEASURED WITH THE LOADING SPECIFIED IN FIGURE 1.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

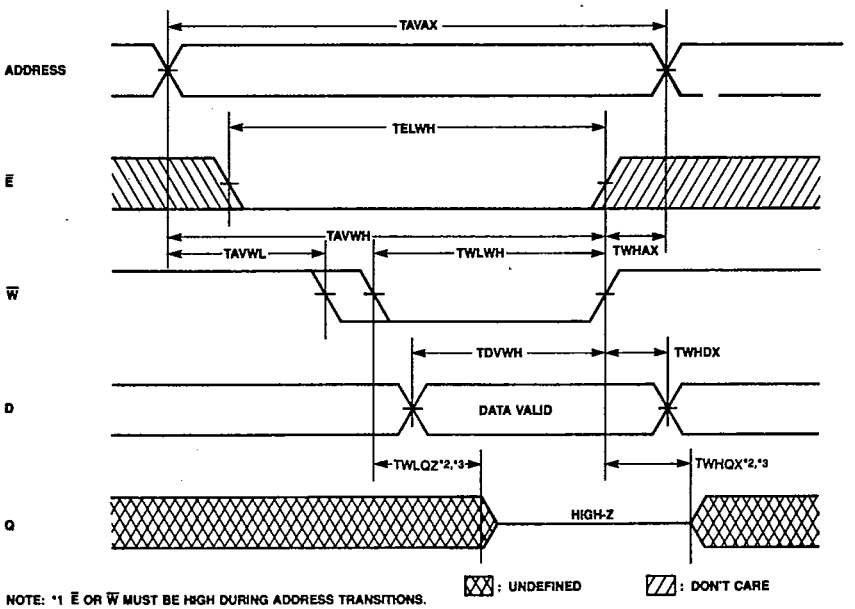
Write Cycle

Parameter	Symbol	MB81C71-45 Min	MB81C71-45 Max	MB81C71-55 Min	MB81C71-55 Max	Unit
Write cycle time	TAVAX	45		55		ns
Chip enable to end of write	TELWH	40		50		ns
Address valid to end of write	TAVWH	40		50		ns
Address setup time	TAVWL	5		5		ns
Address setup time	TAVEL	0		0		ns
Write pulse width	TWLWH	30		35		ns
Data valid to end of write	TDVWH	25		30		ns
Write recovery time	TWHAX	5		5		ns
Data hold time	TWHDX	0		0		ns
Write enable to output in high-Z*1 *2	TWLQZ	0	25	0	30	ns
Output active from end of write*1 *2	TWHQX	0		0		ns

Notes: *1 Transition is measured at the point of ±500 mV from steady state voltage.
*2 This parameter is measured with the loading specified in Figure 1.

Write Cycle Timing Diagrams

Write Cycle: $\overline{W}$ Controlled*1

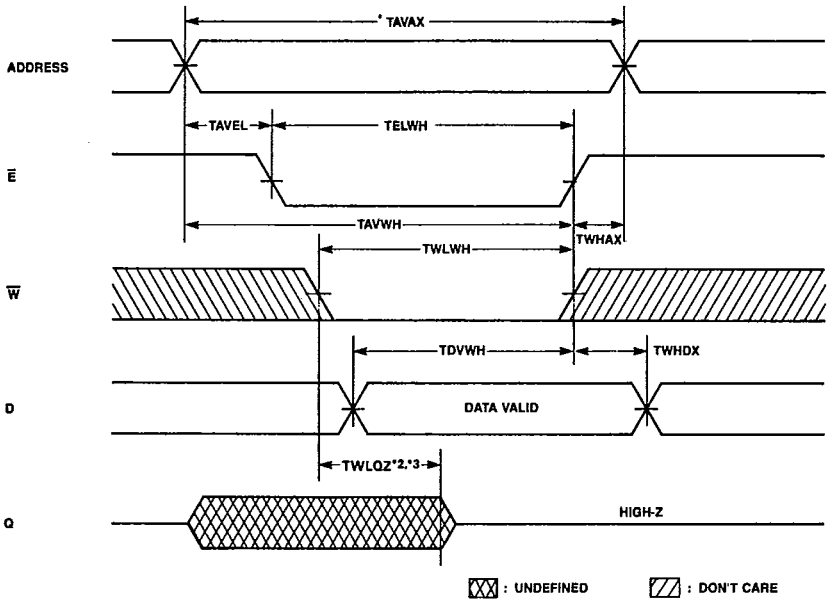


NOTE: *1 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.
*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.
*3 THIS PARAMETER IS MEASURED WITH THE LOADING SPECIFIED IN FIGURE 1.

AC Characteristics
(continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagram*1

Write Cycle: $\overline{E}$ Controlled



NOTES: * ALL WRITE CYCLES ARE DETERMINED FROM LAST VALID ADDRESS TRANSITIONING TO THE FIRST ADDRESS TRANSITIONING OF NEXT CYCLE.
*1 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.
*2 TRANSITION IS MEASURED AT THE POINT OF ±0.5 V FROM STEADY STATE VOLTAGE.
*3 THIS PARAMETER IS MEASURED WITH THE LOADING SPECIFIED IN FIGURE 1.

AC Test Conditions

Input pulse levels:	0.6V to 2.4V
Input pulse rise and fall times:	5 ns
Timing measurement reference levels:	Input: 1.5V
	Output: 1.5V

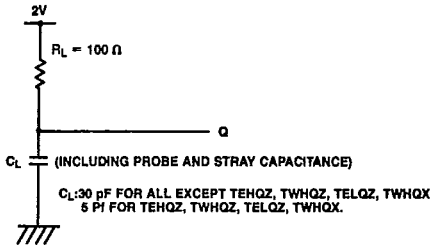
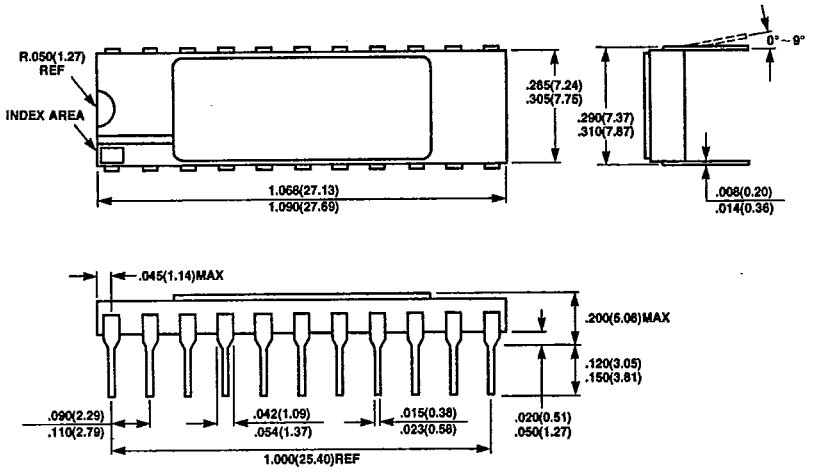


Figure 1. Output Loading

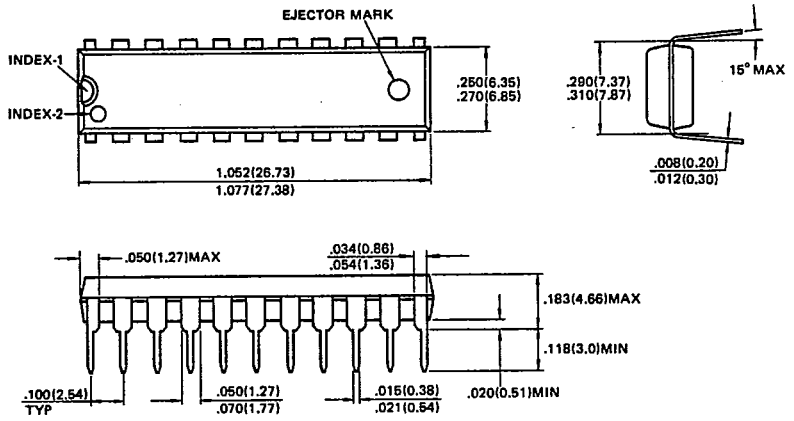
MB81C71-45
MB81C71-55

Package Dimensions
Dimensions in inches
(millimeters)

22-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-22C-A02)



22-Lead Plastic Dual In-Line Package
(Case No.: DIP-22P-M02)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

22-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-22C-A01)