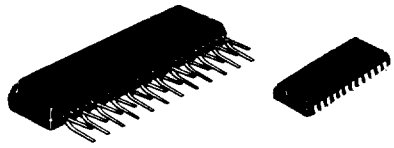
M5M4C264AL,J-8,-10,-12

262144-BIT DUAL-PORT DYNAMIC RAM



DESCRIPTION

The Mitsubishi M5M4C264A is a high speed 262,144-bit Dual Port Dynamic Memory equipped with a 64K x 4 Dynamic RAM Port and a 256 x 4 Serial Read/Write Port. The use of N-well CMOS Process combined with silicide technology and a single transistor dynamic storage cell provide high circuit density and low power dissipation. The Serial Read/Write Port is connected to an internal 1024 bit Data Register through a 256 x 4 Serial Input/Output Control and is serially read out or written in with a clock rate of up to 33 MHz.

All reads and writes are done relative to the RAM Array, thus Data Transfer from the RAM Array to the Data Register is referred to as Read Transfer, while Data Transfer from the Data Register to the RAM Array is referred to as Write Transfer.

FEATURES

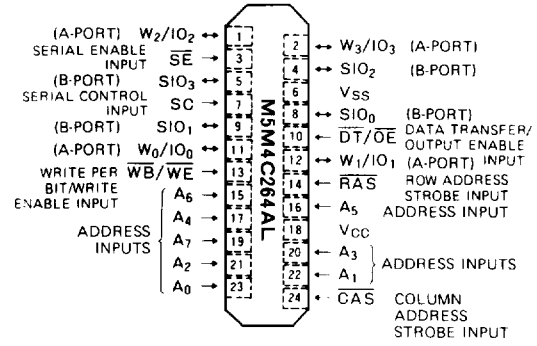
Type name	$\overline{RAS}$ Access Time (ns)	Random Read/Write Cycle Time (ns)	Serial Read/Write Cycle Time (ns)	Random Read/Write V_{CC} Supply Current (mA)	Serial Read/Write V_{CC} Supply Current (mA)
M5M4C264AL, J-8	80	160	30	60	30
M5M4C264AL, J-10	100	190	35	50	25
M5M4C264AL, J-12	120	220	40	40	20

- Dual Port Architecture
  - RAM Port: 64k word x 4-bit
    - Access Time . . . . . 80 ns (max)
  - Serial Read/Write Port: 256 word x 4-bit
    - Cycle Time . . . . . 30 ns (max)
- Bidirectional Data Transfer function between the RAM Array and the Data Resister
- Fully Asynchronous Dual Port Accessability (except during the Data Transfer Period)
- Addressable Start of Serial Read/Write (Pointer Control Function)
- Write per Bit Function
- Real Time Data Transfer from the RAM Array to the Data Register
- Fast Page Mode, Hidden Refresh and $\overline{CAS}$ before $\overline{RAS}$ Refresh
- 256 cycles/4 ms Refresh
- Fully TTL Compatible
- Outline 24 Pin ZIP, 24 Pin 300 mil SOJ
- N-well CMOS Process & Low Power Dissipation
  - RAM & SAM Active
    - (-8/-10/-12) . . . . . 90/75/60 mA max
  - RAM & SAM Standby
    - (-8/-10/-12) . . . . . 5/5/5 mA max

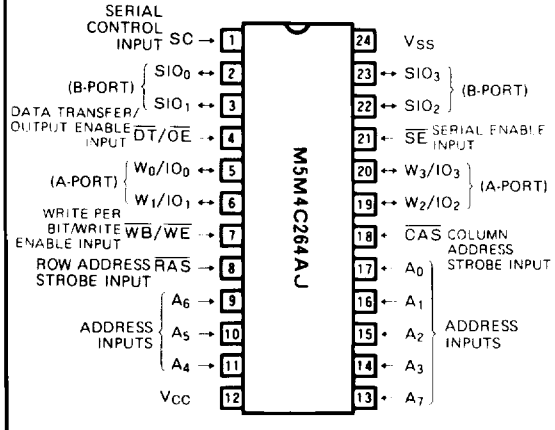
APPLICATION

Display equipment for personal computer/work station, Frame memory for digital TV/VCR, Videotex, Teletext, Video printer, High Speed data transmission systems

PIN CONFIGURATION (TOP VIEW)

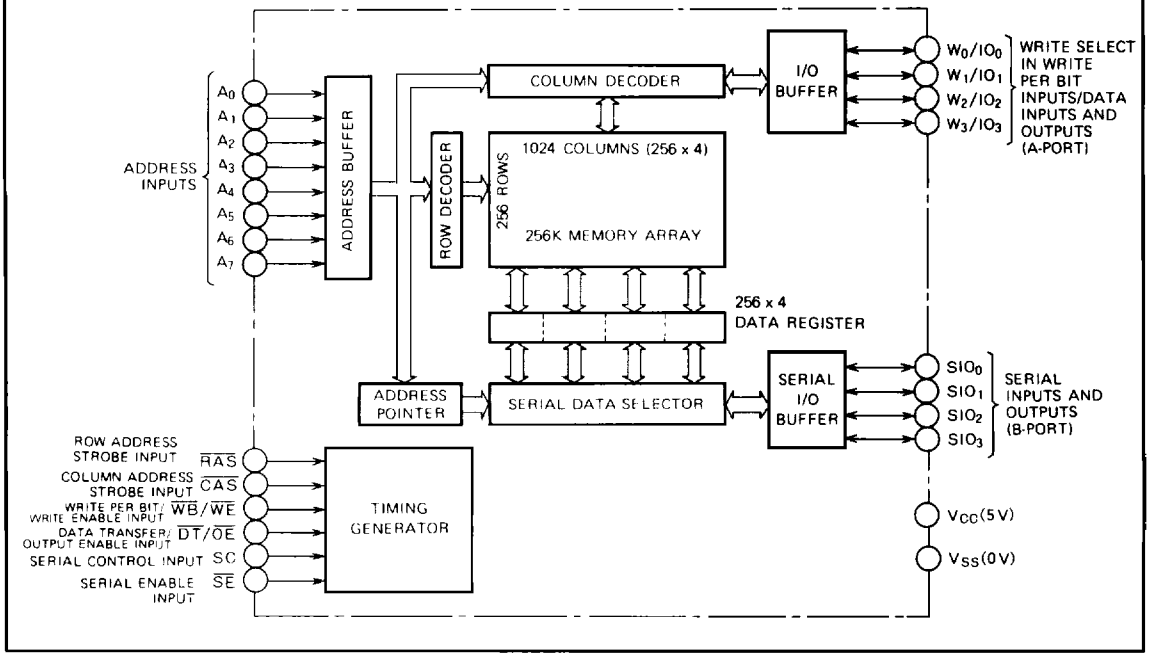


Outline 24P5L



Outline 24P0J

BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
$\overline{RAS}$	ROW ADDRESS STROBE INPUT	It is used as a clock which latches the row address ($A_0 \sim A_7$) and selects the word line. It also selects the write-per-bit, the data transfer and the $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.
$\overline{CAS}$	COLUMN ADDRESS STROBE INPUT	It is used as a clock which latches the column address ($A_8 \sim A_{15}$) and reads or writes the selected words. In the data transfer cycle, it becomes the SAM start address.
$A_0 \sim A_7$	ADDRESS INPUT	The M5M4C264A is an address multiplex method for inputting the row addresses and column addresses separately, in order to select one word from the 64K word memory cells. The various addresses are latched by the $\overline{RAS}$/$\overline{CAS}$ falling edge. In the data transfer cycle, this address input is also combined with the serial access start address.
$\overline{WB}/\overline{WE}$	WRITE-PER-BIT/ WRITE ENABLE INPUT	When the $\overline{WB}/\overline{WE}$ level in the $\overline{RAS}$ clock falling edge is "L", the write-per-bit or write transfer cycle is selected, and when it is "H", a 4 bit write to the RAM or a read transfer cycle from the RAM is selected.
$\overline{DT}/\overline{OE}$	DATA TRANSFER/ OUTPUT ENABLE INPUT	In the RAM read cycle, it makes the data output into enable. Also, when the $\overline{DT}/\overline{OE}$ level in the $\overline{RAS}$ clock falling edge is "L", the data transfer cycle is selected, and when it is "H", the read/write cycle is selected.
$W_0 \sim W_3$/ $IO_0 \sim IO_3$	WRITE-PER-BIT SELECTION INPUT/ DATA INPUT/OUTPUT	These are the data input/output pins to the RAM. During the write-per-bit cycle in the $\overline{RAS}$ clock falling edge, the "H" pin is enable and the selected bit-only-write is performed. Also, in the write cycle, the data in the late falling edge, whether it is $\overline{CAS}$ or $\overline{WE}$, is latched.
SC	SERIAL CONTROL INPUT	The serial access is started from the SC clock rising edge. In the serial read cycle the output data is held until the next clock rise. Also in the serial write cycle, the data is latched at the SC clock rising edge.
$SIO_0 \sim SIO_3$	SERIAL INPUT/ OUTPUT	256 x 4 words serial data input/output pins.
$\overline{SE}$	SERIAL ENABLE INPUT	This makes serial input/output into enable. In the $\overline{RAS}$ clock falling edge, when $\overline{SE}$ is "H", it is a pseudo transfer, and when it is "L", it is a write transfer.

NB. SAM: Serial Access Memory

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FUNCTION

RAM Port Operation

The row/column addresses are specified by the $\overline{RAS}$/$\overline{CAS}$ clocks.

The RAM read/write cycle is set up by maintaining the $\overline{DT}$/$\overline{OE}$ at "H" level, while the $\overline{RAS}$ clock is falling. In addition, the column address is specified while the $\overline{RAS}$ clock is held at "L" level and goes into fast page mode when the $\overline{CAS}$ clock is activated, and then the column data in one row can be read/written continually.

1. Random Read Cycle

Data is read out when $\overline{DT}$/$\overline{OE}$ is a "L" level.

2. Random Write Cycle

Data is written in when $\overline{WB}$/$\overline{WE}$ is a "L" level.

When the $\overline{WE}$ clock is input before the $\overline{CAS}$ clock, it becomes an early write cycle, and the data from the $\overline{CAS}$ clock falling, is written in the RAM.

When the $\overline{WE}$ clock is input after the $\overline{CAS}$ clock, it becomes a Delayed write cycle and the data from the $\overline{WE}$ clock falling is written in the RAM.

The read-modify-write cycle modifies the data which has been read and writes it in again. This time also, the $\overline{OE}$, $\overline{WE}$ clock controls the reading/writing of data.

In this random write cycle, the write-per-bit function (Note 1) is available.

SAM Port Operation

At the falling edge of the $\overline{RAS}$ clock, the data transfer cycle is set up by maintaining the $\overline{DT}$/$\overline{OE}$ at "L" level. At such a time, the transfer cycle is the read transfer when the $\overline{WB}$/$\overline{WE}$ clock is "H" level, and the write transfer when it is "L" level.

In the transfer cycle, the row address sets up the RAM row and the column address becomes the serial access start address.

- $\overline{DT}$/$\overline{OE}$ signal can be used to select RAM or SAM independent mode ($\overline{DT}$ = "H") and between RAM and SAM data transfer mode ($\overline{DT}$ = "L").
- Within one transfer cycle, transfer of data (256 x 4 bits) is possible between any rows in the RAM and SAM.
- $\overline{WE}$ signal permits the designation of transfer direction. ($\overline{WE}$ = "H": RAM → SAM (read transfer)/$\overline{WE}$ = "L": SAM → RAM (write transfer)]
- During read transfer, high-speed transfer execution is started at $\overline{DT}$/$\overline{OE}$ leading edge. (Note 2)
- Transfer cycle allows the selection of SAM I/O mode. In write transfer mode, $\overline{SE}$ control allows the transfer execution to be inhibited. (pseudo write transfer) (Note 3)
- Row address in transfer cycle permits the transfer page of RAM.
- Column address in transfer cycle specifies the read (write) start address of SAM after transfer.

Memory Refresh Operation

The M5M4C264A consists of dynamic RAMs memory cells so a refresh operation is required every 4 m seconds.

The refresh operation consists of reading the data from the memory, amplifying it in the sense amp and then rewriting it. With the M5M4C264A, all the memory cells are refreshed by performing a refresh operation on all 256 row addresses which are designated by the 8 bits.

1. $\overline{RAS}$ Only Refresh

When the row address is input while the $\overline{CAS}$ clock is held at "H" level, and the $\overline{RAS}$ clock is activated, all the column data in the designated row address are refreshed simultaneously.

2. $\overline{CAS}$-Before-$\overline{RAS}$ Refresh

When the $\overline{CAS}$ clock is activated before the $\overline{RAS}$ clock, the designated row address, which is generated by the internal 8 bit refresh counter, is refreshed. The built-in refresh counter is increased with every refresh cycle. Then all the memory cells are refreshed by repeating the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle 256 times.

3. Hidden Refresh

The memory cells are refreshed by the 8 bit refresh counter built into the chip, in the same way as the $\overline{CAS}$-before-$\overline{RAS}$ refresh, by activating the $\overline{RAS}$ clock while the $\overline{CAS}$, $\overline{OE}$ clocks are being held at "L" level after the previous read cycle. At this time, the data which was read into the previous cycle is held in output.

SAM READ OUT/WRITE IN

In the same way as a shift register, SAM inputs and outputs data simultaneously with the SC clock rise. $\overline{SE}$ is used to control the data inputs/outputs.

RAM and SAM are connected to each other by 1024 data buses, and the data from RAM can be transferred to SAM and the data from SAM can be transferred to RAM.

1. SERIAL READ TRANSFER CYCLE (RAM → SAM TRANSFER)

When the $\overline{RAS}$ clock is falling, the serial read transfer mode is selected and at the same time the row address indicates the row for transfer from RAM to SAM and the data are read out. When the column address is input and the $\overline{DT}$ signal is "H", the one row data read out from RAM is transferred to the data register. At the same time as this, the decoded column address is set to the serial selector and the serial read start address is determined. (pointer control) After this, every time the SC clock goes from "L" to "H", the data is output to the serial port and the selector moves on to the next bit. For the serial selector to be cyclic, when the SC clock is input more than 257 times, the same data from the start address mentioned above is output again. $\overline{SE}$ clock controls the serial output buffer. When $\overline{SE}$ is "L" the data register contents are output to the SIO pins and when $\overline{SE}$ is "H", the SIO pins are at high impedance. The serial selector has no relation with the $\overline{SE}$ level and shifts one bit every time the SC clock is input. Serial read transfer can be done when SAM is in operation and also, data from different rows can be continuously output. (real time transfer)

A horizontal scroll can easily be realized with the pointer control function which is utilized to indicate the arbitrary address.

The memory can be effectively used with the real time transfer function which is utilized to scan multiple lines horizontally.

2. SERIAL WRITE TRANSFER CYCLE (SAM → RAM TRANSFER)

When the $\overline{RAS}$ clock is falling, the serial write transfer mode is selected and at the same time the row transferred from SAM is designated by the row address, in the same way as for the serial read transfer mode. When the column address is input and the $\overline{DT}$ signal is turned "H", the single row data which are read out from SAM is written into the row selected by RAM. At the same time as this, the decoded row address is set to the serial selector and the next serial write start address is determined. After this, every time the SC clock is input, the data which are input to SIO are written into SAM. $\overline{SE}$ controls the serial input buffer. It writes into the data register when the level is "L", and when the level is "H", it only shifts the serial selector without writing in the data.

3. PSEUDO WRITE TRANSFER CYCLE

This is the same as the write transfer cycle, except for the fact that data is not transferred from SAM to RAM. (The row address which is input is ignored.)

When the mode changes from serial read to serial write, this cycle is used so that the RAM data is not destroyed, and also for changing the mode of the serial port.

Different to serial read transfer, serial write transfer and pseudo write transfer cycles cannot be done while SAM is operating, and it cannot input data continuously to different rows.

Note 1: Write-Per-Bit Function

During the RAM operation, data is written to the specified terminals of the four I/O common terminals, while being inhibited at the others.

Write-Per-Bit mode is specified by $\overline{WB}$ (= "L") at $\overline{RAS}$ falling edge.

Write terminals are specified by W/IO (Write = "H", Write inhibit = "L") at this time. Actual writing is then carried out by $\overline{WE}$ in the same manner as with the conventional DRAM.

Note 2: Real – Time Data Transfer

Read transfer (RAM → SAM) is executed with $\overline{DT}$ leading timing in transfer cycle. In the SC clock input before this timing, the SAM contents before transfer are output, while the new SAM contents after read transfer are output in the SC clock input after this timing.

During read transfer, continuous SC clock is also applied, thus making it possible to continuously produce SAM output before read transfer and SAM output after transfer.

Note 3: Pseudo Write Transfer

In order to write data to SAM when it has been in the output mode it is necessary to change the SAM I/O common terminals (SIO) to the input mode using the write transfer mode. If write transfer is not desired, the pseudo write transfer mode should be used.

If $\overline{SE}$ is in "H" at $\overline{RAS}$ falling edge of write transfer mode is selected; thus, SAM I/O common terminals are set to the input mode, but SAM to RAM data transfer is not executed.

MODE SELECTION

Input pin state at $\overline{RAS}$ falling				RAM		SAM
$\overline{DT}/\overline{OE}$	$\overline{WB}/WB$	$\overline{SE}$	W/IO 0 ~ 3		Bit Mask	SIO_{0-3}
H	X	X	X	READ	—	—
	H			WRITE	—	—
	L	X	H	Write-Per-Bit	Non Masked	—
			L		Masked	
L	H	X	X	RAM→SAM (read transfer)	—	Output mode
	L	L	X	SAM→RAM (write transfer)	—	Input mode
		H	X	Pseudo Write Transfer (No RAM contents will be changed)	—	Input mode

X: Not specified.

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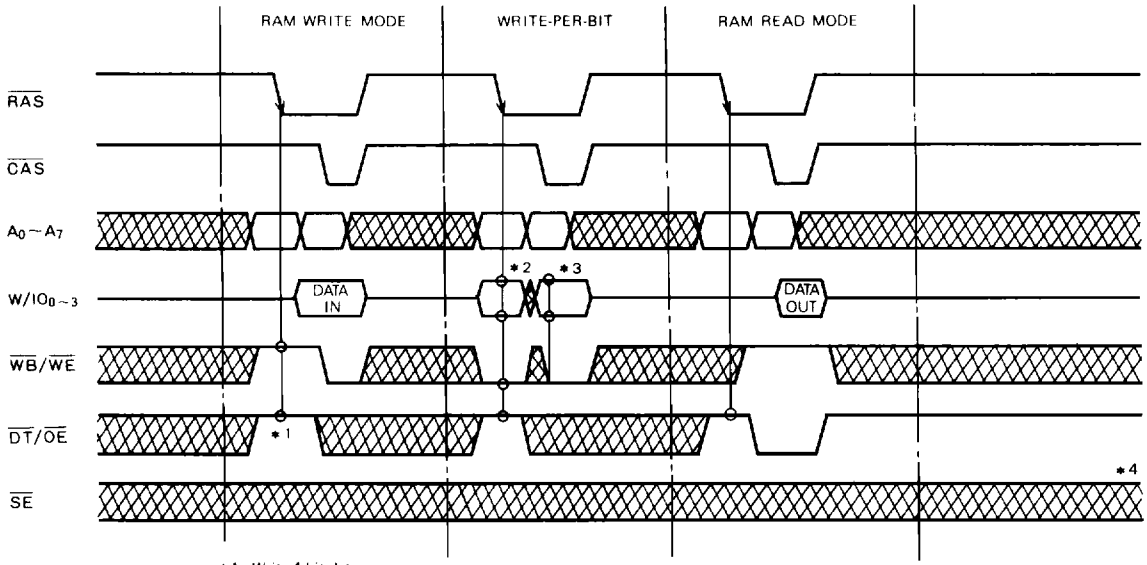
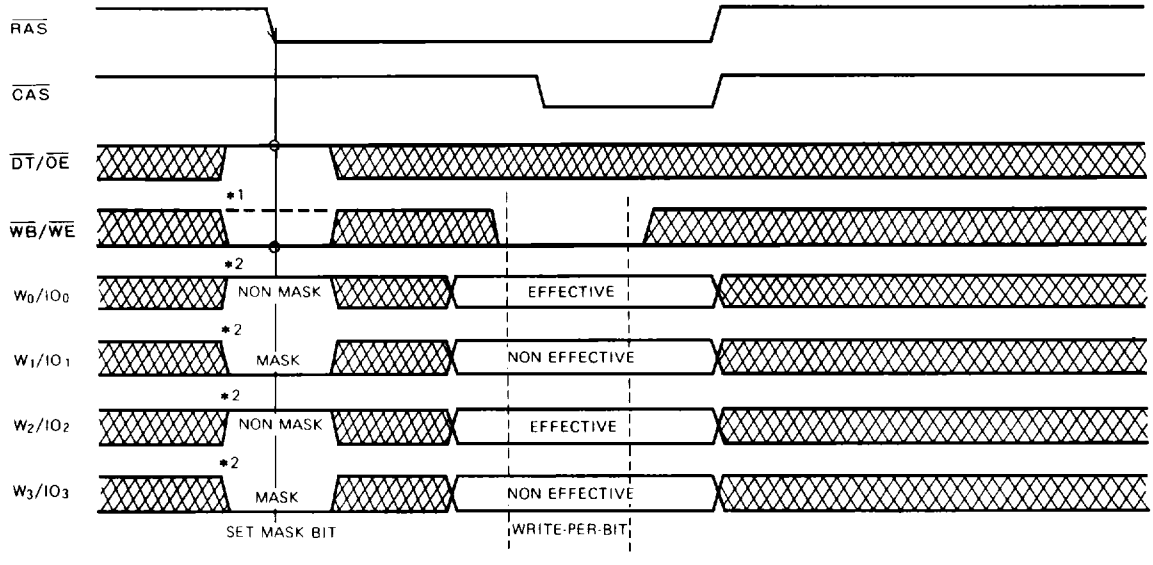
RAM Access Mode



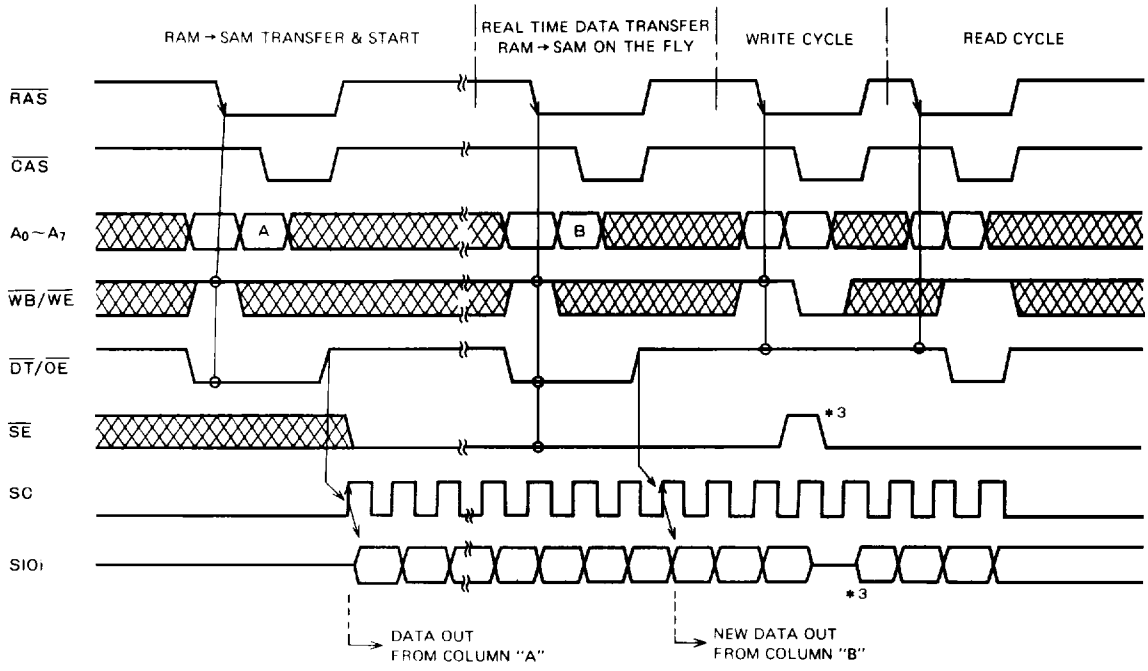
*1: Write 4 bit data
*2: Set mask bit
*3: Write selected bit
*4: Indicates the don't care input

Write-Per-Bit Operation



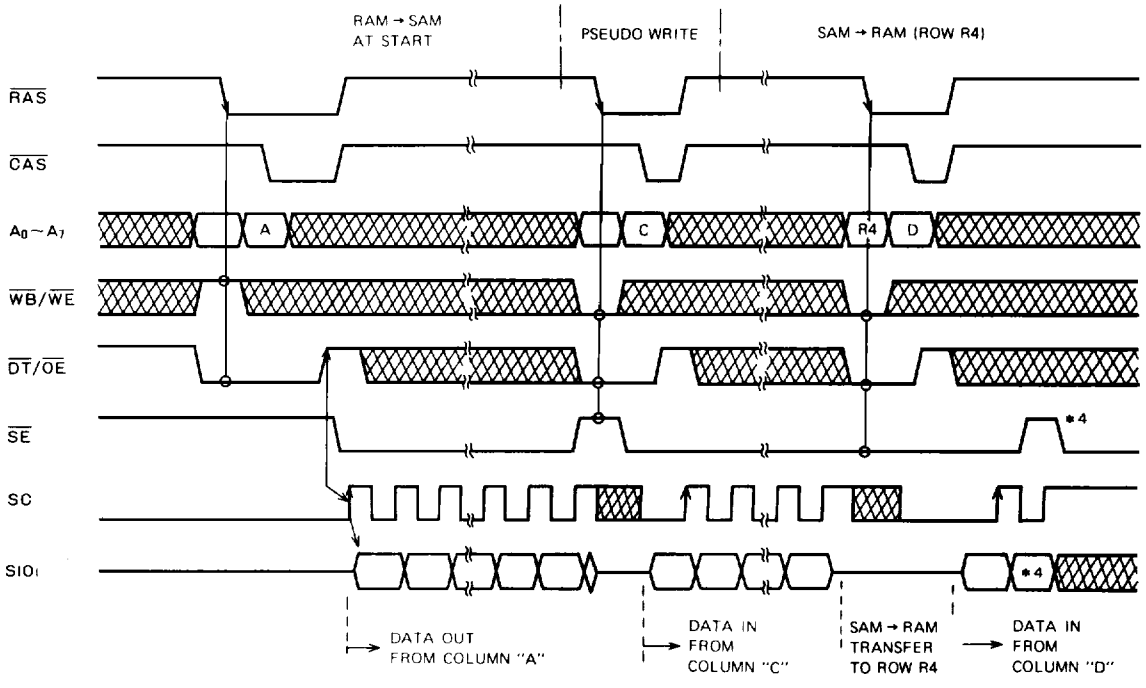
*1. At WB/WE = "H", the 4 bit data are written into RAM
*2. W0 ~ 3/IO0 ~ 3 = "H": Non masked
W0 ~ 3/IO0 ~ 3 = "L": Masked

Serial Output Mode



*3 If $\overline{SE}$ goes "H" level, SIOi become into high impedance state, but serial data selector is continuously working.

Serial Input Mode



*4 If $\overline{SE}$ goes "H" level, SIOi input data is ignored, but serial data selector is continuously working.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta＝25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Norm	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input	2.4		6.5	V
V_{IL}	Low-level input	−1.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{OH(R)}$	High level output (RAM port)	$I_{OH(R)}$＝−2mA	2.4		V_{CC}	V
$V_{OL(R)}$	Low level output (RAM port)	$I_{OL(R)}$＝4.2mA	0		0.4	V
$V_{OH(S)}$	High level output (Serial I_O port)	$I_{OH(S)}$＝−2mA	2.4		V_{CC}	V
$V_{OL(S)}$	Low level output (Serial I_O port)	$I_{OL(S)}$＝4.2mA	0		0.4	V
I_{OZ}	Off-state output current	Q Floating 0＜Vout＜V_{CC}	−10		10	μA
I_I	Input current	0＜Vin＜V_{CC}	−10		10	μA

CAPACITANCE (Ta＝25°C, f＝1MHz, V_I＝25Vmrs)

Symbol	Pin name	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN0}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, SC, $\overline{SE}$, $\overline{DT}/\overline{OE}$	V_I＝V_{SS}, f＝1MHz, V_I＝25mVrms			8	pF
C_{IN1}	A_0～A_7				8	pF
C_O	WIO_0～WIO_3, SIO_0～SIO_3				10	pF

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Note 3)

Symbol	Parameter		Limits			Unit
			M5M4C264-8	M5M4C264-10	M5M4C264-12	
	RAM port	SAM port	Max	Max	Max	
I_{CC1}	Random R/W cycle $\overline{RAS}/\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ (min)	Standby ($SC = V_{IL}$)	60	50	40	mA
I_{CC2}	Standby $\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IH}$, D_{OUT} = Hi-Z	($SC = V_{IL}$)	5	5	5	mA
I_{CC3}	$\overline{RAS}$ only refresh cycle $\overline{RAS}$ = cycling, $\overline{CAS} = V_{IH}$, t_{RC} = min	($SC = V_{IL}$)	60	50	40	mA
I_{CC4}	Page mode cycle $\overline{RAS} = V_{IL}$, $\overline{CAS}$ = cycling, t_{PC} = min	($SC = V_{IL}$)	50	40	30	mA
I_{CC5}	$\overline{CAS}$ before $\overline{RAS}$ refresh $t_{RC} = t_{RC}$ (min)	($SC = V_{IL}$)	60	50	40	mA
I_{CC6}	Data transfer cycle $t_{RC} = t_{RC}$ (min)	($SC = V_{IL}$)	65	55	45	mA
I_{CC7}	Random R/W cycle $\overline{RAS}/\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ (min)	Active (t_{SCC} = min)	90	75	60	mA
I_{CC8}	Standby $\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IH}$, D_{OUT} = Hi-Z	(t_{SCC} = min)	30	25	20	mA
I_{CC9}	$\overline{RAS}$ only refresh cycle $\overline{RAS}$ = cycling, $\overline{CAS} = V_{IH}$, t_{RC} = min	(t_{SCC} = min)	90	75	60	mA
I_{CC10}	Page mode cycle $\overline{RAS} = V_{IL}$, $\overline{CAS}$ = cycling, t_{RC} = min	(t_{SCC} = min)	80	65	50	mA
I_{CC11}	$\overline{CAS}$ before $\overline{RAS}$ refresh $t_{RC} = t_{RC}$ min	(t_{SCC} = min)	90	75	60	mA
I_{CC12}	Data transfer cycle $t_{RC} = t_{RC}$ (min)	(t_{SCC} = min)	95	80	65	mA

Note 3: I_{CC} is obtained with the output open.
4: If $V_{IH} \geqq V_{CC} \times 0.9$ and $V_{IL} \leqq 0.6V$.
Then $I_{CC2} \leqq 2.0$ mA. ($\overline{SE}$ and $SIO_0 \sim SIO_7$ must be stable in high or low level.)

SWITCH CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter		Limits						Unit
			M5M4C264-8		M5M4C264-10		M5M4C264-12		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		20		25		30	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		80		100		120	ns
t_{CAA}	Column address access time	(Note 6, 9)		40		50		60	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		45		55		65	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		20		25		30	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	20	0	25	0	30	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 11)	0	20	0	25	0	30	ns
t_{SCA}	Access time from SC high	(Note 6-S)		25		30		35	ns
t_{SEA}	Access time from $\overline{SE}$ low	(Note 6-S)		25		30		35	ns
t_{SEZ}	Output disable time after $\overline{SE}$ high	(Note 11)	0	20	0	25	0	30	ns
t_{SOH}	Serial output hold time after SC high		5		5		5		ns
t_{SOO}	Delay time $\overline{SE}$ low to serial setup	(Note 6-S)	0		0		0		ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles and 8 SC cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prelonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
6-S: Measured with a load circuit equivalent to 2TTL loads and 50pF.
7: Assume that $t_{RCD(max)} \leqq t_{RCD}$ and $t_{RAD(max)} \geqq t_{RAD}$.
8: Assume that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$.
9: Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.
10: Assume that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.
11: $t_{OFF(max)}$, $t_{SOZ(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the high impedance state ($|I_{out}| \leqq 10\mu A$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

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Read, Write, Refresh, Read/Write Transfer and Fast Page Cycles

Symbol	Parameter		Limits						Unit
			M5M4C264-8		M5M4C264-10		M5M4C264-12		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			4		4		4	ms
t_{RP}	$\overline{RAS}$ high pulse width		70		80		90		ns
t_{RCD}	Delay time $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	25	60	25	75	25	90	ns
t_{CRP}	Delay time $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 15)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 16)	35		35		35		ns
t_{RAD}	Column address delay time from $\overline{RAS}$	(Note 17)	20	40	20	50	20	60	ns
t_{ASR}	Row address setup time before $\overline{RAS}$		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$	(Note 18)	0	15	0	20	0	25	ns
t_{RAH}	Row address hold time after $\overline{RAS}$		15		15		15		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		20		20		20		ns
t_T	Transition time	(Note 19)	3	35	3	35	3	35	ns
t_{WBS}	$\overline{WB}/\overline{WE}$ setup time before $\overline{RAS}$		0		0		0		ns
t_{WBH}	$\overline{WB}/\overline{WE}$ hold time after $\overline{RAS}$		15		15		15		ns
t_{DHS}	$\overline{DT}/\overline{OE}$ setup time before $\overline{RAS}$		0		0		0		ns
t_{DHH}	$\overline{DT}/\overline{OE}$ high hold time after $\overline{RAS}$		15		15		15		ns
t_{WS}	Write mask setup time before $\overline{RAS}$		0		0		0		ns
t_{WH}	Write mask hold time after $\overline{RAS}$		15		15		15		ns

Note 12: The timing requirements are assumed t_T = 5ns.
13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
14: $t_{RCD(max)}$ is specified as a reference point only.
If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}.
If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAA} and t_{CAA} as shown in notes 7, 9.
15: t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
16: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)}$ except for t_{CP} of fast page mode cycle.
17: $t_{RAD(max)}$ is specified as a reference point only.
If $t_{RAD} \geqq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle.
18: $t_{ASC(max)}$ is specified as a reference point only of address access time.
19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M4C264-8		M5M4C264-10		M5M4C264-12		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		160		190		220		ns
t_{RAS}	$\overline{RAS}$ low pulse width		80	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	25	10000	30	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$		80		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$		20		25		30		ns
t_{RCS}	Read setup time before $\overline{CAS}$		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time		40		50		60		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time		0		0		0		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low		20		25		30		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		80		100		120		ns
t_{DOEL}	Delay time data to $\overline{OE}$ low		0		0		0		ns
t_{OEHD}	Delay time $\overline{OE}$ high to data		15		20		25		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low		20		25		30		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low		20		25		30		ns

Note 20. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M4C264-8		M5M4C264-10		M5M4C264-12		
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		160		190		220		ns
t_{RAS}	$\overline{RAS}$ low pulse width		80	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	25	10000	30	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$		80		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$		20		25		30		ns
t_{WCS}	Write setup time before $\overline{CAS}$	(Note 22)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$		15		20		25		ns
t_{CWL}	$\overline{CAS}$ hold time after write		20		25		30		ns
t_{RWL}	$\overline{RAS}$ hold time after write		20		25		30		ns
t_{WP}	Write pulse width		15		20		25		ns
t_{DSC}	Data setup time before $\overline{CAS}$		0		0		0		ns
t_{DSW}	Data setup time before write		0		0		0		ns
t_{DHC}	Data hold time after $\overline{CAS}$		25		25		25		ns
t_{DHW}	Data hold time after write		25		25		25		ns
t_{OEHD}	Delay time $\overline{OE}$ high to data		15		20		25		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write		15		20		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M4C264-8		M5M4C264-10		M5M4C264-12		
			Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 21)	205		245		285		ns
t_{RAS}	$\overline{RAS}$ low pulse width		125	10000	155	10000	185	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		65	10000	80	10000	95	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$		125		155		185		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$		65		80		95		ns
t_{RCS}	Read setup time before $\overline{CAS}$		0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ to write	(Note 22)	40		50		60		ns
t_{RWD}	Delay time, $\overline{RAS}$ to write	(Note 22)	100		125		150		ns
t_{CWL}	$\overline{CAS}$ hold time after write		20		25		30		ns
t_{RWL}	$\overline{RAS}$ hold time after write		20		25		30		ns
t_{WP}	Write pulse width		15		20		25		ns
t_{DSW}	Data setup time before write		0		0		0		ns
t_{DHW}	Data hold time after write		15		20		25		ns
t_{AWD}	Delay time address to write	(Note 22)	60		75		90		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$		20		25		30		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$		80		100		120		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to data		15		20		25		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low		15		20		25		ns

Note 21 t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{OEHD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$.

22 t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are specified as reference points only.
If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the WIO pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, the cycle is a read-modify-write cycle and the WIO will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the WIO (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter		Limits						Unit
			M5M4C264-8		M5M4C264-10		M5M4C264-12		
			Min	Max	Min	Max	Min	Max	
t_{PC}	Read, write cycle time		50		60		70		ns
t_{RWPC}	Read, write/read modify write cycle time		100		115		135		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle		135	50000	160	50000	190	50000	ns
t_{CAS}	$\overline{CAS}$ low pulse width for read cycle		20	10000	25	10000	30	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 23)	10	20	10	25	15	30	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$		20		25		30		ns

Note 23. $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leqq t_{CP}$, access time is assumed by t_{CAC}.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 24)

Symbol	Parameter	Limits						Unit
		M5M4C264-8		M5M4C264-10		M5M4C264-12		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	15		20		25		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 24. Eight of more $\overline{CAS}$ before $\overline{RAS}$ cycle is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Normal Read/Write/Pseudo Write Transfer

Symbol	Parameter	Limits						Unit
		M5M4C264-8		M5M4C264-10		M5M4C264-12		
		Min	Max	Min	Max	Min	Max	
t_{WTS}	$\overline{WB}/\overline{WF}$ high setup time before $\overline{RAS}$	0		0		0		ns
t_{WTH}	$\overline{WB}/\overline{WE}$ high hold time after $\overline{RAS}$	15		15		15		ns
t_{DLS}	$\overline{DT}/\overline{OE}$ setup time before $\overline{RAS}$	0		0		0		ns
t_{RDH}	$\overline{DT}/\overline{OE}$ low hold time after $\overline{RAS}$	15		15		15		ns
t_{RSD}	Delay time $\overline{RAS}$ to SC	90		105		120		ns
t_{ASD}	Delay time address to SC	55		60		65		ns
t_{CSD}	Delay time $\overline{CAS}$ to SC	50		55		60		ns
t_{SDH}	SC hold time after $\overline{DT}$	10		10		10		ns
t_{DTSR}	$\overline{DT}$ high setup time before $\overline{RAS}$ high	0		0		0		ns
t_{DTW}	$\overline{DT}$ high pulse width	20		25		30		ns
t_{ES}	$\overline{SE}$ setup time before $\overline{RAS}$ low	0		0		0		ns
t_{EH}	$\overline{SE}$ hold time after $\overline{RAS}$ low	15		15		15		ns
t_{SZR}	$\overline{RAS}$ low to serial input delay time (Serial-in → Serial-out)	20		20		20		ns
t_{SRS}	SC setup time before $\overline{RAS}$ low	20		20		20		ns
t_{SDZ}	Serial output turn-off delay from $\overline{RAS}$ (Serial-out → Serial-in)	10	50	10	50	10	60	ns
t_{SDP}	$\overline{RAS}$ to Serial input delay time (Serial-out → Serial-in)	50		50		60		ns

Serial Input/Serial Output

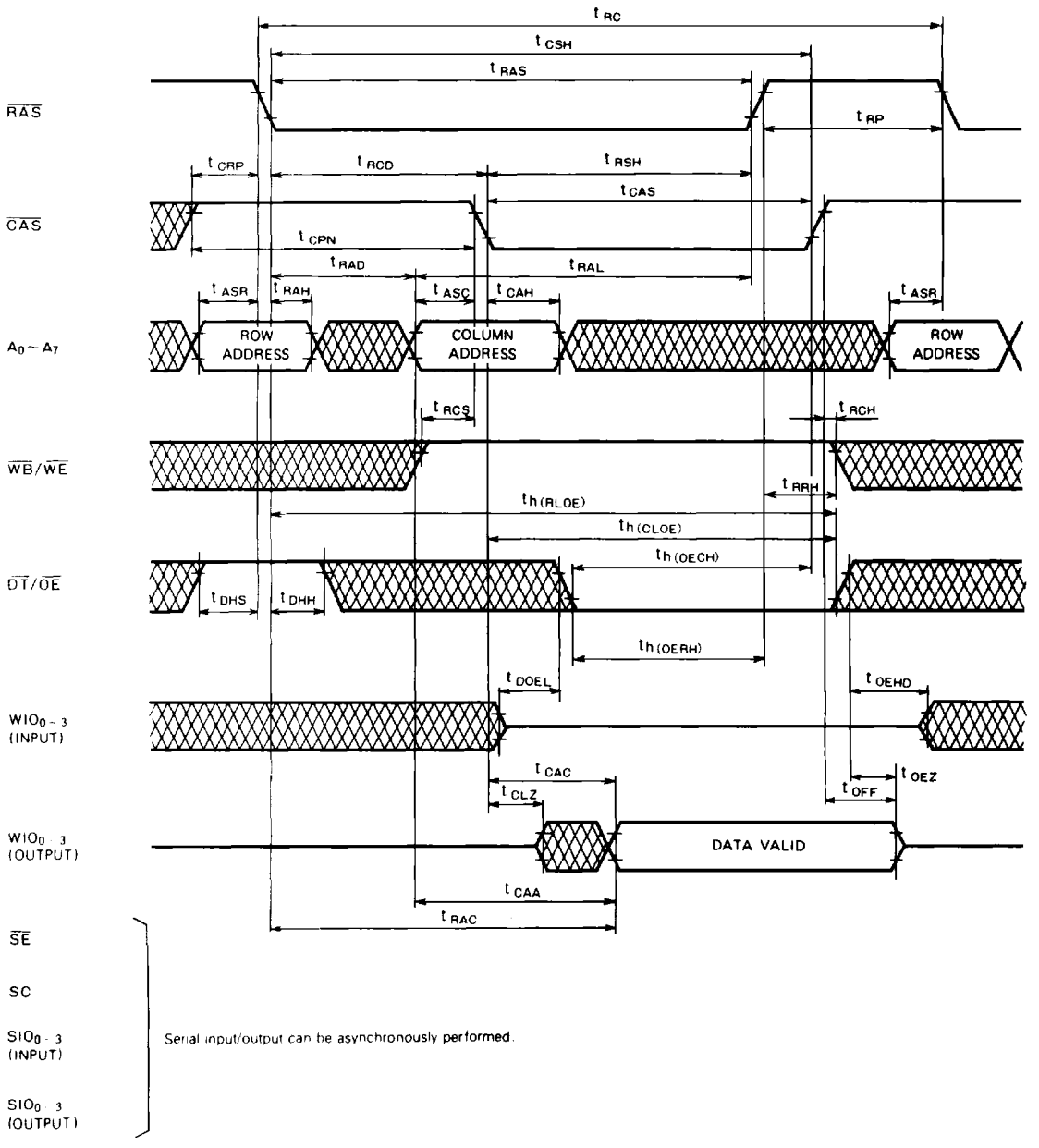
Symbol	Parameter	Limits						Unit
		M5M4C264-8		M5M4C264-10		M5M4C264-12		
		Min	Max	Min	Max	Min	Max	
$t_{SCC(R)}$	SC clock cycle time (Serial Read)	30		35		40		ns
$t_{SCC(W)}$	SC clock cycle time (Serial Write)	30		35		40		ns
t_{SCH}	SC high pulse width	10		10		15		ns
t_{SCL}	SC low pulse width	10		10		15		ns
t_{SOP}	$\overline{SE}$ high pulse width	10		10		10		ns
t_{SOE}	$\overline{SE}$ low pulse width	25		30		35		ns
t_{SIH}	Serial input data hold time after SC high	10		10		10		ns
t_{SIS}	Serial input data setup time before SC high	0		0		0		ns
t_{SWIH}	$\overline{SE}$ disable hold time after SC high	15		20		20		ns
t_{SWIS}	$\overline{SE}$ disable setup time before SC high	10		10		10		ns
t_{SWH}	$\overline{SE}$ enable hold time after SC high	15		20		20		ns
t_{SWS}	$\overline{SE}$ enable setup time before SC high	10		10		10		ns

Real Time Read Transfer

Symbol	Parameter	Limits						Unit
		M5M4C264-8		M5M4C264-10		M5M4C264-12		
		Min	Max	Min	Max	Min	Max	
t_{RDH}	$\overline{DT}$ hold time after $\overline{RAS}$	70		80		90		ns
t_{CDH}	$\overline{DT}$ hold time after $\overline{CAS}$	30		35		40		ns
t_{ADH}	$\overline{DT}$ hold time after address	35		40		45		ns
t_{SDD}	Delay time SC to $\overline{DT}$	15		20		20		ns
t_{SDH}	SC hold time after $\overline{DT}$	10		10		10		ns
t_{RDTD}	$\overline{DT}$ hold time after $\overline{RAS}$ high	0		0		0		ns

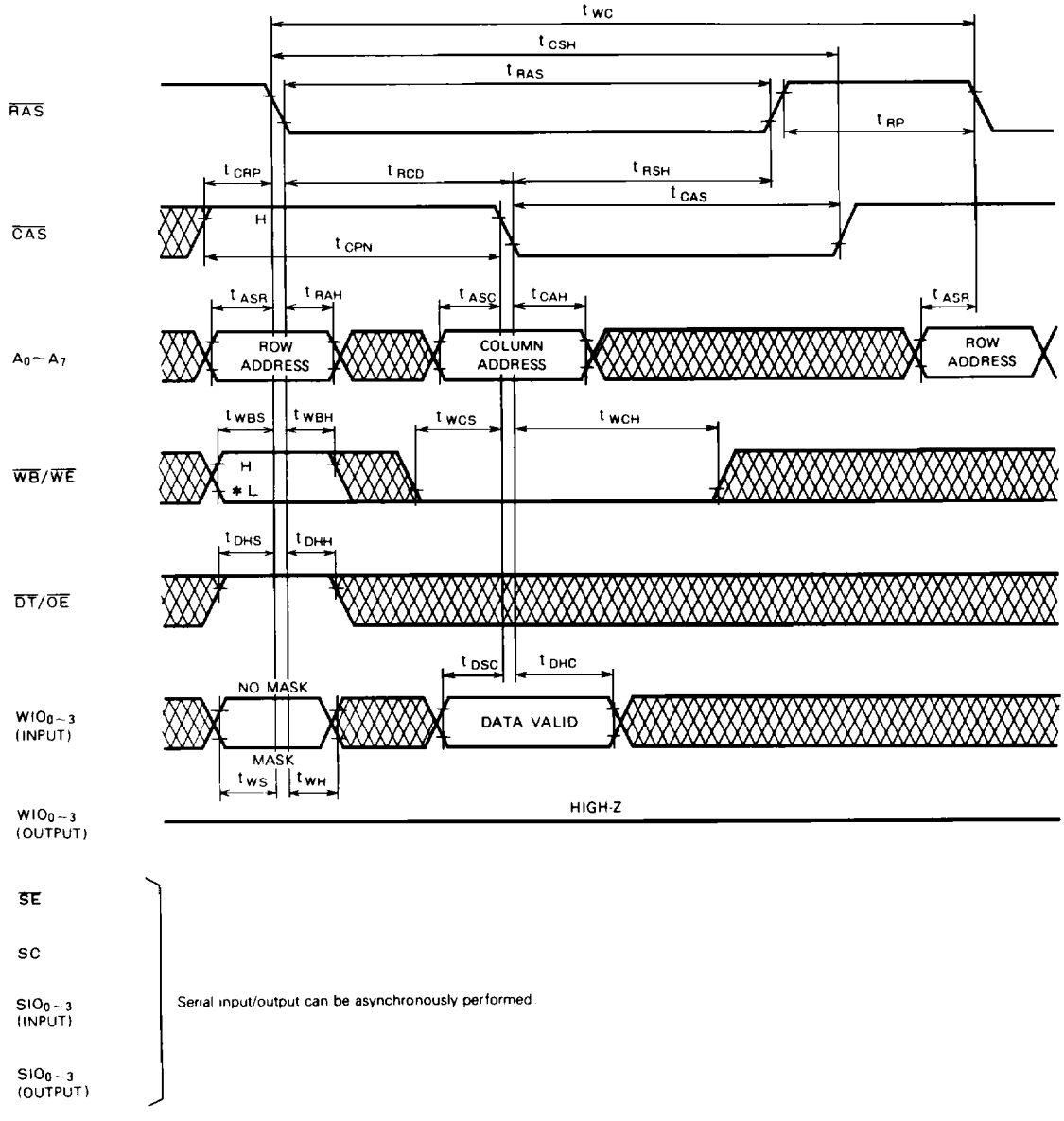
TIMING DIAGRAMS

Normal Read Cycle



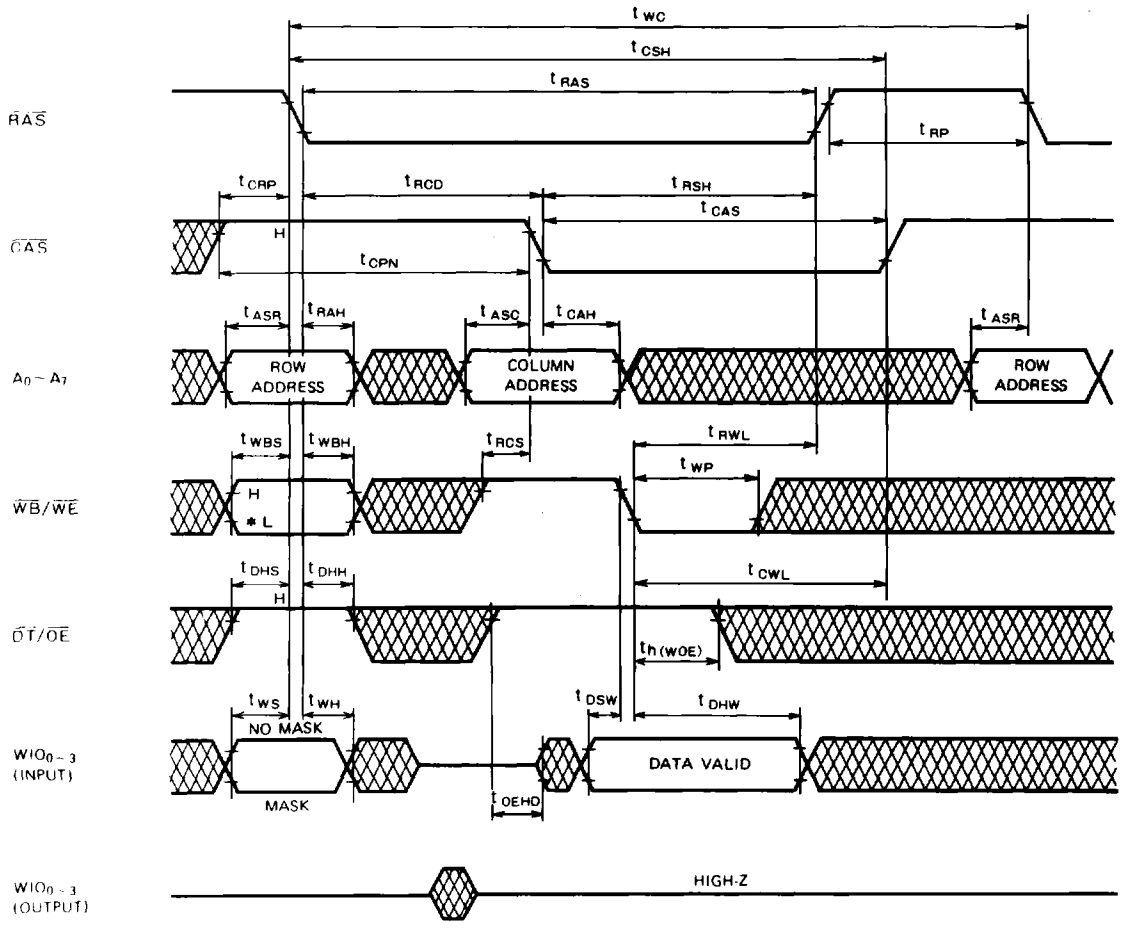
Serial input/output can be asynchronously performed.

Normal Write Cycle (Early Write)



*L = Write per bit operation (New mask)

Normal Write Cycle (Delayed Write)



*L = Write per bit operation (New mask)

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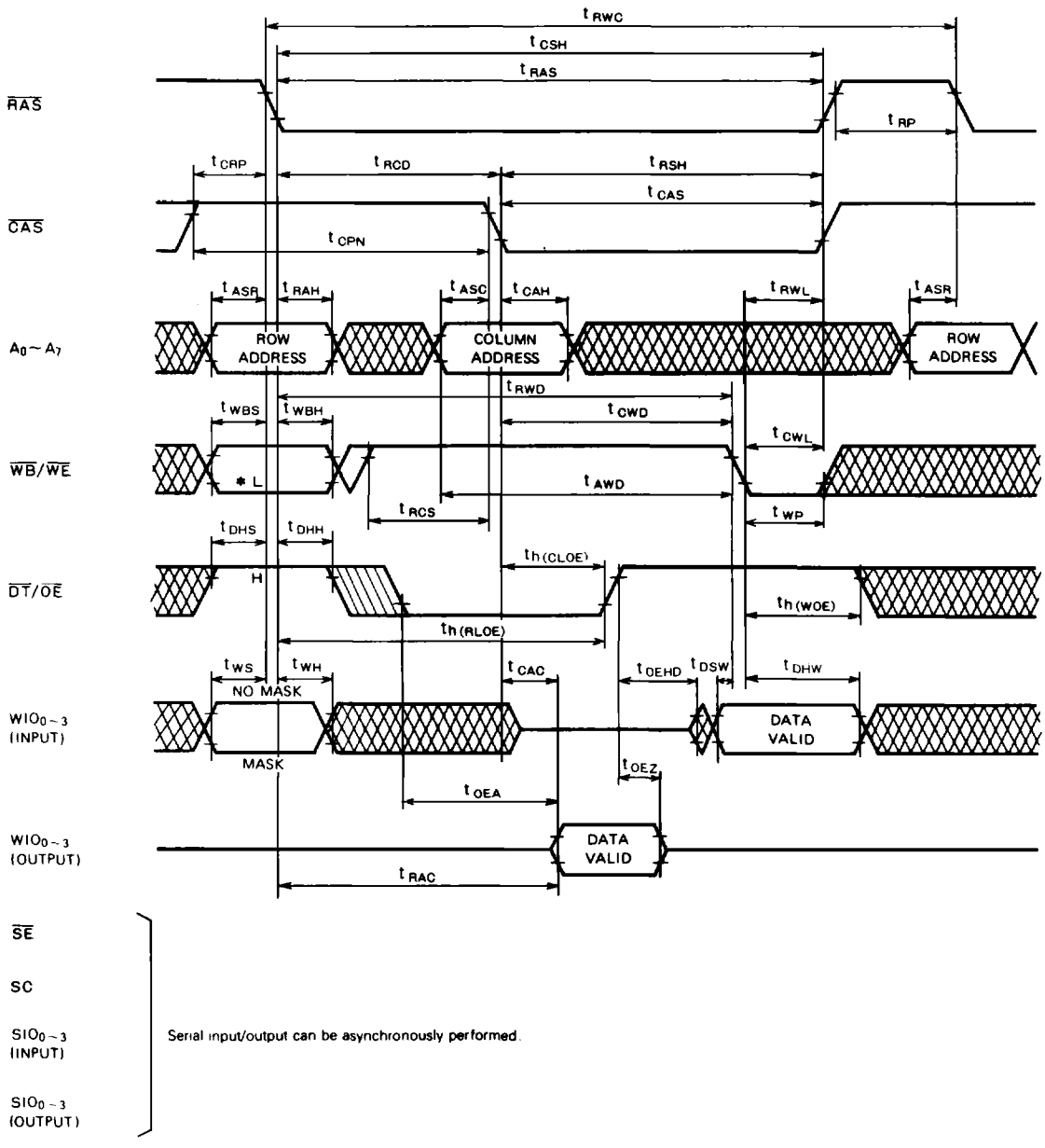
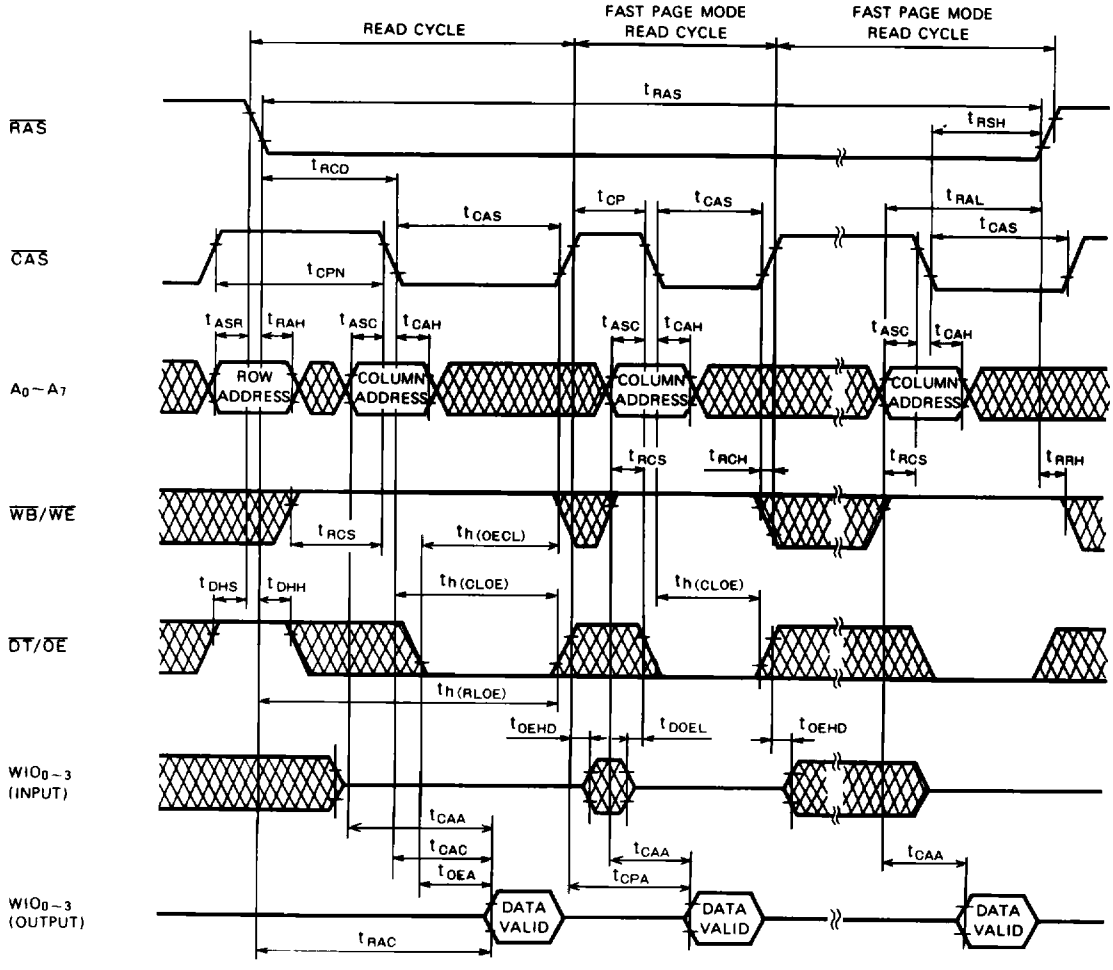
Normal Read Modify Write Cycle



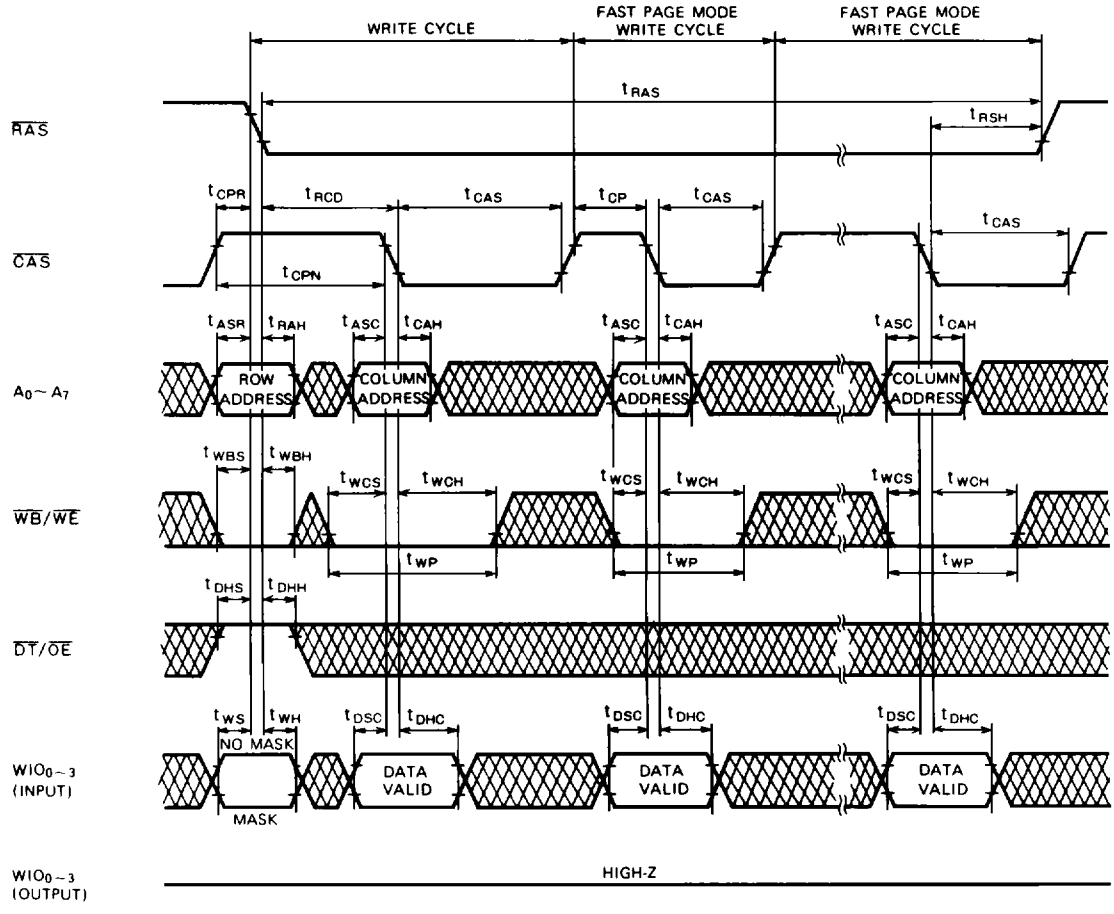
* L = Write per bit operation

Fast Page Mode Read Cycle



MITSUBISHI ELECTRIC

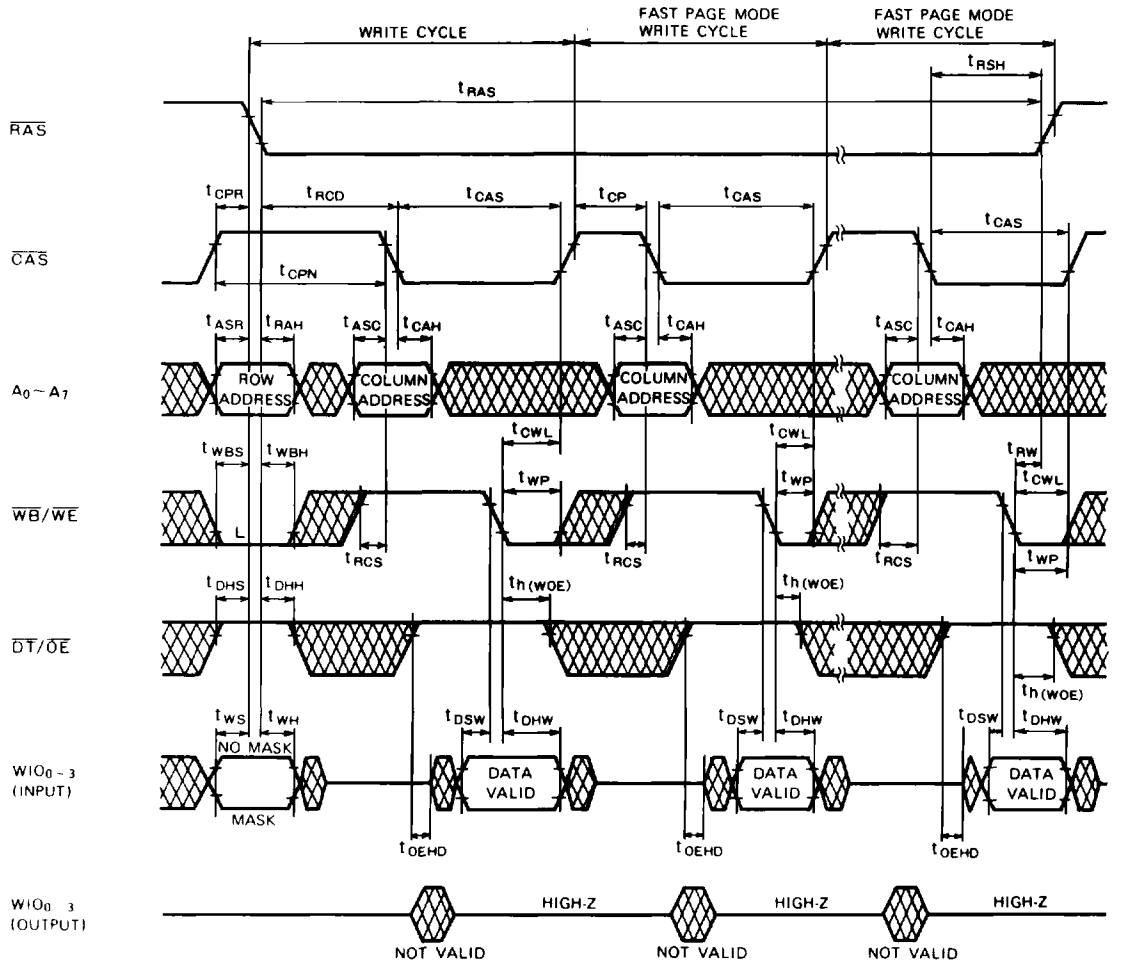
Fast Page Mode Early Write Cycle with New Mask



Serial input/output can be asynchronously performed.

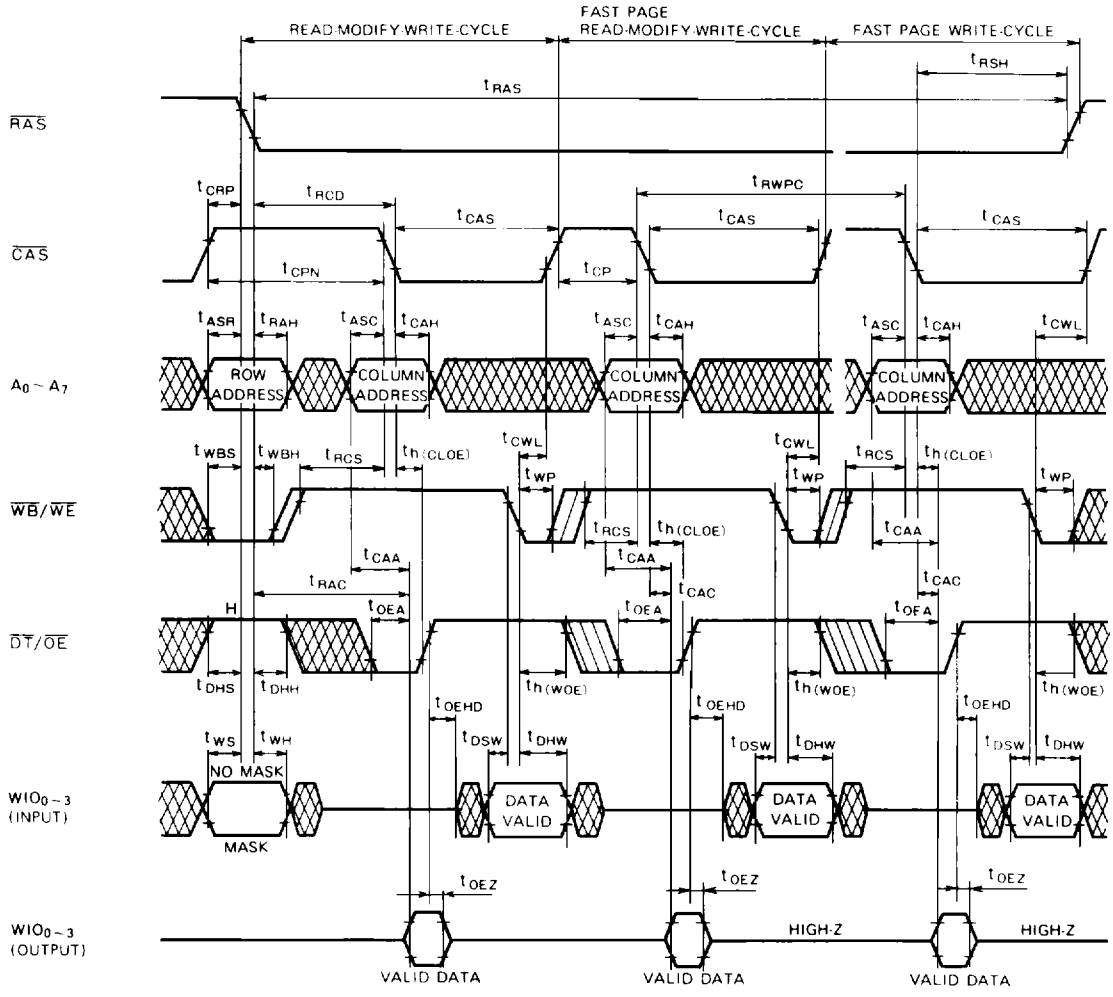
Write per bit operation mask is effective during the continuous page mode cycle.

Fast Page Mode Delayed Write Cycle with New Mask



Serial input/output can be asynchronously performed.
Write per bit operation mask is effective during the continuous page mode cycle.

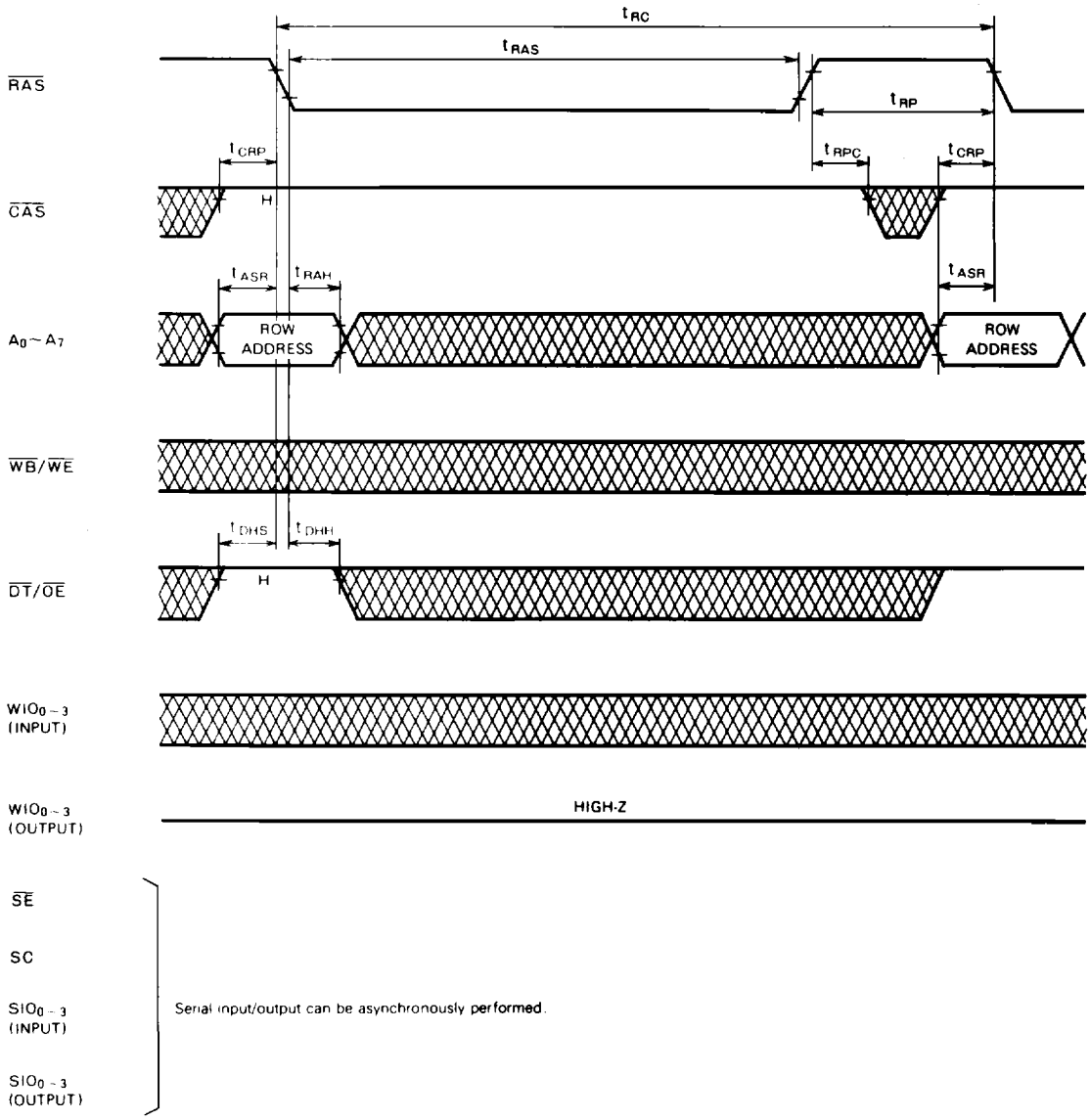
Fast Page Mode Read-Write, Read-Modify-Write-Cycle with New Mask



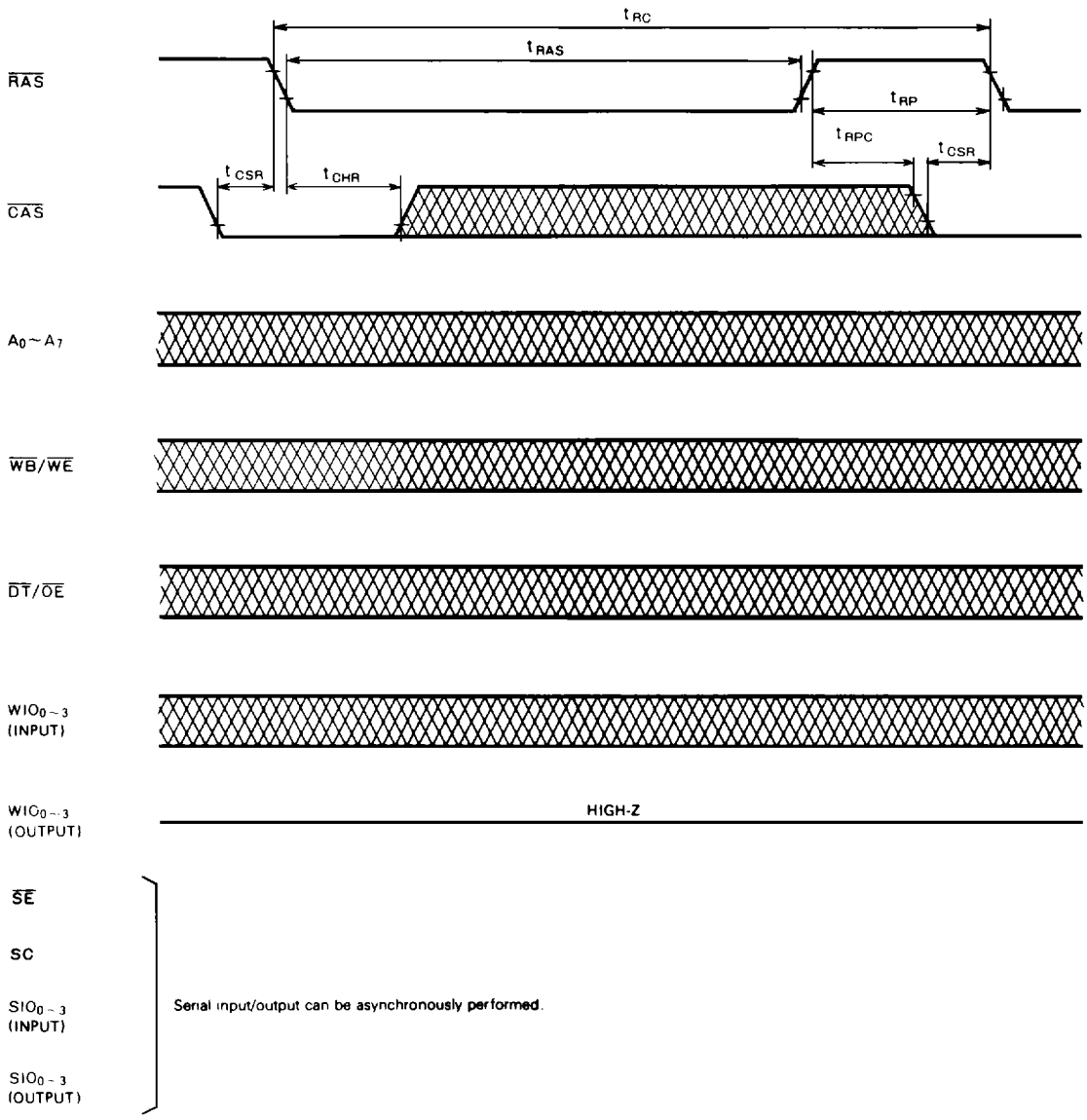
Serial input/output can be asynchronously performed

Write per bit operation mask is effective during the continuous page mode cycle.

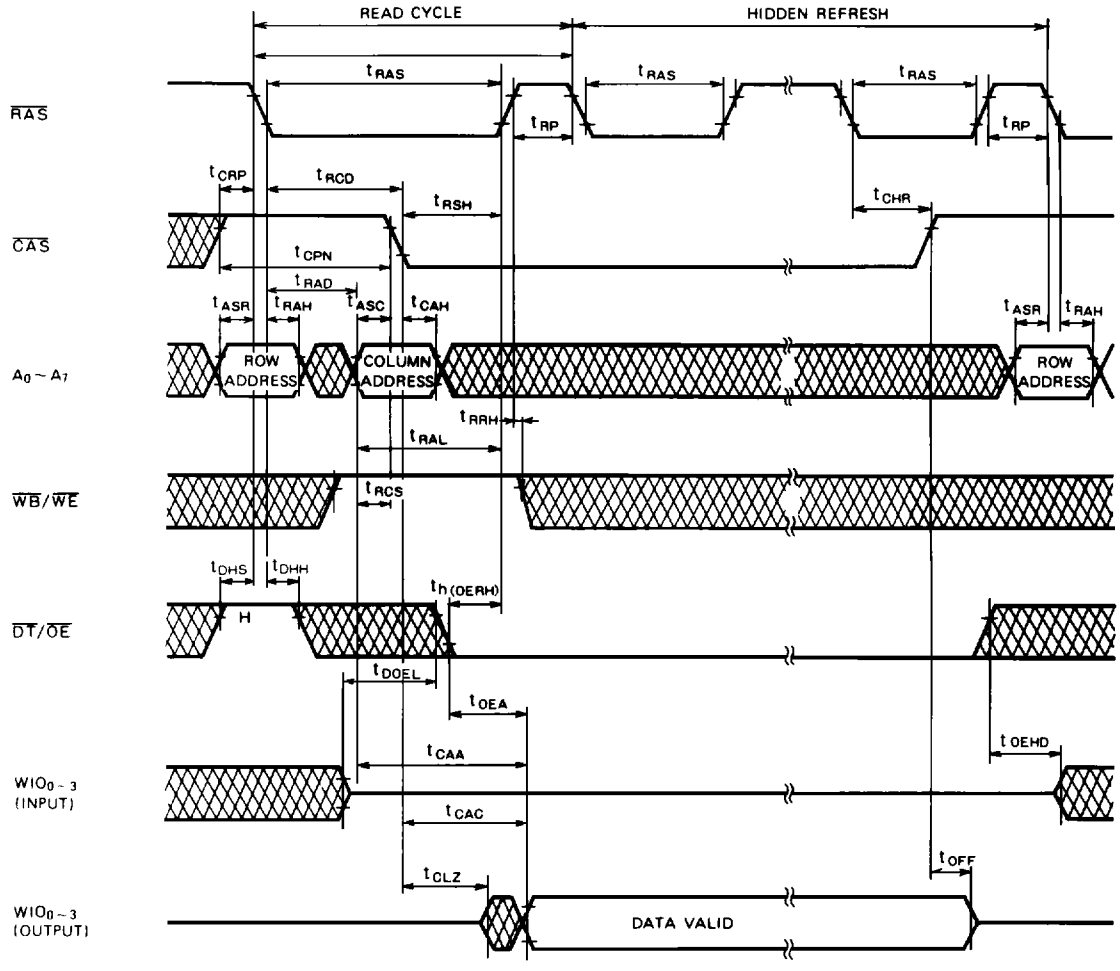
$\overline{RAS}$ only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Hidden Refresh Cycle (Automatic Refresh)



Serial input/output can be asynchronously performed.

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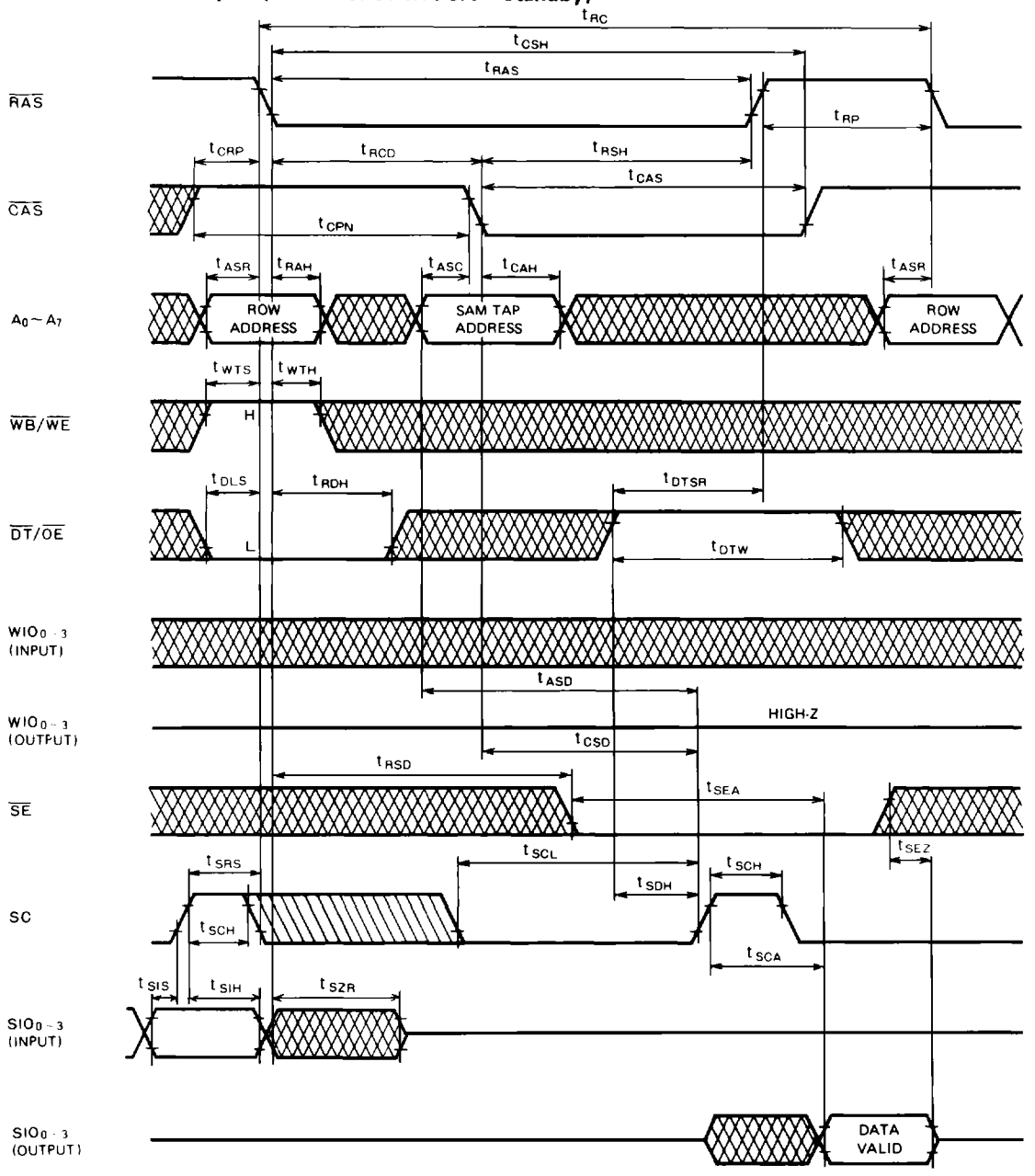
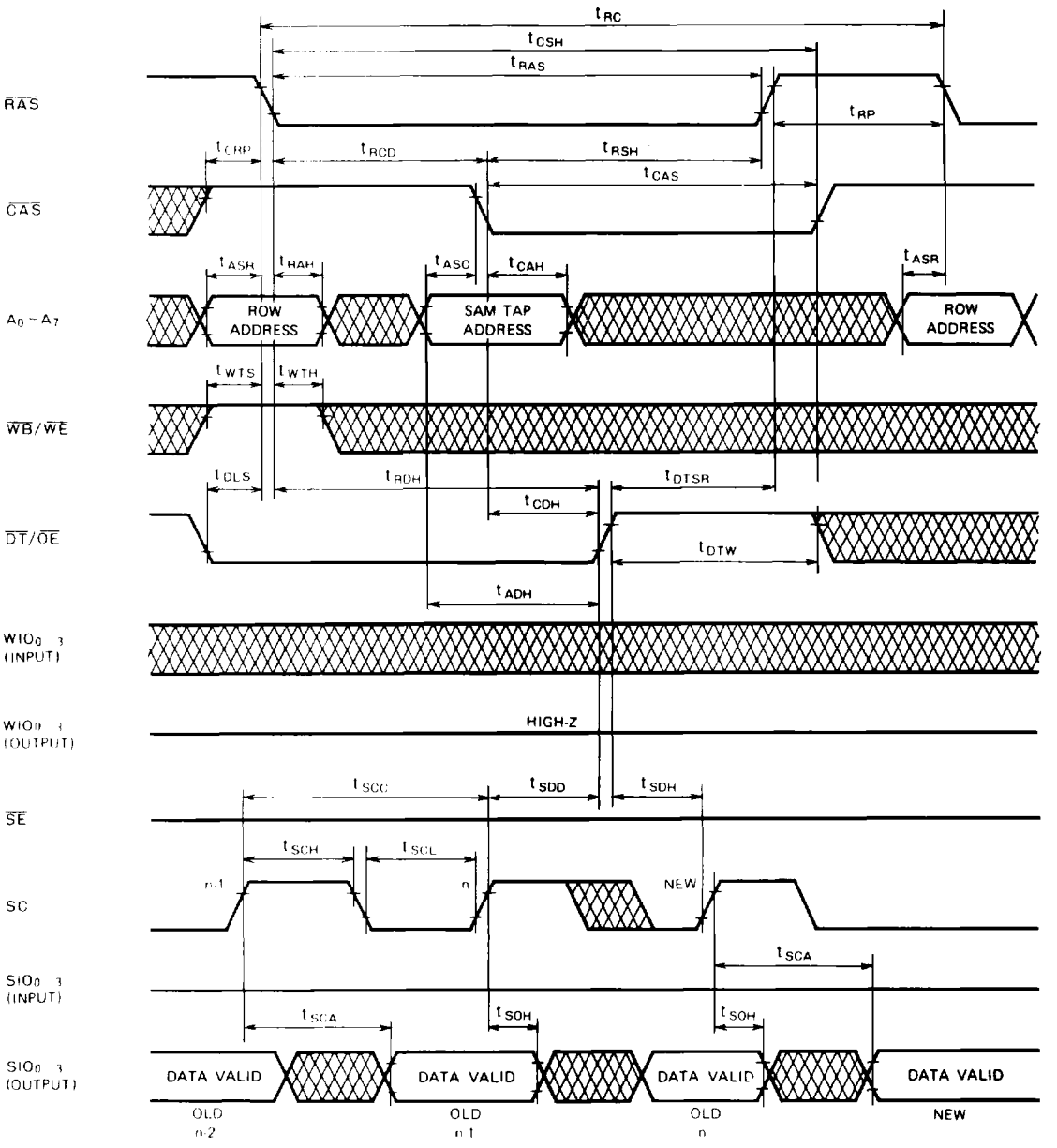
Normal Read Transfer Cycle (Pre-State: Serial Port = Standby)



Real-Time Read Transfer Cycle (To Active Register; Serial Port Active)



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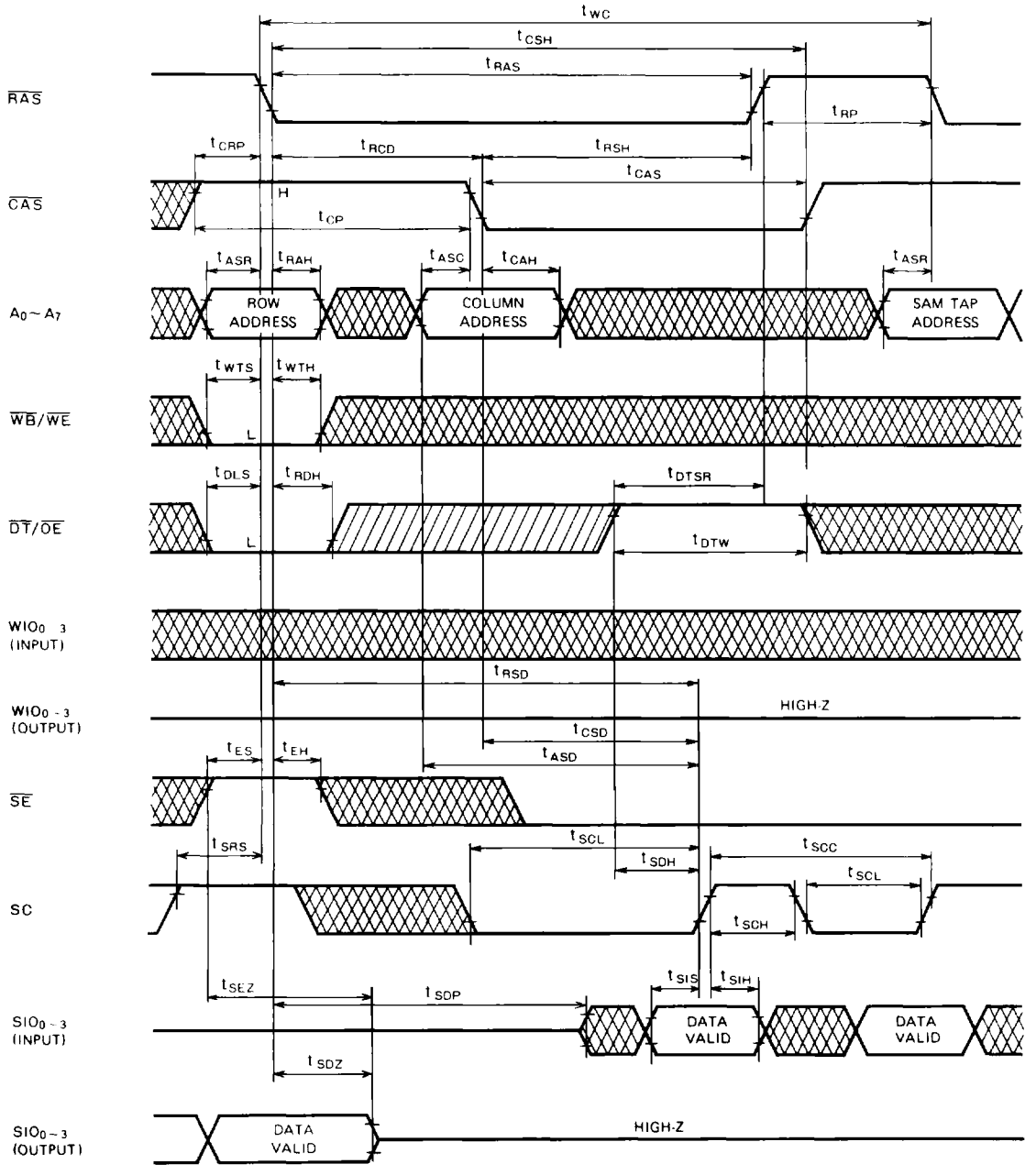
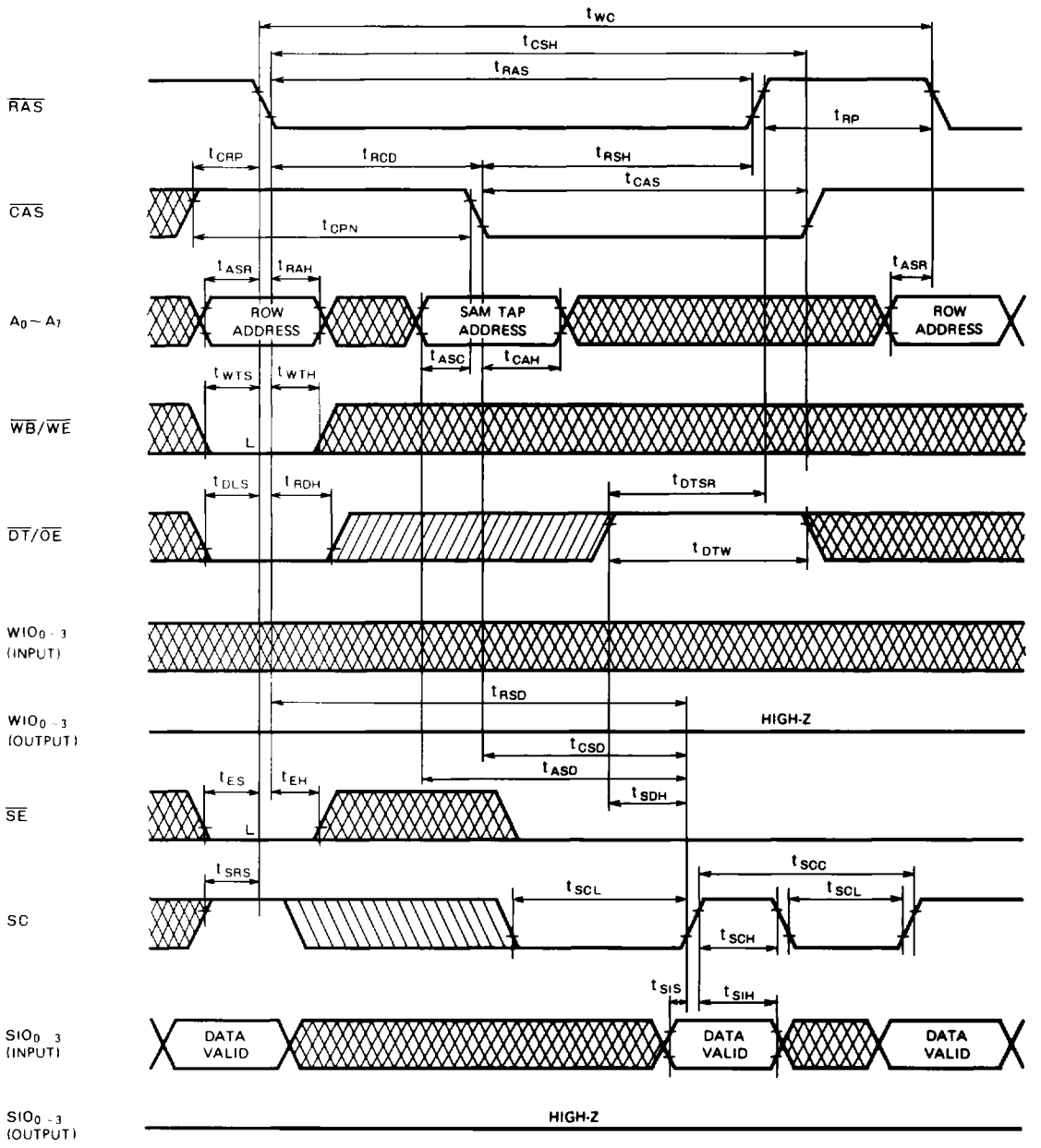
Pseudo Write Transfer Cycle (Serial Port Active) Serial Write Setup

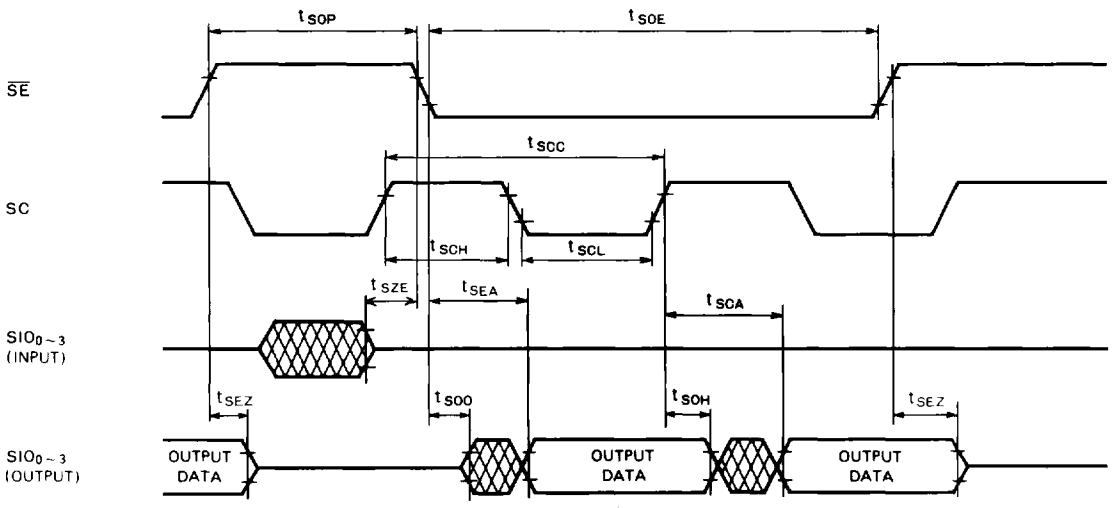


Note When $\overline{SE}$ is "H" level, the serial input data are not written into the Data Register, but the serial data selector works.

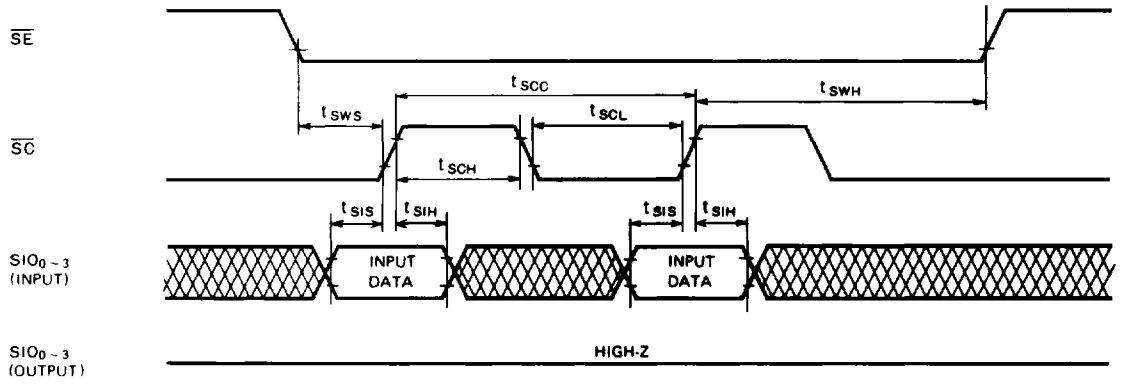
Write Transfer Cycle (Serial Port = Write Cycle)



Serial Read Cycle



Serial Write Cycle (SC Toggling, $\overline{SE}$ = L)



Serial Write Cycle ($\overline{SE}$ control)